

Process Parameters for Homework Problems

ECE 5411 – CMOS Analog IC Design (Spring 2014)

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Table 1: Long-channel MOSFET general design parameters.

Parameter	NMOS	PMOS
Scale factor (L_{min})	$1\ \mu m$	
V_{DD}	5 V	
V_{THN} and V_{THP}	0.8	0.9
KP_n and KP_p	$120\ \frac{\mu A}{V^2}$	$40\ \frac{\mu A}{V^2}$
$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$	$1.75\ \frac{fF}{\mu m^2}$	
Bias Current, I_D	$20\ \mu A$	$20\ \mu A$
W/L	10/2	30/2
V_{GS} and V_{SG}	1.05 V	1.15 V
$V_{DS,sat}$ and $V_{SD,sat}$	250 mV	250 mV
g_{mn} and g_{mp}	$150\ \frac{\mu A}{V}$	$150\ \frac{\mu A}{V}$
r_{on} and r_{op}	$5\ M\Omega$	$4\ M\Omega$
$g_{mn} \cdot r_{on}$ and $g_{mp} \cdot r_{op}$	$750\ \frac{V}{V}$	$600\ \frac{V}{V}$
λ_n and λ_p	$0.01\ V^{-1}$	$0.0125\ V^{-1}$
C_{oxn} and C_{oxp}	35 fF	105 fF
C_{gsn} and C_{sgp}	23.3 fF	70 fF
C_{gdn} and C_{dgp}	2 fF	6 fF
f_{Tn} and f_{Tp}	900 MHz	300 MHz

The corresponding $1\ \mu m$ CMOS models are available at the following file ocation on the AMS servers:

`/home/pdks/Cadence_IC61_CMOSedu/models/cmosedu_models.txt`

References

- [1] R. J. Baker, “CMOS: Circuit Design, Layout and Simulation,” 3rd ed., Wiley-IEEE, 2010: Sections 9.1&2, Tables 9.1 and 9.2.