

Homework 7

ECE 5/411 – CMOS Analog IC Design

Note:

1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.
2. Use the $1\ \mu\text{m}$ CMOS parameters from Table 1 posted on the site, along with the corresponding Spectre models.

Problem 1: Understand Examples 21.6-21.10 in the CMOS book. Fig. 1 shows amplifier circuits with wide-swing cascoded bias voltages (V_{bias1} to V_{bias4}) generated for the current and overdrive parameters from Table 1. For each of these amplifiers

- (a) Determine the frequency response (perform symbolic as well as numerical calculations for DC gain and pole-zero locations, and provide hand-sketched Bode magnitude and phase responses)
- (b) Estimate the unity-gain frequency (f_{un}), gain and phase margins for the amplifiers. Use $R_s = 1k\Omega$
- (c) Create circuit schematics and verify your calculations with Spectre simulations.

Extra: Use/modify the provided MATLAB scripts (*e.g.* `CommonSourceFreqResp1.m` or `TwoStageFreqResp1.m`) to generate frequency response and pole-zero plots to augment your understanding.

Problem 2: Read Section 6.3 in the Analog CMOS IC Textbook. Figure 2 shows a source follower (SF) designed using parameters from Table 1.

- (a) Determine the frequency response for Fig. 2 (a). Create circuit schematics and verify your calculations with Spectre simulations.
- (b) Assuming $R_s = 0$, derive the input AC impedance Z_{in} of the SF. Show that the overall input capacitance contributed by M_1

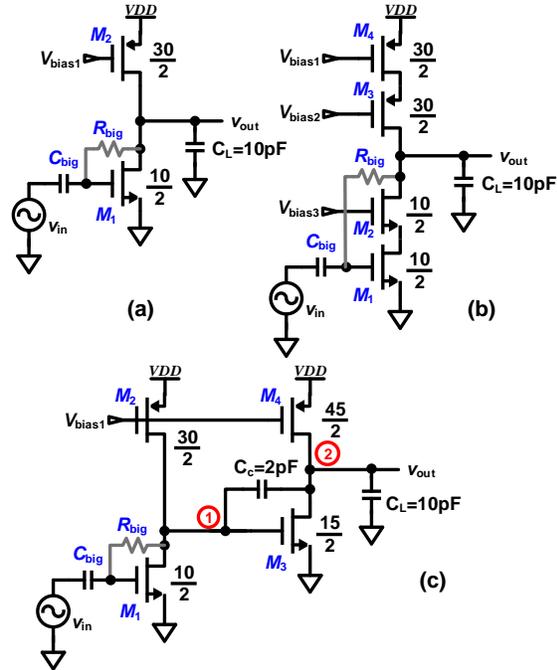


Figure 1

is the sum of C_{gd1} and a fraction of C_{gs1} . Plot $|Z_{in}(f)|$ using Spectre and verify your results.

(c) Figure 2 (b) shows the SF driving a large load with a pulsed source. It can be shown that the equivalent output impedance of the SF can be expressed as an inductive combination $Z_{out} = (sL || R_1) + R_2$. Here, $R_2 = \frac{1}{g_{m1}}$, $R_1 = R_s - \frac{1}{g_{m1}}$ and $L = \frac{C_{gs1}}{g_{m1}} \left(R_s - \frac{1}{g_m} \right)$. This property is commonly used to realize active inductors on chip. Using Spectre, plot $|Z_{out}(f)|$ for the cases including $R_s \gg \frac{1}{g_{m1}}$ and $R_s \ll \frac{1}{g_{m1}}$ to demonstrate this behavior.

(d) In Figure 2 (b), use a 10 MHz clock source as the input to the SF, and plot output response for $R_s = 0, 50\Omega, 1k\Omega, \text{ and } 10k\Omega$. Explain the results.

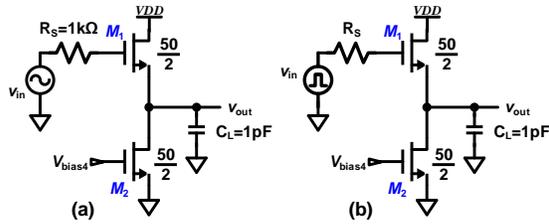


Figure 2

Problem 3: Figure 3 (a) shows the canonical model discussed in class for a two-stage amplifier with Miller compensation (i.e. pole-splitting). Use values: $g_{m1} = 20 \frac{\mu A}{V}$, $R_1 = 4M\Omega$, $g_{m2} = 80 \frac{\mu A}{V}$, $R_2 = 0.5M\Omega$, $C_{in} = 10fF$, $C_1 = 40fF$, $C_C = 250fF$, $C_L = 1pF$, $R_z = 12.5k\Omega$. Suitably modify the MATLAB file *TwoStage-FreqResp1.m* for the individual parts of this problem.

(a) Determine the poles and zeros of the open-loop transfer function $\frac{v_{out}}{v_{in}}(s)$ -calculate the transfer function symbolically and then numerically. Show the pole-zero plot, Bode magnitude and phase response and determine- low-frequency gain (A_v), unity-gain frequency (f_{un}) and phase margin (ϕ_M).

(b) Using the method used in class, show that the zero location in the amplifier without zero-nulling resistor R_z is given by $\omega_z = \frac{g_{m2}}{C_c}$. Similarly, derive the expression for the zero location when a zero-nulling resistor R_z is added in series with C_c . Using the MATLAB script demonstrate pole-splitting (root locus for varying C_C) with zero-nulling.

(c) The circuits in Fig. 3 (b, c) are modified versions of the two-stage Miller compensated amplifier. Calculate their transfer functions and compare them with that of the conventional structure. Explain the difference with results.

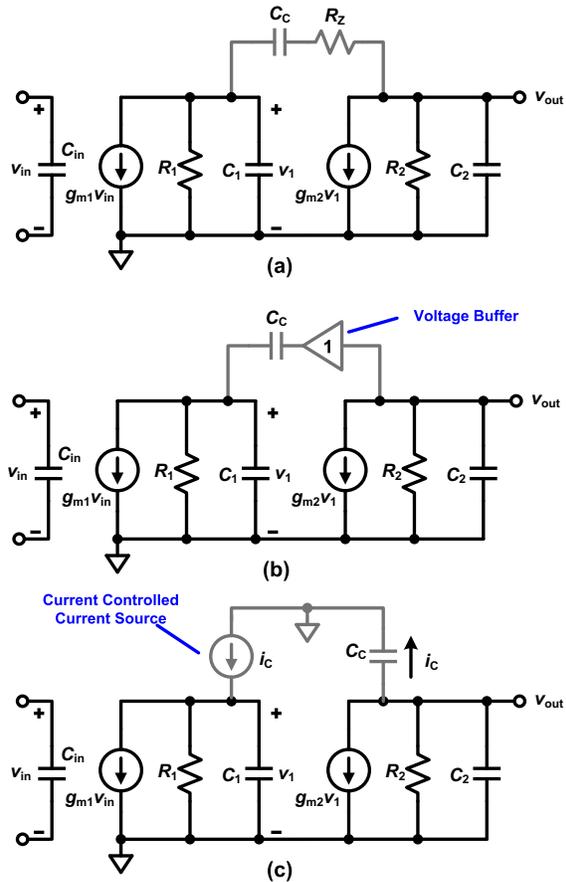


Figure 3