Homework 4

ECE 5/411 – CMOS Analog IC Design

Note:
1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.
2. Use the 1 μm CMOS parameters from Table 1 posted on the site, along with the corresponding Spectre models.

Problem 1: The impedance looking into a circuit node (R_x) can be estimated by finding the AC current (i_x) flowing into that node, when an AC voltage source (V_x) is applied (using DC coupling). See Fig. 1 for illustration of this method, where $R_x = \frac{v_x}{i_x}$.

(a) For the circuits in Fig. 1, estimate the impedance R_x.

(b) Using AC analysis in Spectre, verify results in part (a). In your simulations select a value of the decoupling capacitor C_{big}, such that the cut-off frequency of the decoupling network (ω_x) is much smaller than the AC source frequency (ω_{in}), i.e. $\omega_x = \frac{1}{R_x C_{big}} \leq \frac{\omega_{in}}{10}$.

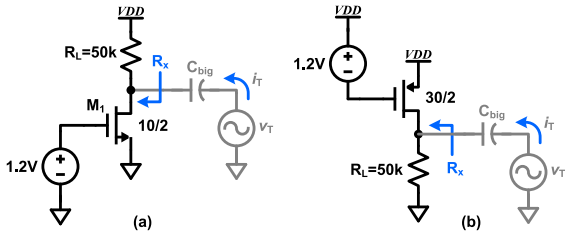

Figure 1

Problem 2:

(a) Calculate the currents and voltages in the circuit in Fig. 2 (a). What is the maximum value allowed for R_2 so that M_2 remains operating in the saturation region? Verify results with simulation.

(b) Sketch I_x vsV_x for the circuit shown in Fig. 2 (b).

Problem 3: Estimate the current I_X flowing in circuits shown in Fig. 3. Verify results with simulations.

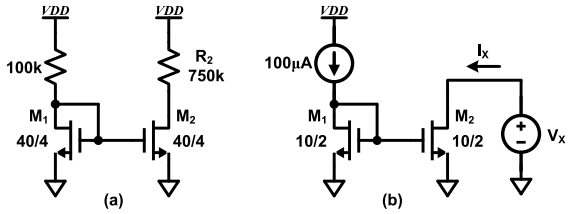

Figure 2

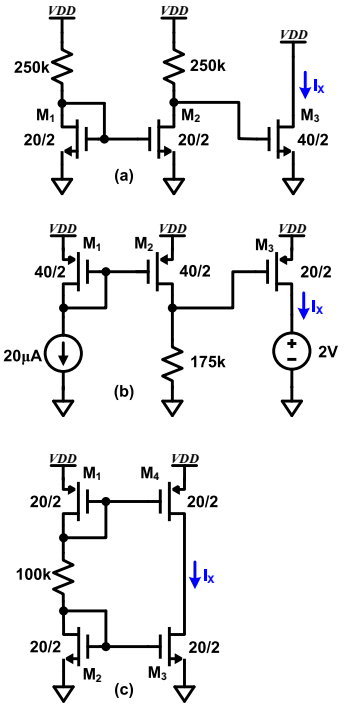

Figure 3

Problem 4: In the circuit below, M_1 and M_2 both operate in saturation. Further, KP_n and W/L for both transistors is the same. The threshold voltage of M_2 is *slightly* larger than that of M_1, and given by $V_{THN_2} = V_{THN_1} + \Delta V_{THN}$. Assuming $\Delta V_1 \ll V_1$, determine the current I_2.

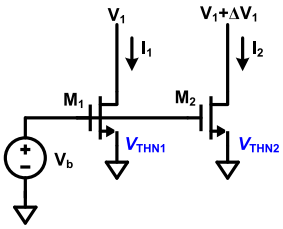

Figure 4