Homework 3

ECE 5/411 – CMOS Analog IC Design

Note:
1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.
2. Use the $1\,\mu m$ CMOS parameters from Table 1 posted on the site, along with the corresponding Spectre models.

Problem 1: For an NMOS device operating in saturation, sketch W/L versus $V_{GS} - V_{THN}$ if (a) I_D is constant, (b) g_m is constant.

Problem 2: Find the DC and AC, voltages as well as the currents in the circuits shown in Figure 1. Clearly show all the hand calculations and compare them with Spectre results (use $1\mu m$ models).

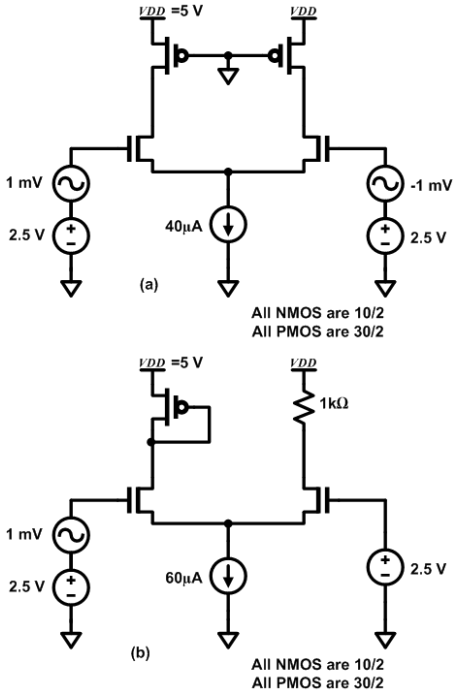

Figure 1

Problem 3: In this problem, we will further explore the notion of *small-signal*. Consider two non-linear amplifiers with their input output characteristics (i.e. the large signal response) given by $V_{out} = \frac{V_{in}^2}{V_A}$ and $V_{out} = V_A e^{\frac{V_{in}}{V_A}}$.

(a) A small-signal gain ($A_v = \frac{v_{out}}{v_{in}}$) of 10 is desired from both of these amplifiers. Determine the operating points so that this gain can be achieved.

(b) Recall that the small-signal approximation is valid only when the higher order terms in the Taylor series expansion can be neglected when compared to the linear term. Compare the second order derivative of the two amplifiers around the operating point. What can you say about the relative magnitudes of the incremental inputs for each of the amplifiers which qualify as small signals ?

Problem 4 - Process Characterization: Using the TSMC 180n CMOS models ($V_{DD} = 1.8V$, $L_{min} = 0.18\mu$):

(a) Regenerate Table 1 below for an overdrive ($V_{OV} = V_{GS} - V_{THN}$) equal to 5% of V_{DD}. Use $L = 2 \cdot L_{min}$ and state your assumptions. Show all the relevant simulation plots. *Save all your neatly created simulation test-benches for upcoming homeworks and project.*

(b) For the NMOS and PMOS devices in your table, plot f_T, $g_m r_o$ and $g_m r_o \cdot f_T$ as a function of overdrive (V_{OV}). Interpret each of these graphs. (*You may plot these results in any software like Excel or Matlab.*)

(c) For the NMOS and PMOS above, plot $\frac{g_m}{I_D}$ as a function of overdrive (V_{OV}). Interpret the trend in this graph?

Table 1: Long-channel MOSFET general design parameters.

Parameter	**NMOS**	**PMOS**
Scale factor (L_{min})	$0.18\,\mu m$	
V_{DD}	1.8 V	
V_{THN} and V_{THP}		
KP_n and KP_p		
$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$		
Bias Current, I_D		
W/L		
V_{GS} and V_{SG}		
$V_{DS,sat}$ and $V_{SD,sat}$		
g_{mn} and g_{mp}		
r_{on} and r_{op}		
$g_{mn}.r_{on}$ and $g_{mp}.r_{op}$		
λ_n and λ_p		
C_{oxn} and C_{oxp}		
C_{gsn} and C_{sgp}		
C_{gdn} and C_{dgp}		
f_{Tn} and f_{Tp}		