ECE 511 - Lecture 8

Note Title 2/13/2014

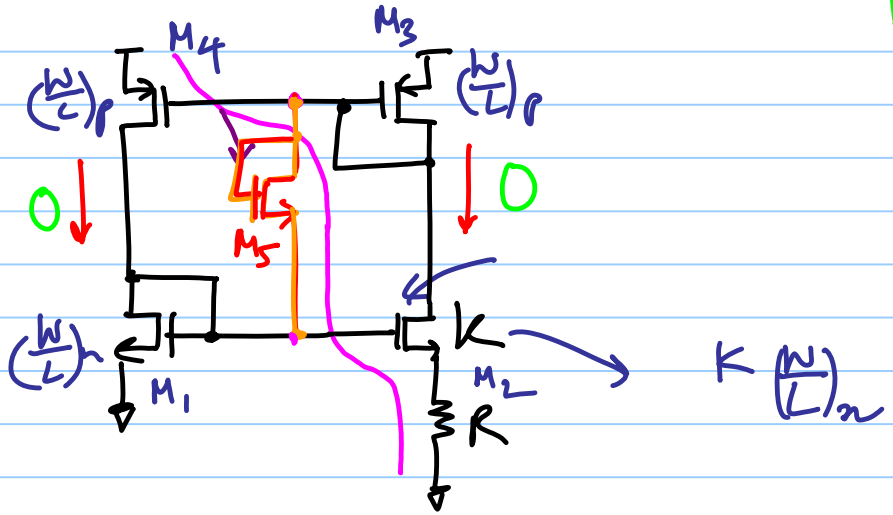
HW 3, Prob 4 → Submit Electronically (preferably) on Tuesday (Feb 18)

HW 4 → Pushed to Thursday (Feb 20)

BGR

$$I_{out} \triangleq I_{ref} = \left\{ \frac{2}{\beta R^2}\left(1-\frac{1}{\sqrt{K}}\right)^2, \cancel{0} \right\}$$

Desired



"Start-up Problem"

* M_5 provides current path from M_3 to M_1 ⇒ M_2 & M_4 turned on
  ↳ Causes I_{out} to snap to the desired value

* In normal operation M_5 should stay off.

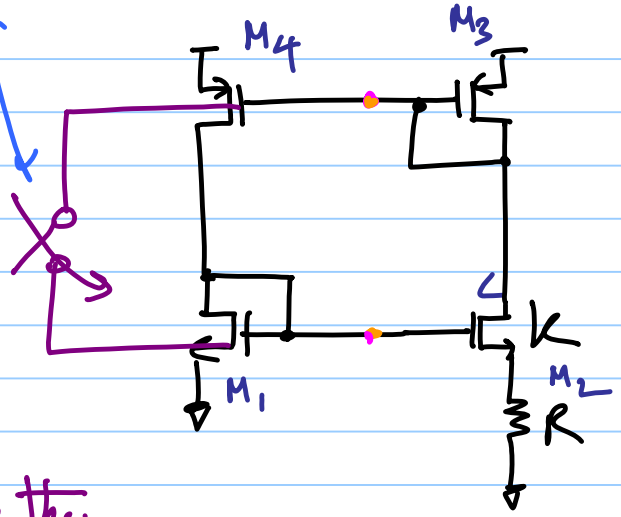
$$V_{GS_5} = V_{DD} - V_{GS_1} - V_{SG_3} < V_{THN_5} \longrightarrow \text{OFF}$$

To turn M_5 ON:

$$V_{THN_1} + V_{THN_5} + V_{THN_3} < V_{DD} \longrightarrow \text{ON}$$

* Not a robust design

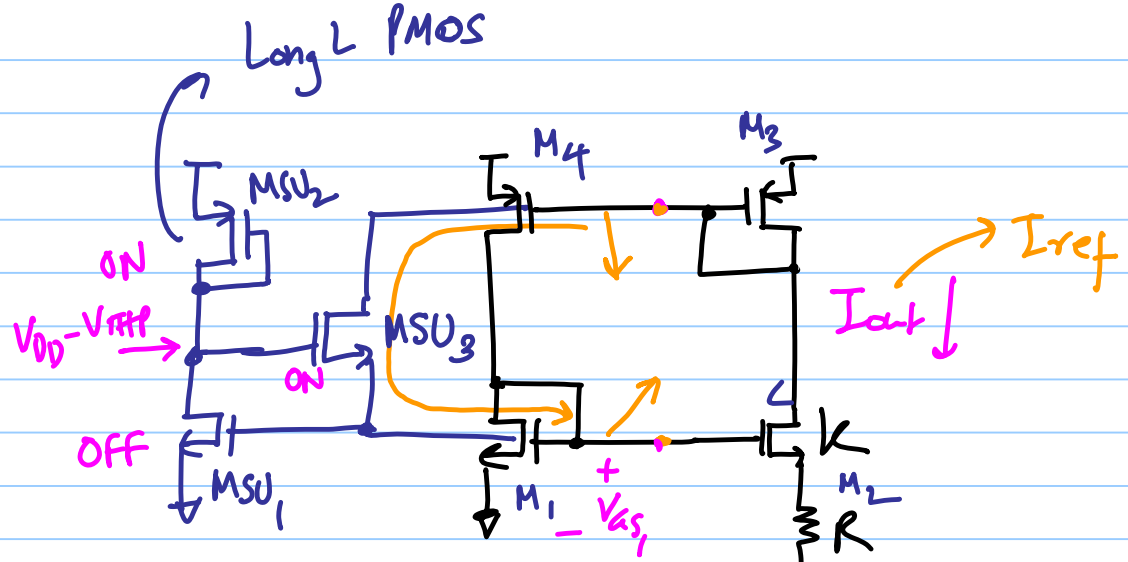
NMOS switch

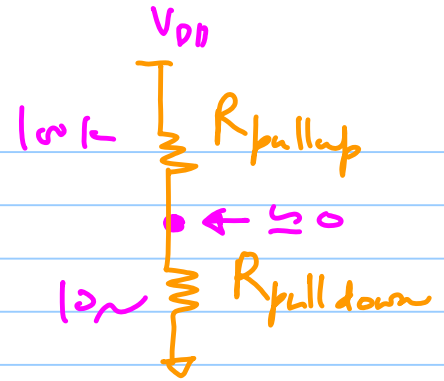


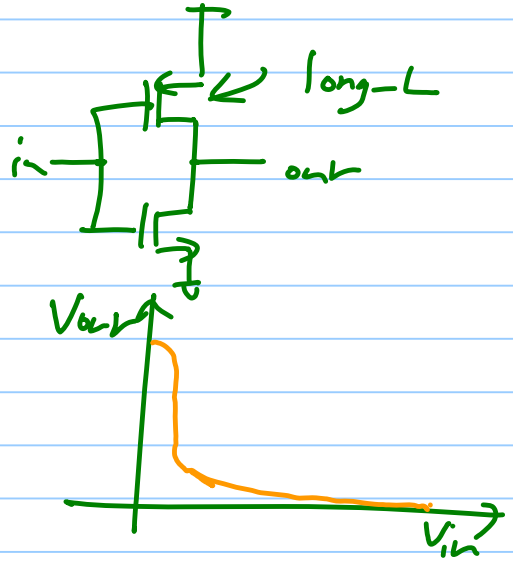
Closed when
$V_{GS_1} = 0$

Open when

V_{GS_1} snaps to the desired value

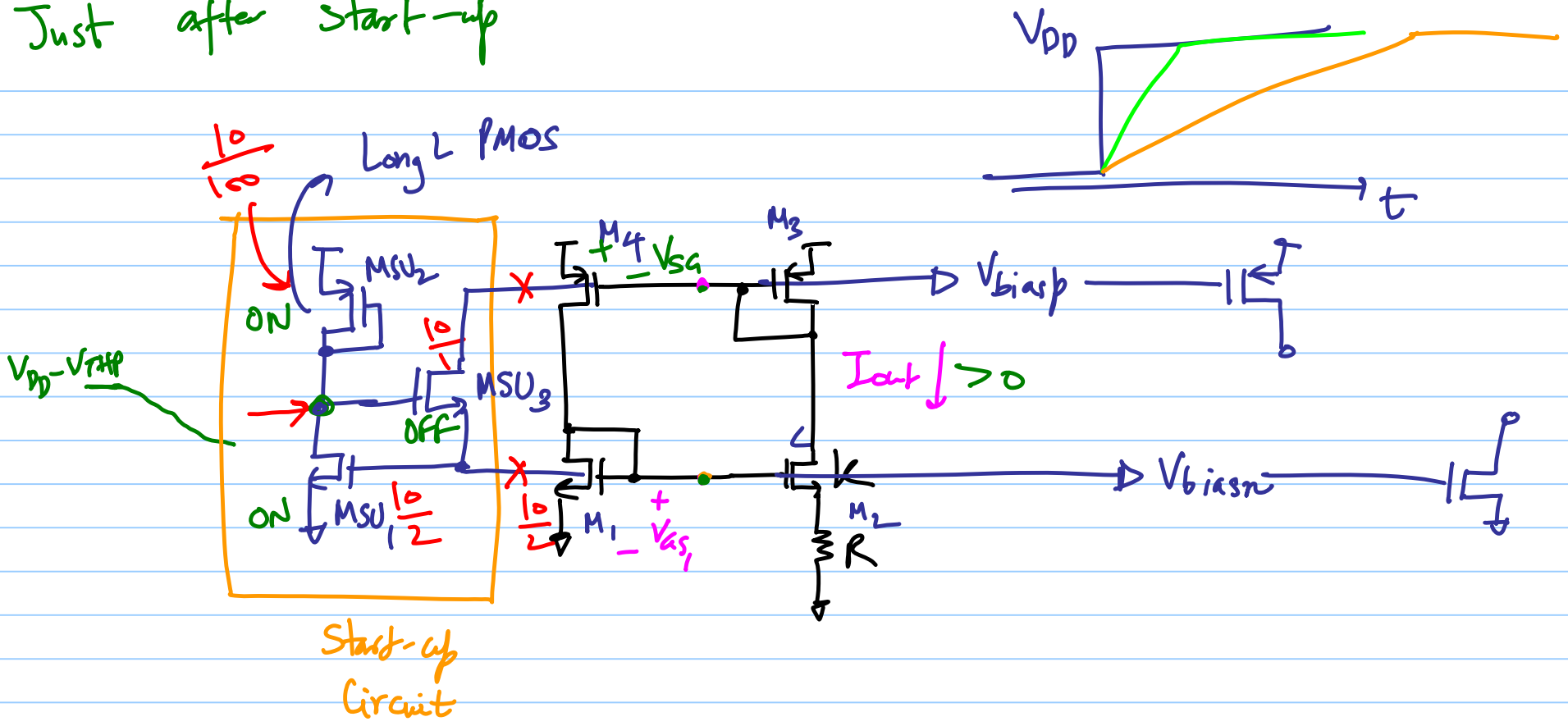






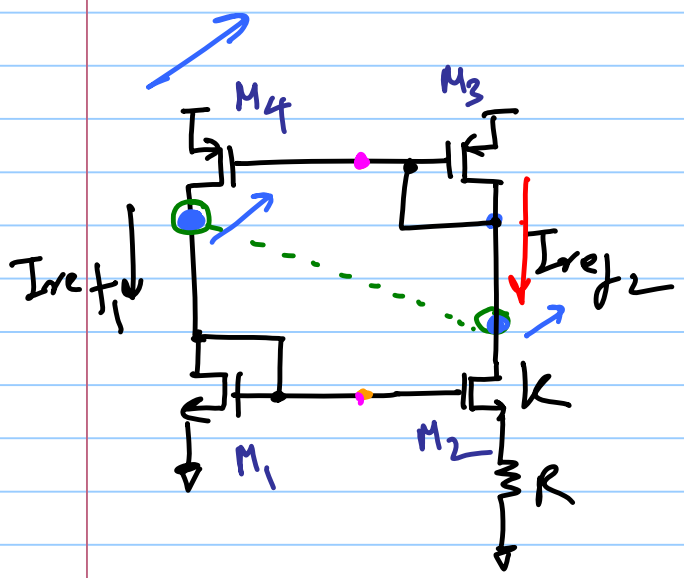
- $t=0^-$, $I_{out}=0 \Rightarrow V_{GS_1}=0$

Just after start-up

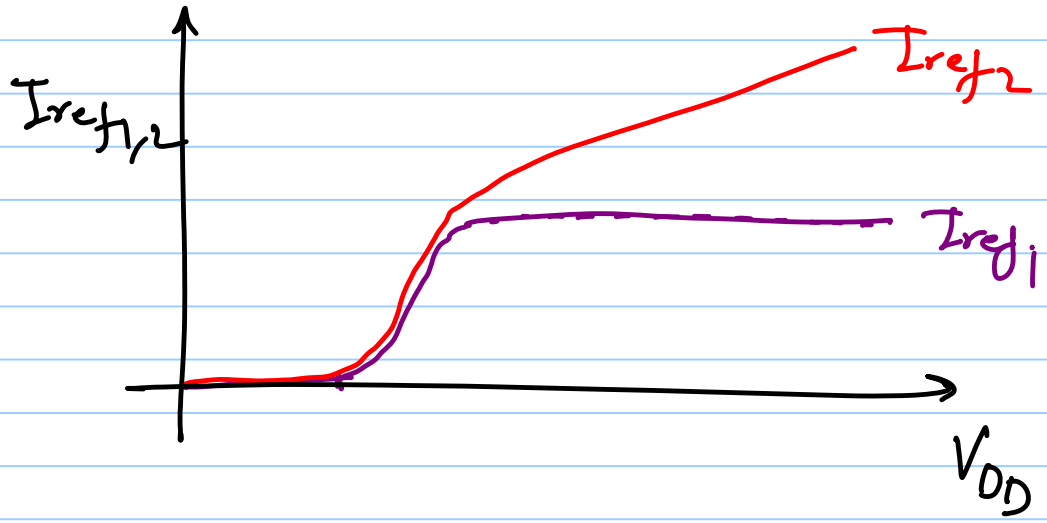


Short-channel BMR Design

$\lambda > 0$

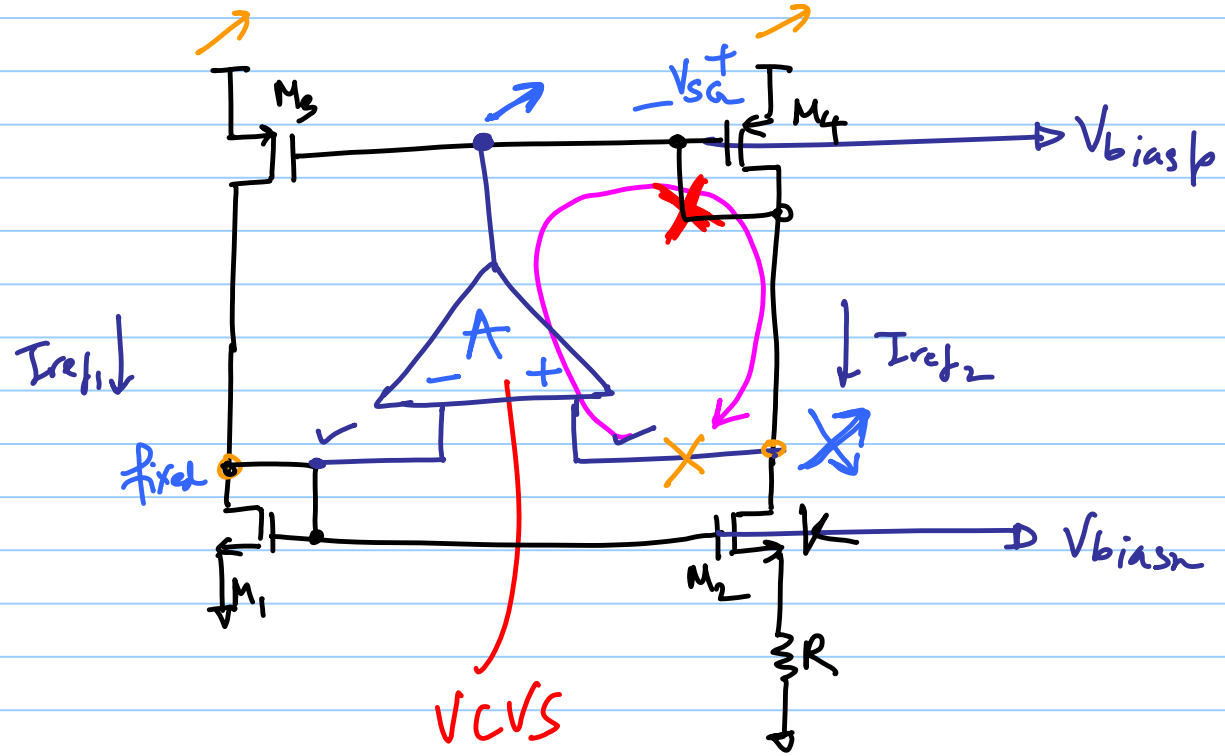


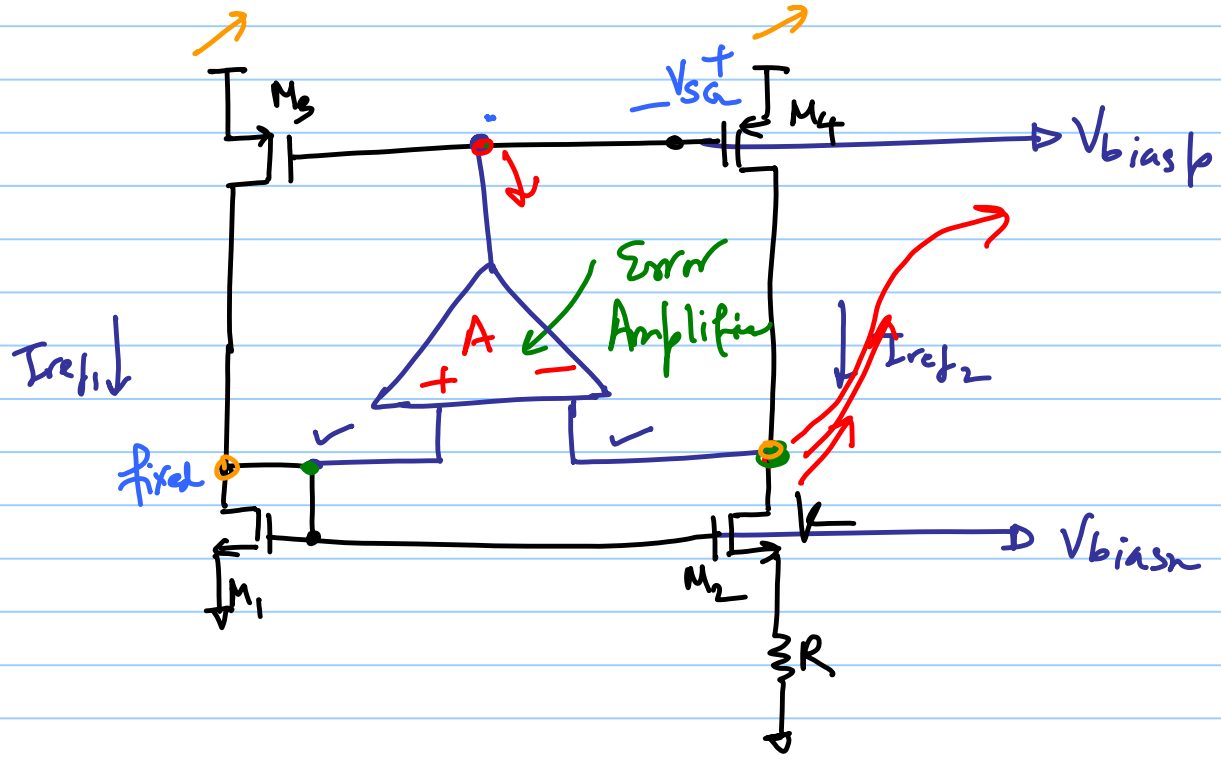
CMOS fig 20.18



* Bad supply sensitivity due to V_{DS} variation in the mirror

-ve feedback loop



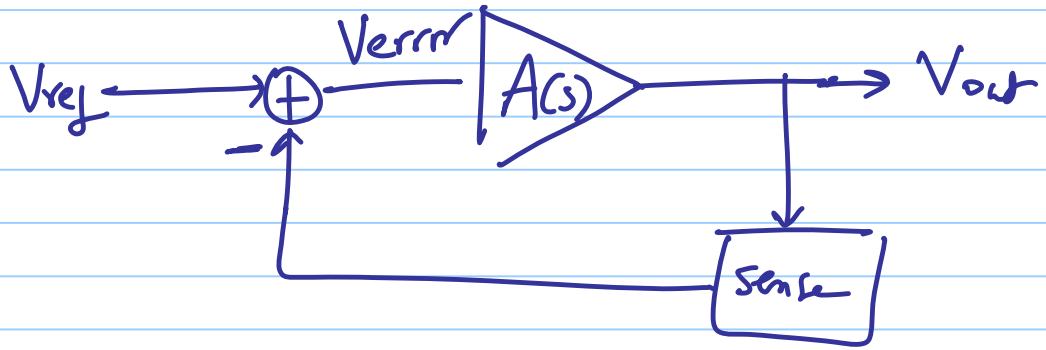


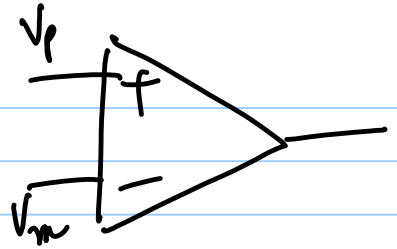
+ve feedback Case

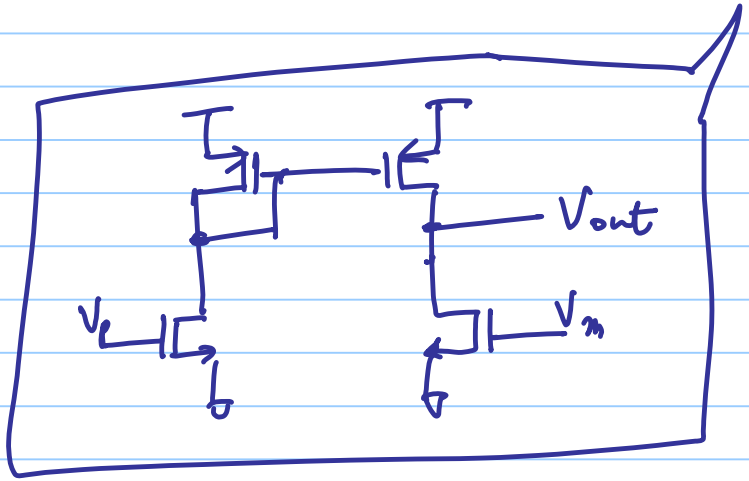
✗

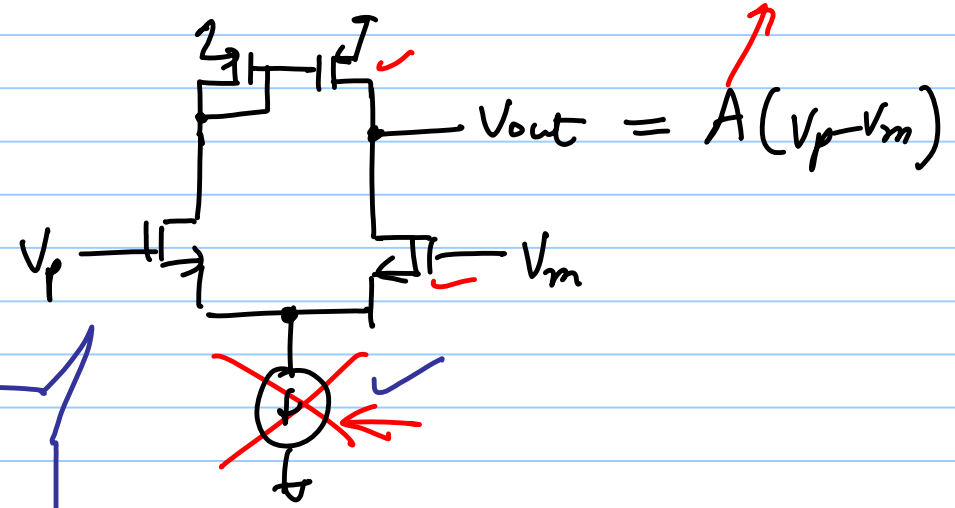
flip the polarity of the Error Amplifier

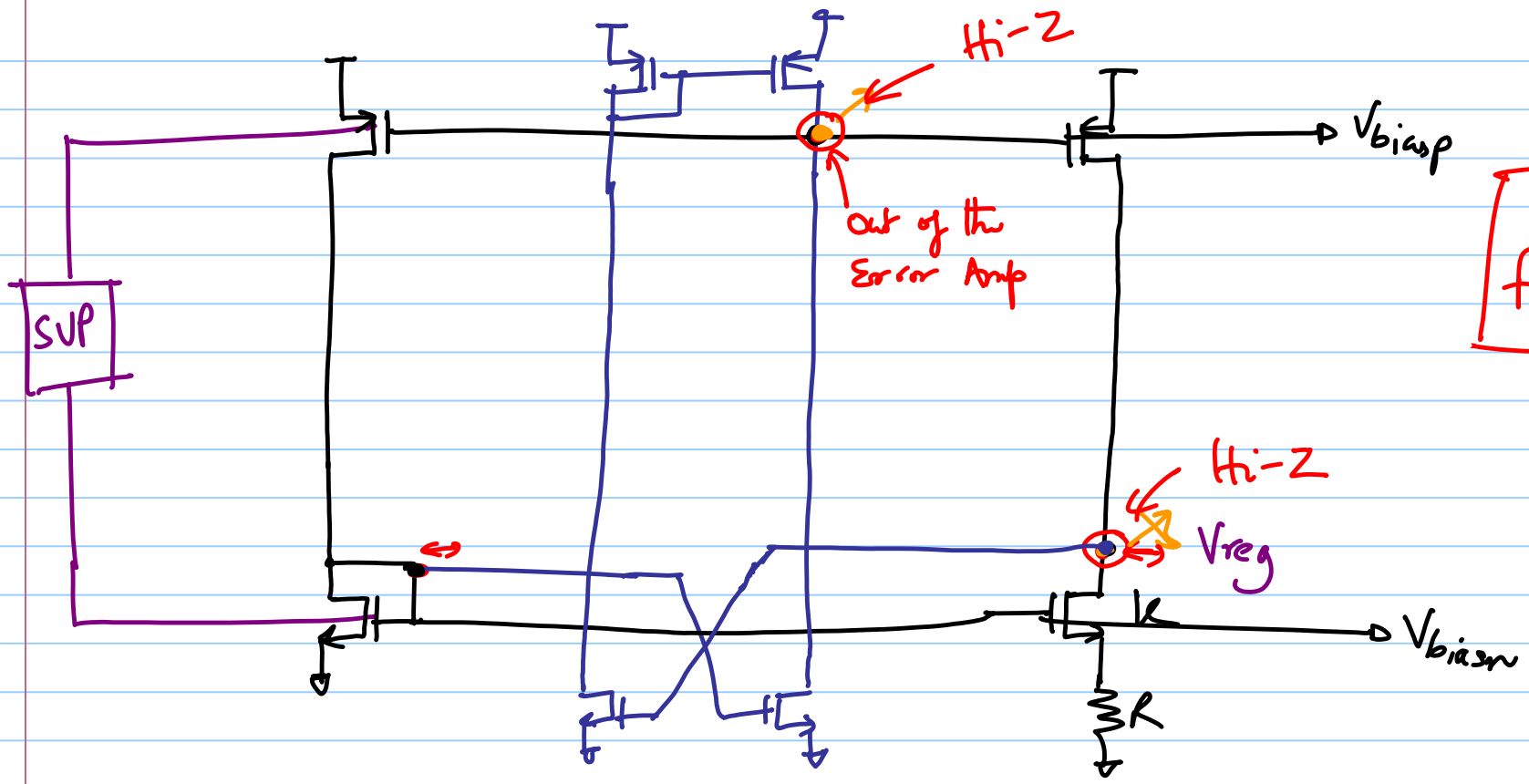
Think of



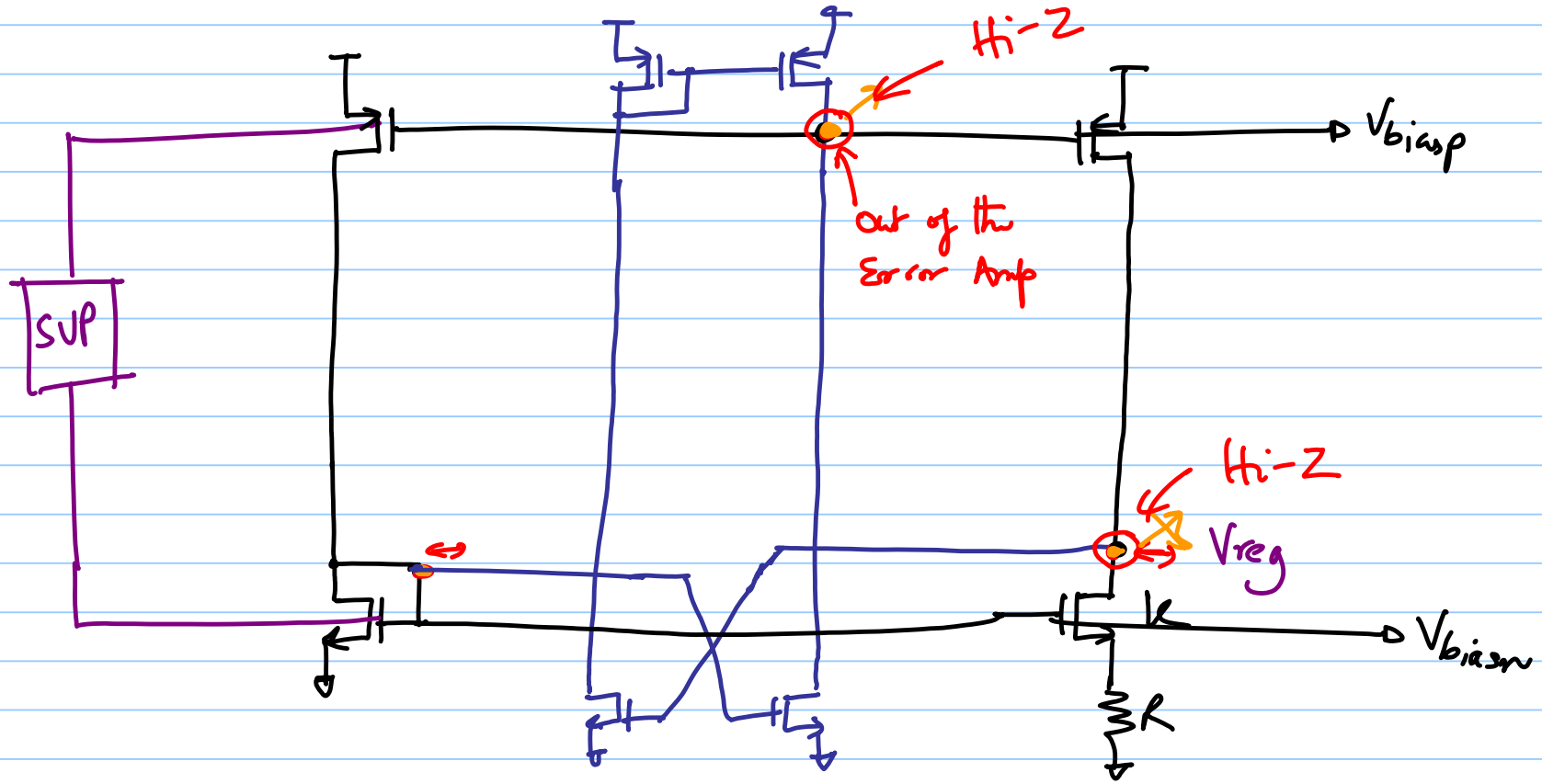

V_p
V_m


V_{out}
V_p
V_m


$V_{out} = A(V_p - V_m)$
$g_{mn}(r_{op} \| r_{on})$
V_p
V_m



CMOS
fig 20.23


Hi-Z
out of the Error Amp
V_{biasp}
SUP
Hi-Z
Vreg
V_{biasn}
R