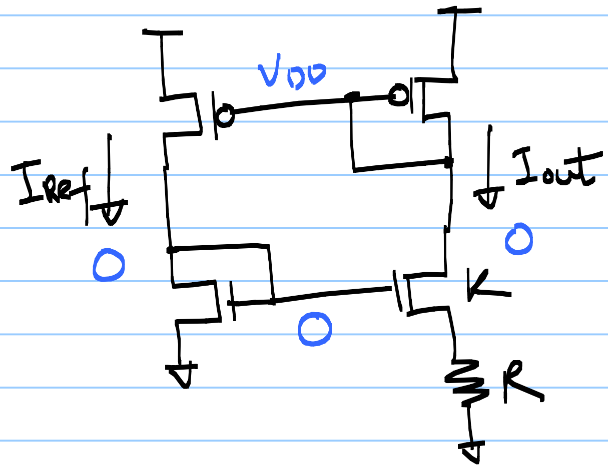
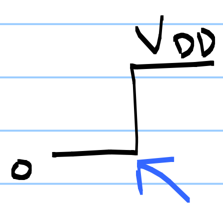
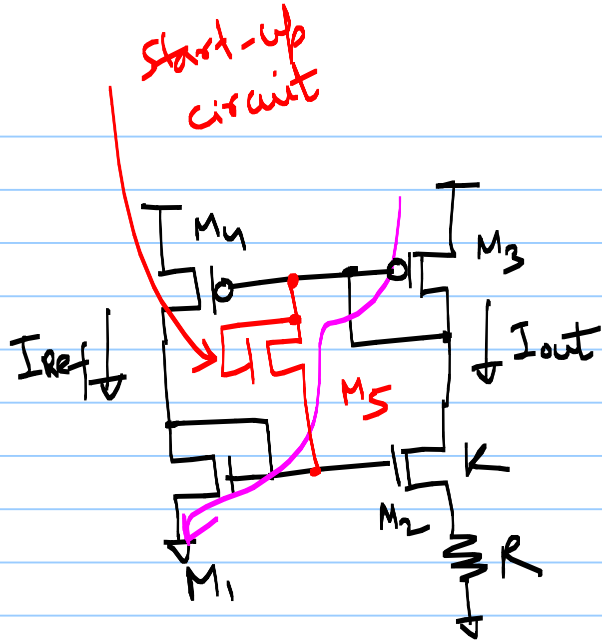
ECE 5411 – Lecture 8

Note Title 2/14/2011



$$I_{ref} = \begin{cases} 0 & \text{degenerate} \\ \dfrac{2}{KP_n\left(\frac{W}{L}\right)_1 R^2}\left(1 - \dfrac{1}{\sqrt{K}}\right)^2 & \leftarrow \text{desired current} \end{cases}$$





forces flow of current from
$M_3 \rightarrow M_1$
$\hookrightarrow$ turn M_2 & M_4 on

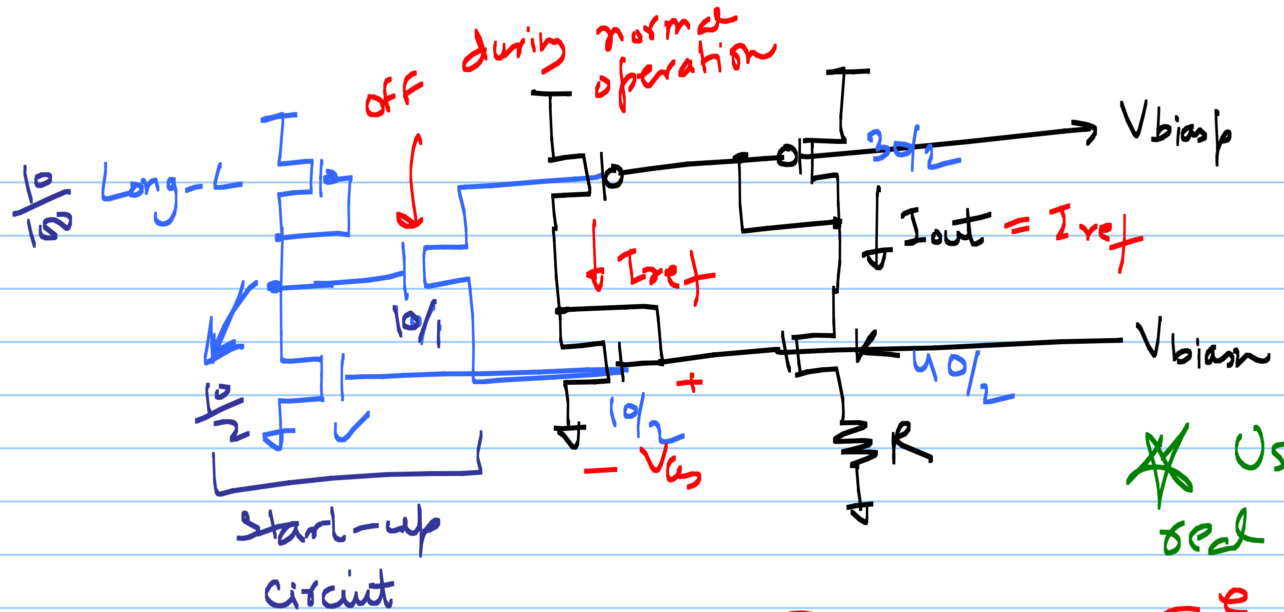
* But M_5 should be off during normal operation.

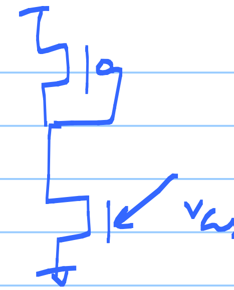
To turn 'ON' $\Rightarrow$ $V_{THN_1} + V_{THN_5} + V_{THN_3} < V_{DD}$

To turn 'OFF' $\Rightarrow$ $V_{DD} - (V_{GS_1} + V_{SG_3}) < V_{THN5}$

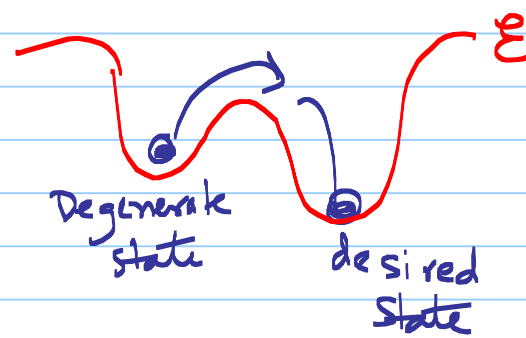
↳ $V_{GS1} + V_{THN5} + V_{SG3} > V_{DD}$

↳ very restrictive solution.





☆ Use Trims in real chips



* Design requires careful analysis & simulation

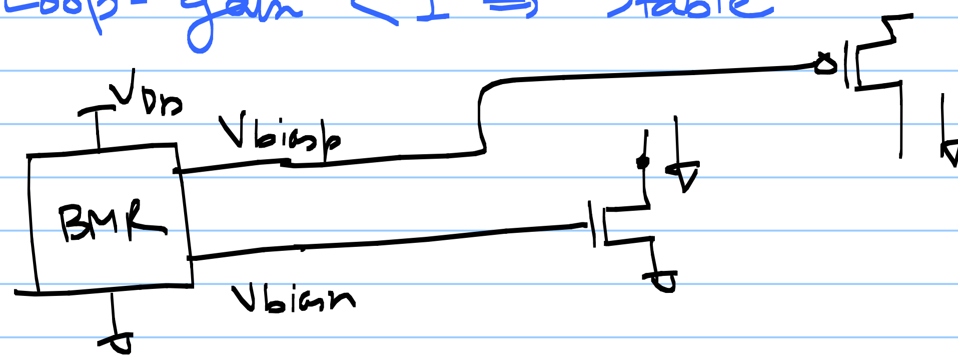
  ↳ ramp up supply $0 \rightarrow V_{DD}$ (DC sweep)

  ↳ transient sims for all corners.

* BMR is an example of a +ve feedback circuit

  Loop-gain $< 1 \Rightarrow$ Stable

Fig 20.16



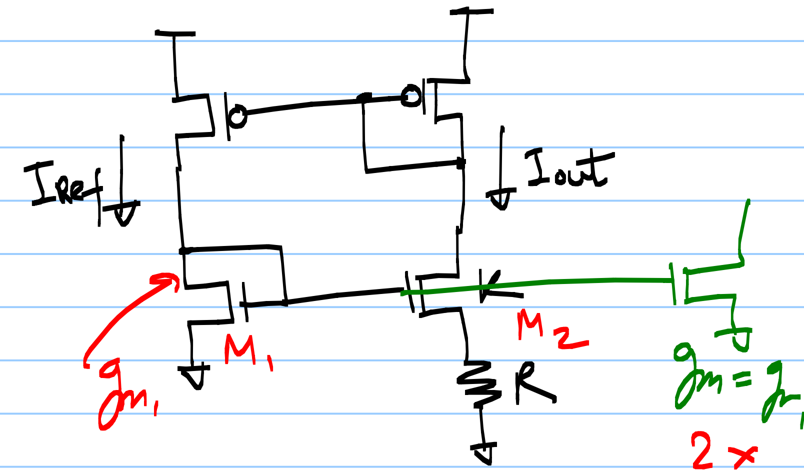
Minimum V_{DD} :

$$V_{DD\,min} = V_{SD_3,sat} + V_{GS_1} = \underline{\underline{1.3\,V}} \checkmark \text{ in } 1\mu m \text{ CMOS.}$$

$$I_{out} = I_{ref} = \frac{2}{KP_n \left(\frac{W}{L}\right)_1 R^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

$$V_{ov} = V_{GS} - V_{THN} = \frac{2}{KP_n \frac{W}{L} R} \left(1 - \frac{1}{\sqrt{K}}\right)$$

$$g_m \text{ of } M_1 = \sqrt{2 \beta I_{ref}}$$



$$= \sqrt{\cancel{2 k'_n \left(\frac{W}{L}\right)_1} \cdot \frac{2}{\cancel{k'_n \left(\frac{W}{L}\right)_1}} \cdot \frac{1}{R^2}\left(1-\frac{1}{\sqrt{K}}\right)^2}$$

@ $K=4$

$$\Rightarrow \quad g_{m1} = \frac{2}{R}\left(1-\frac{1}{\sqrt{K}}\right) = 1/R$$

↳ Example of constant-g_m biasing

$$g_m = \underset{2\times}{\beta}\left(\underbrace{V_{GS}-V_{THN}}\right)$$

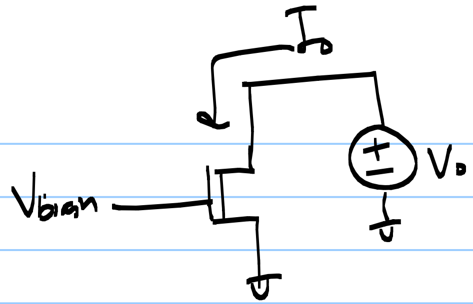
$$g_m \Rightarrow 2\times$$

Fig 20.18

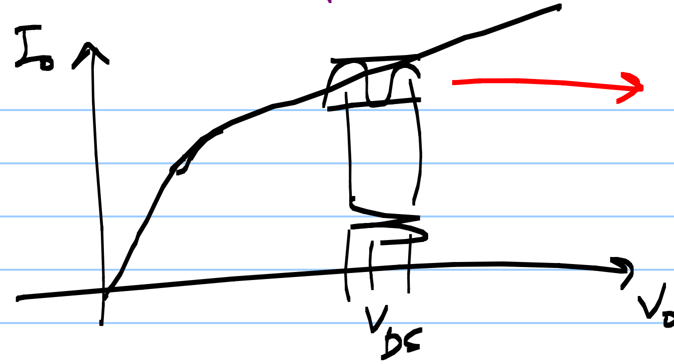
50nm CMOS → BMR design

$V_{DD} = 1V$

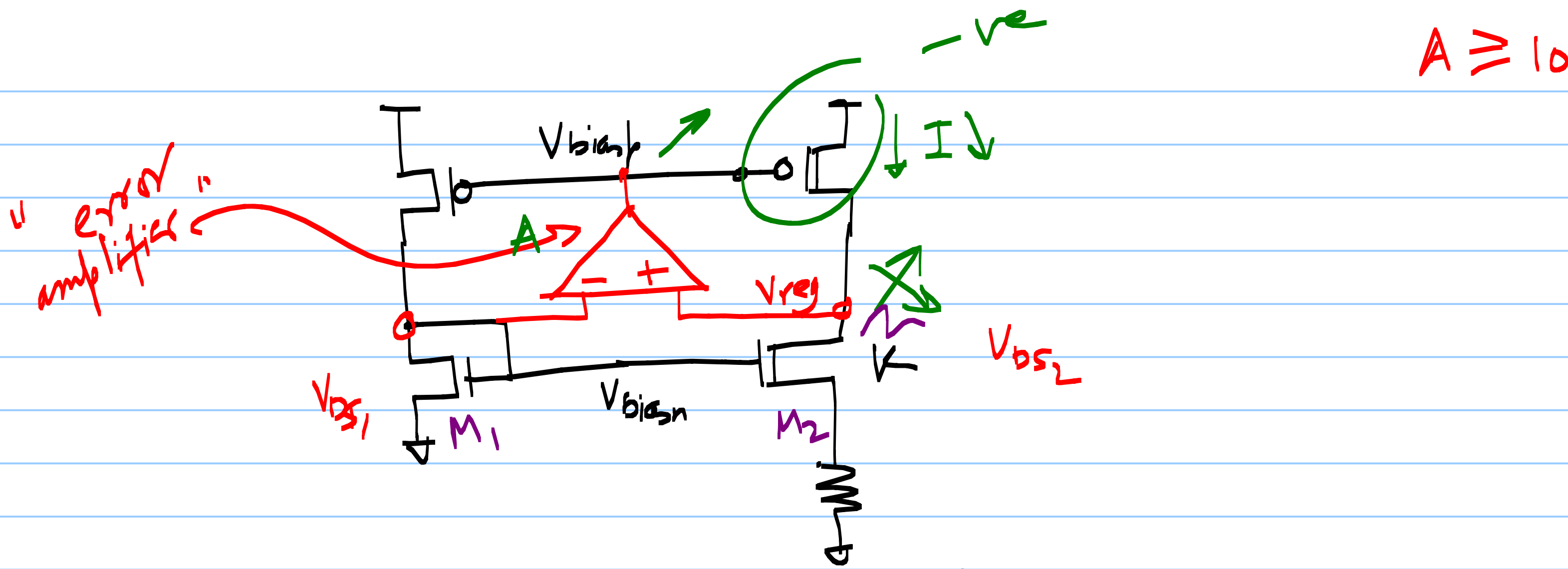
* Strong V_{DD}- sensitivity
* Matching of Iref & Iout is not good.
  - ↳ channel length modulation
    - ↳ larger current mismatch due to ΔV_{DS}



$\hookrightarrow$ lower 'r_o's



$\rightarrow$ lower 'r_o'



* Compare the NMOS drain voltages (Vbiasn & Vreg) and control the PMOS current to keep them equal.
  ↳ effectively increases the output resistance of M_2 (drain)

* If $V_{reg} > V_{bias n}$, $\Rightarrow V_{bias p} \uparrow$

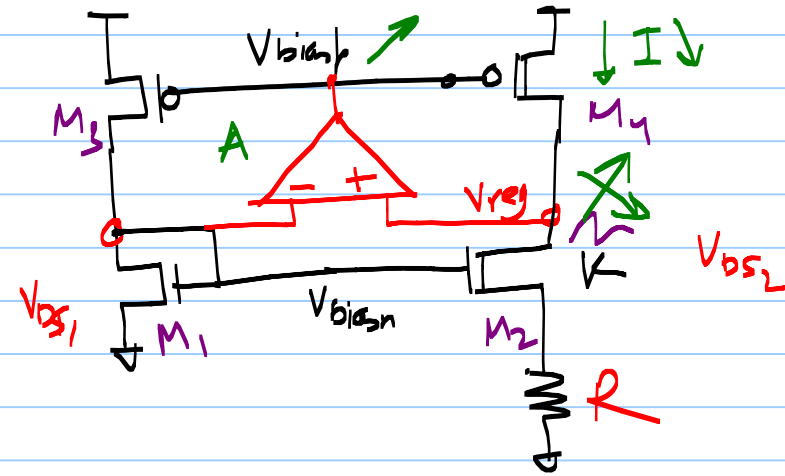
$\Rightarrow$ Current in $M_4 \downarrow$

$\Rightarrow V_{reg} \downarrow$

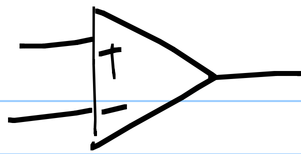
↳ Also gate of $M_3 \uparrow$

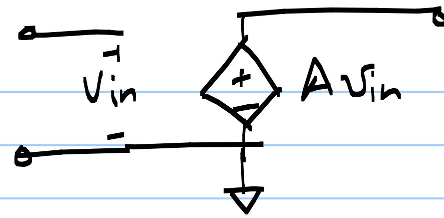
$\Rightarrow$ lower current sourced from M_3

↳ $V_{bias n}$ drops!

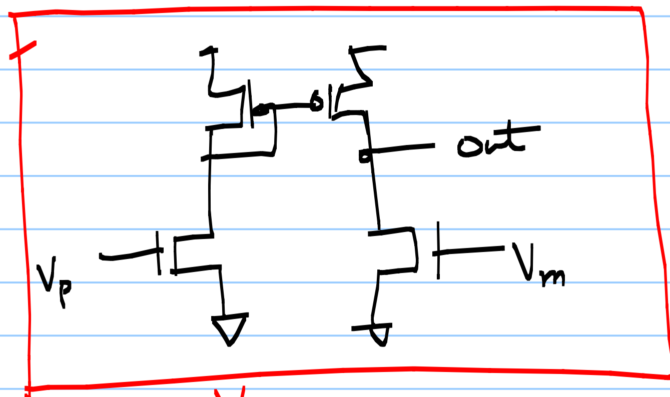


VCVS





$A = 10 - 100$



Error Amplifier

V_{cn}

no precise bias current required.
(self-biased circuit)