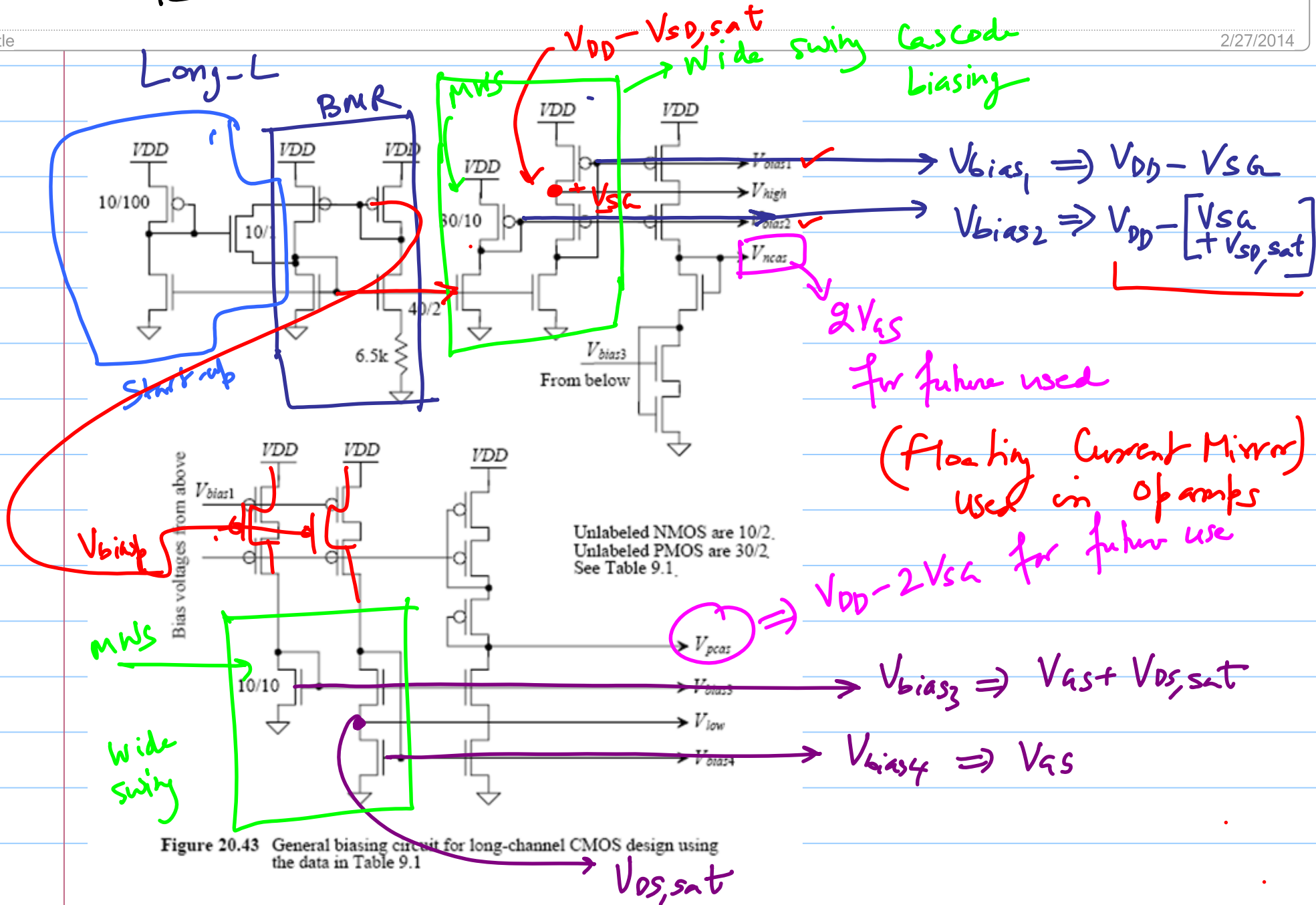
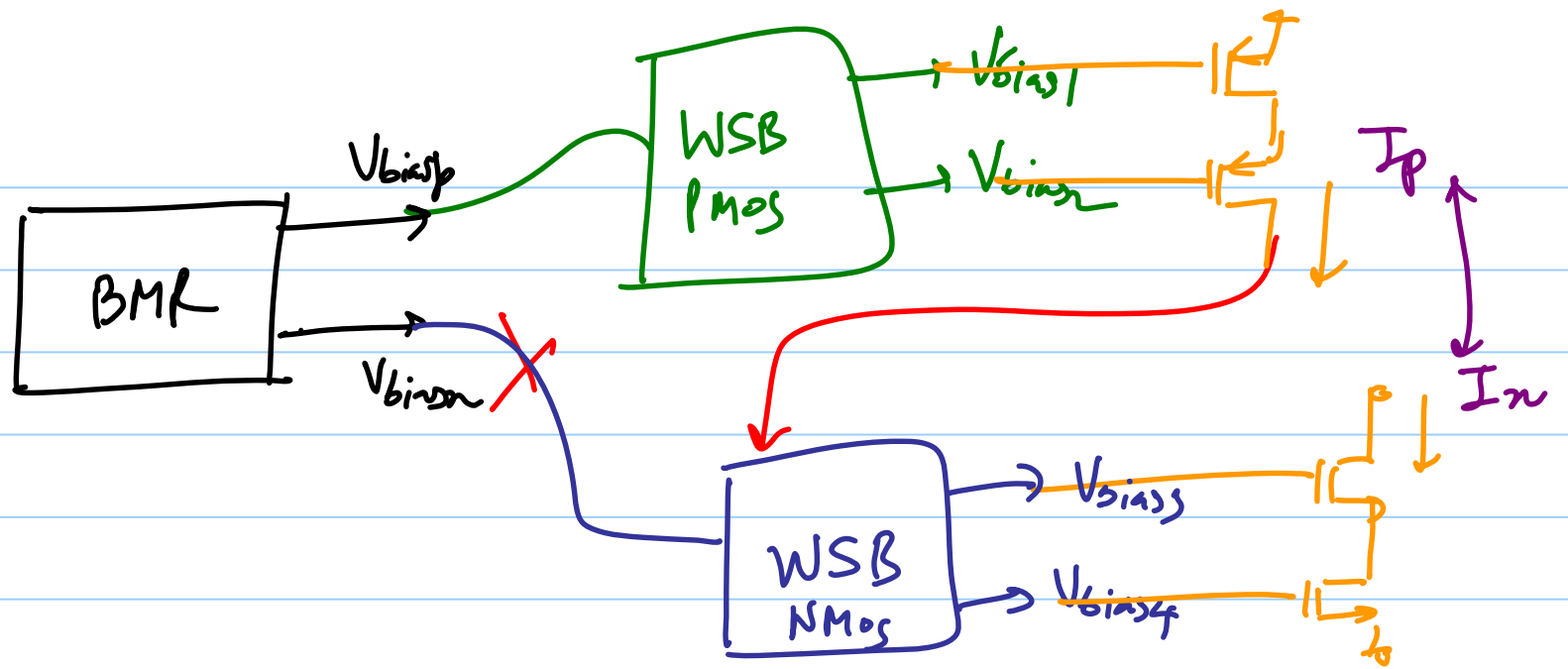
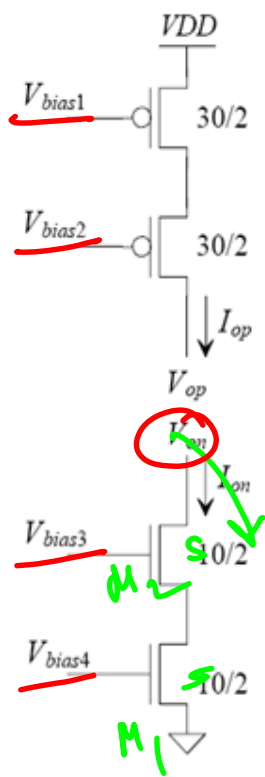


ECE 511 - Lecture 12





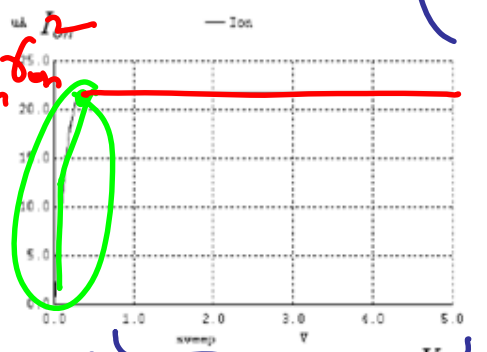
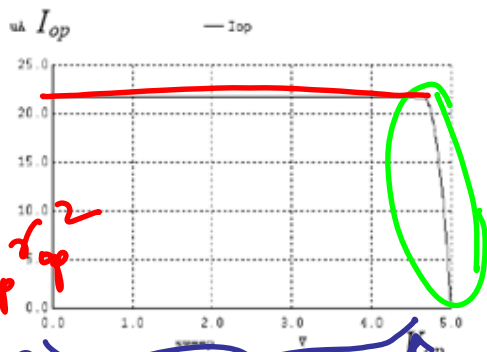
Minimizes systematic offset between the currents I_p & I_n



$g_{m_p} \cdot I_{op}$



$g_{m_n} \cdot I_{on}$

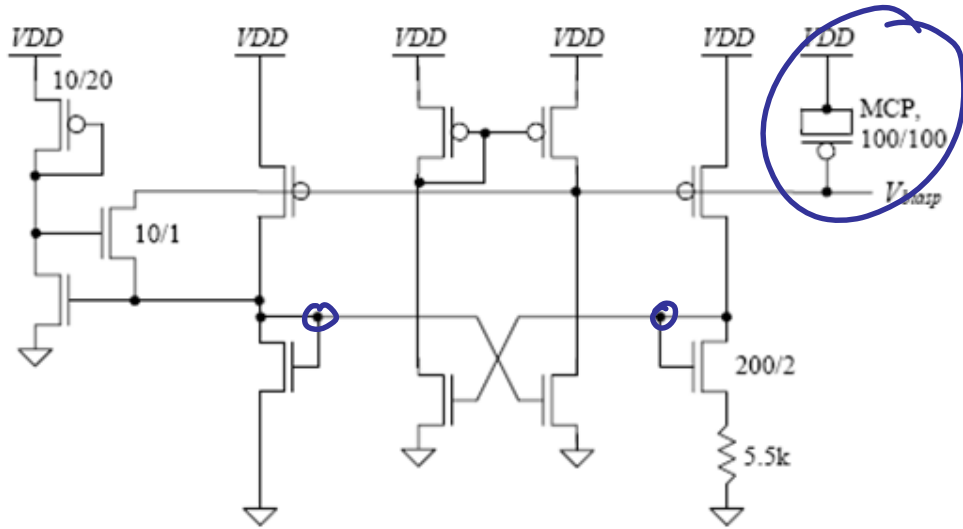


$V_{op} = \{ 2V_{DS,sat} \}$

Bias voltages come from Fig. 20.43 (long-channel parameters in Table 9.1).

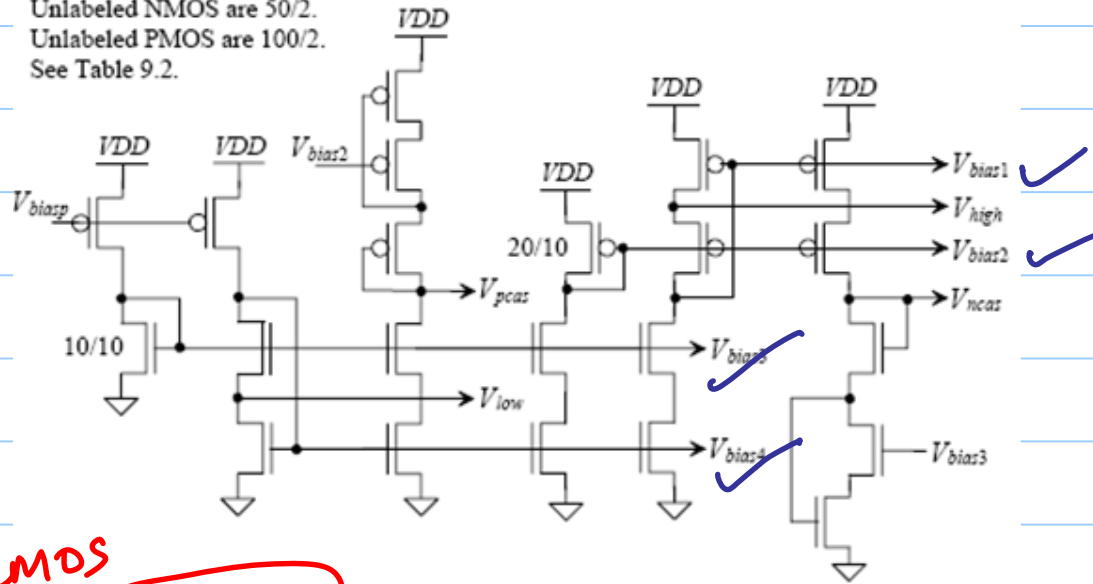
Figure 20.44 How cascode currents are biased and how they operate.

Short-L biasing



compensation for stability

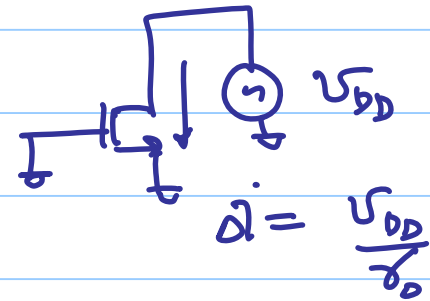
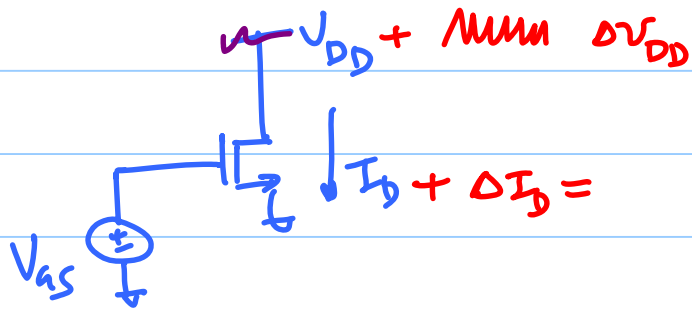
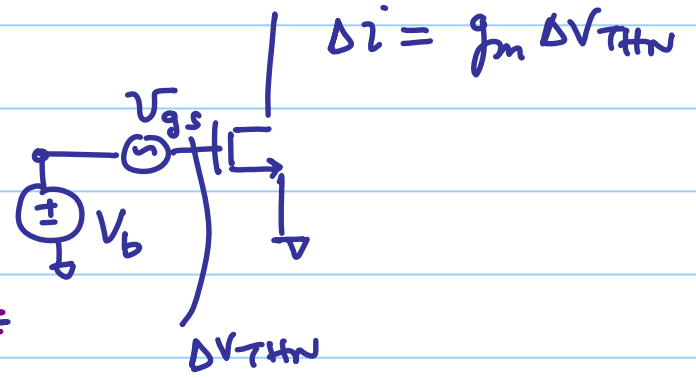
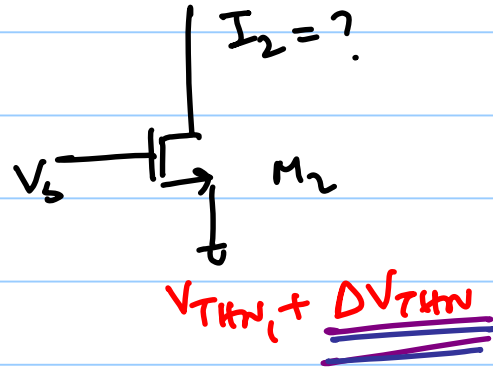
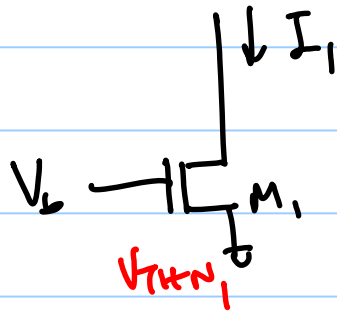
Unlabeled NMOS are 50/2.
Unlabeled PMOS are 100/2.
See Table 9.2.



CMOS
Book

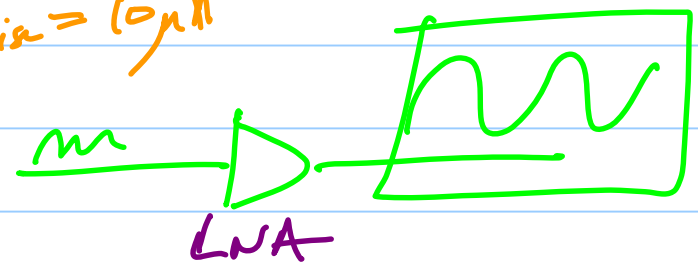
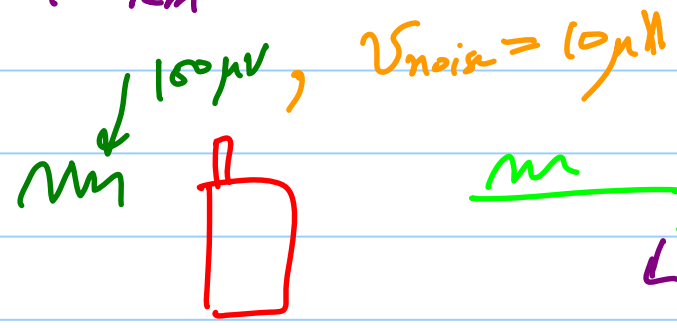
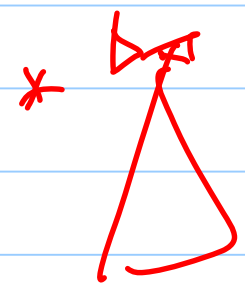
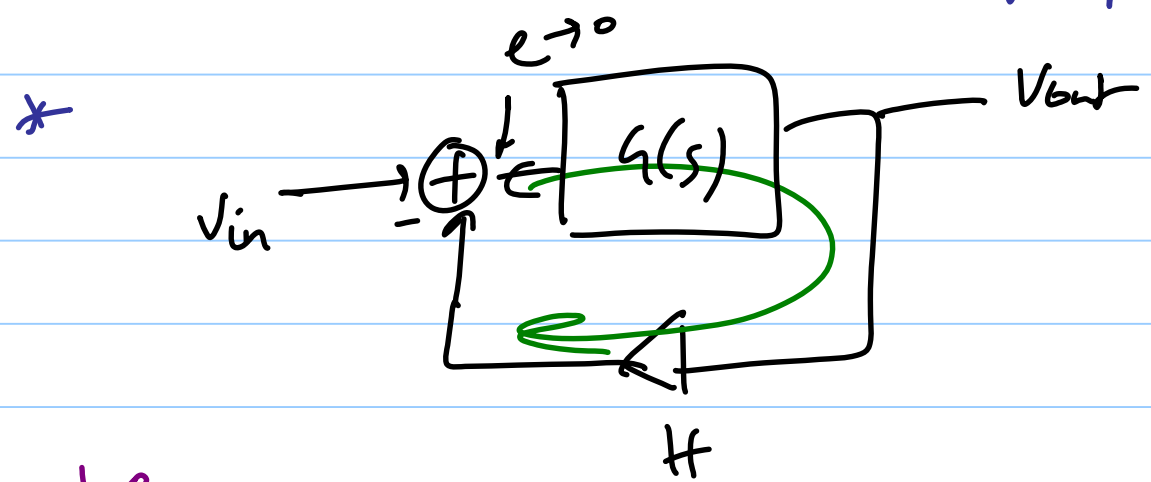
Figure 20.47 General biasing circuit for short-channel design using the data in Table 9.2.

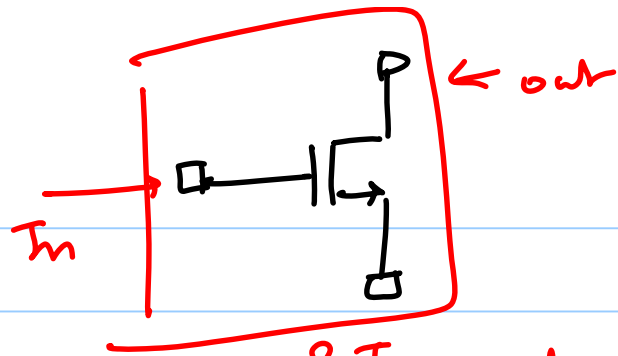
$$I_2 = I_1 - g_m |\Delta V_{THN}|$$



Single Stage Amplifiers

* Signal processing → fundamental building (Opamp)

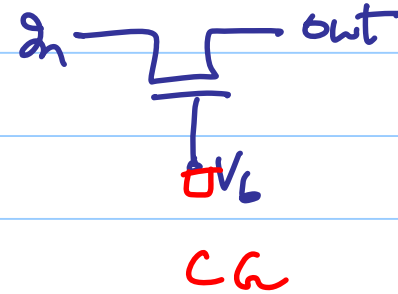
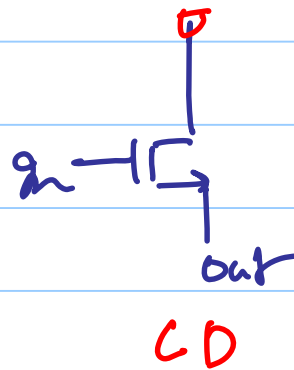
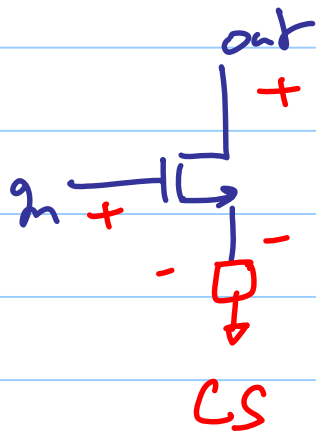




3 Terminals
2-port

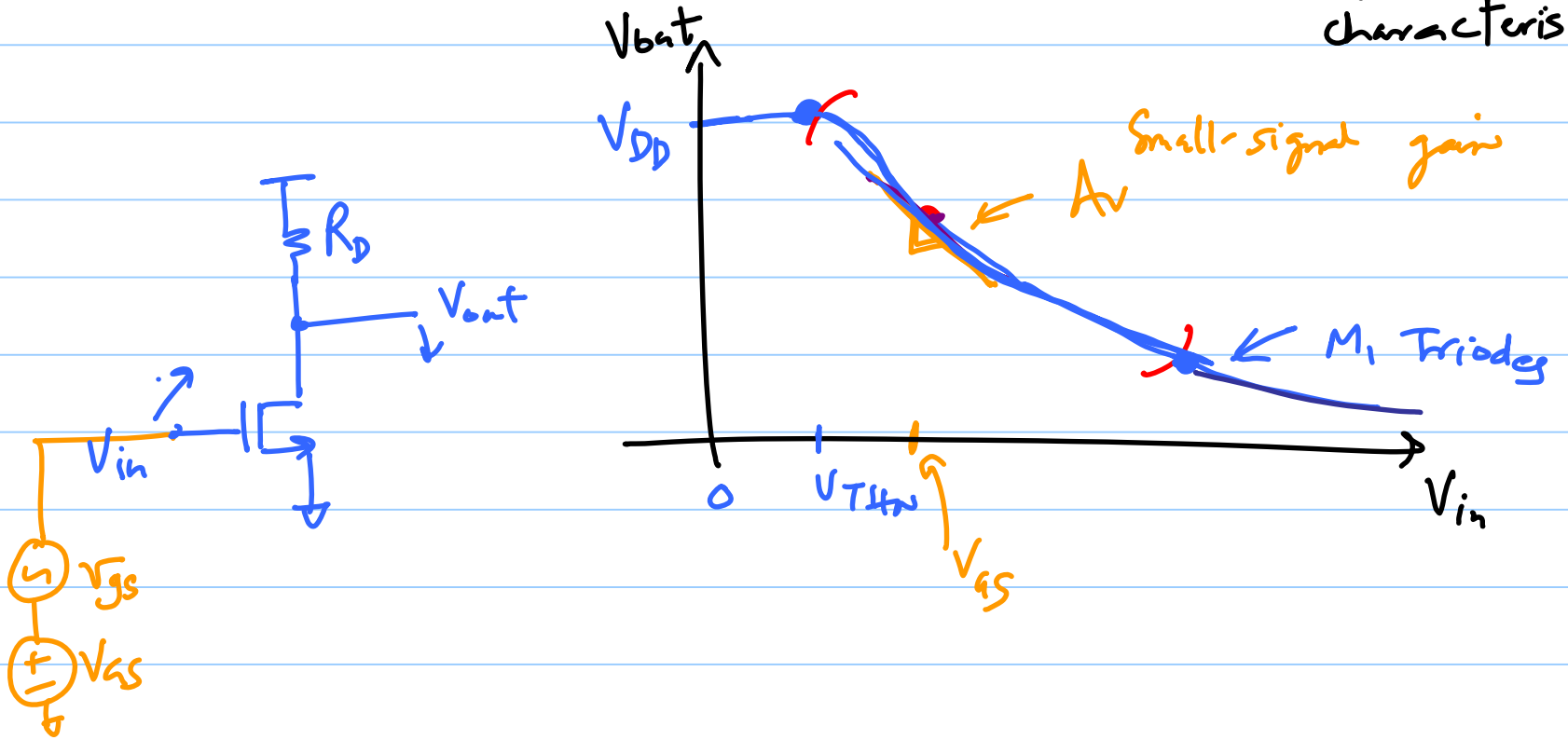
Controlled source
↳ signal gain

$$3 \times \frac{3.2}{1.2} = 3$$

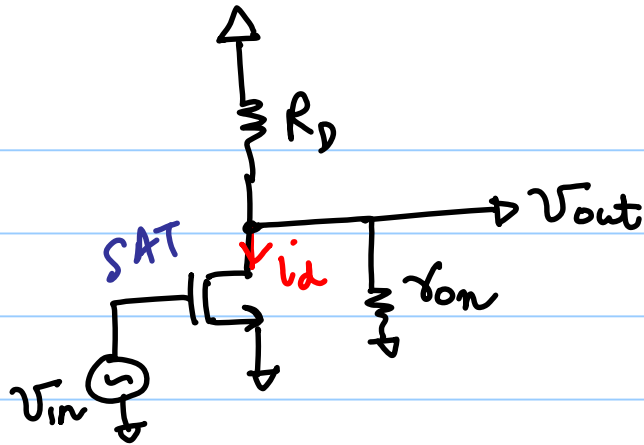


Common Source Stage

Large signal characteristics



AC

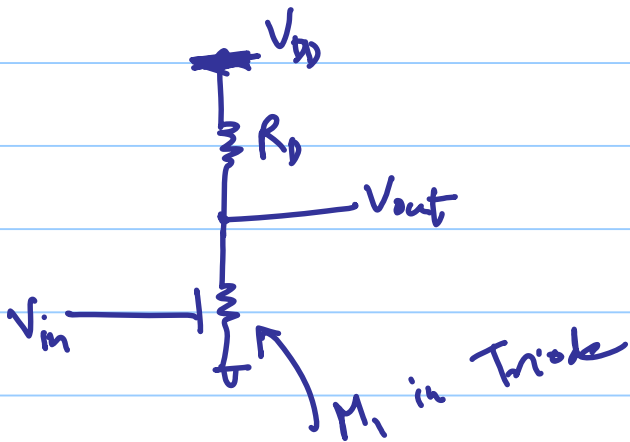


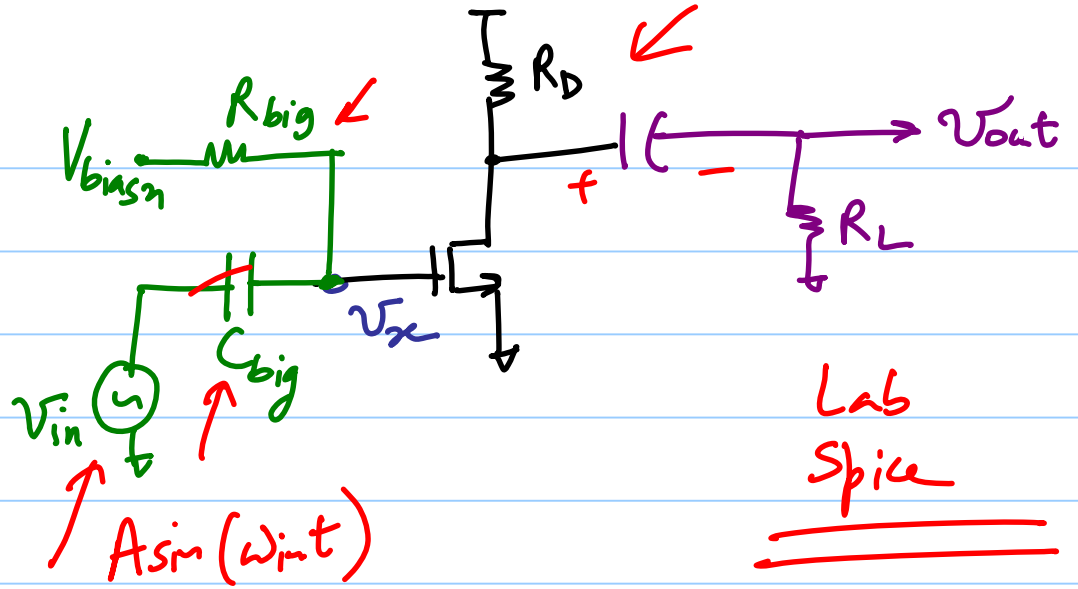
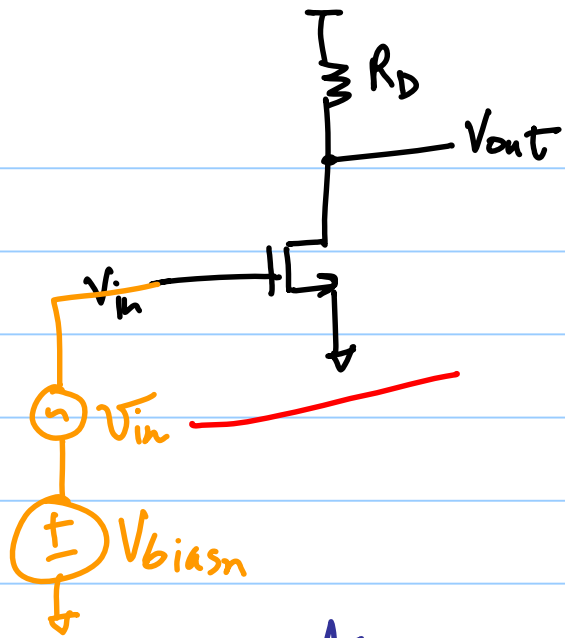
$$v_{out} = -i_d (R_D \parallel r_{on}) \\ = -g_m v_{in} (R_D \parallel r_{on})$$

$$A_v = \frac{v_{out}}{v_{in}} = -g_m (R_D \parallel r_{on})$$

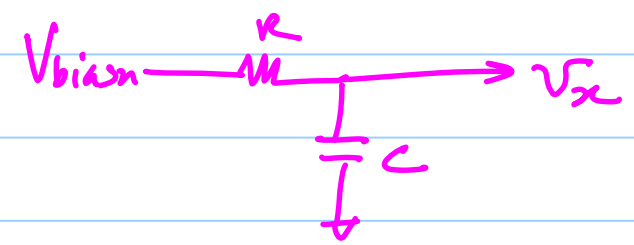
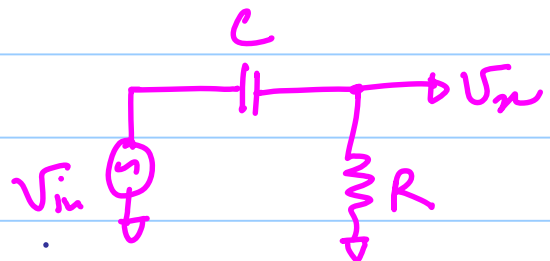
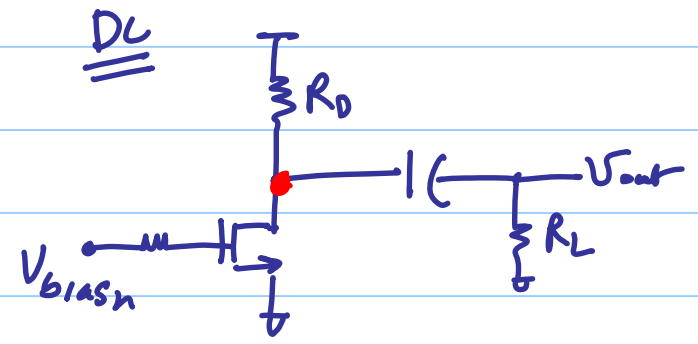
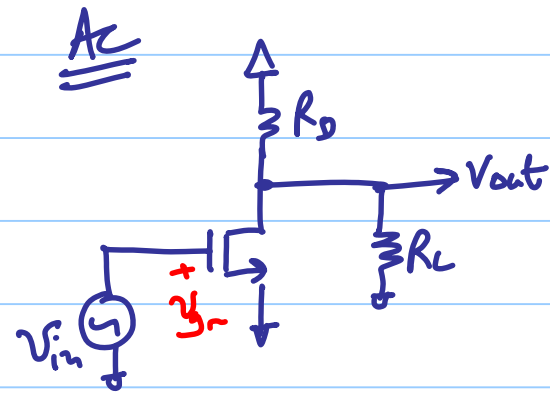
$$\approx -g_m R_D \text{ for } r_{on} \gg R_D$$

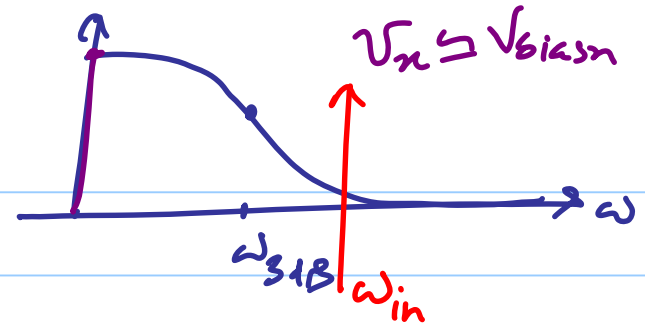
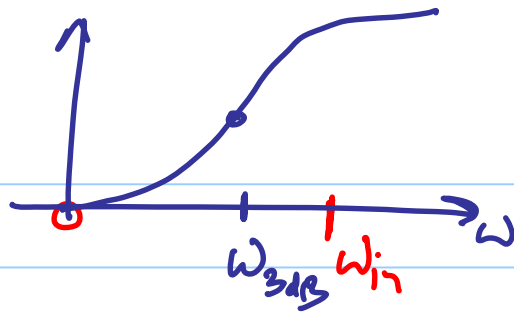
g_m depends on V_{ov}





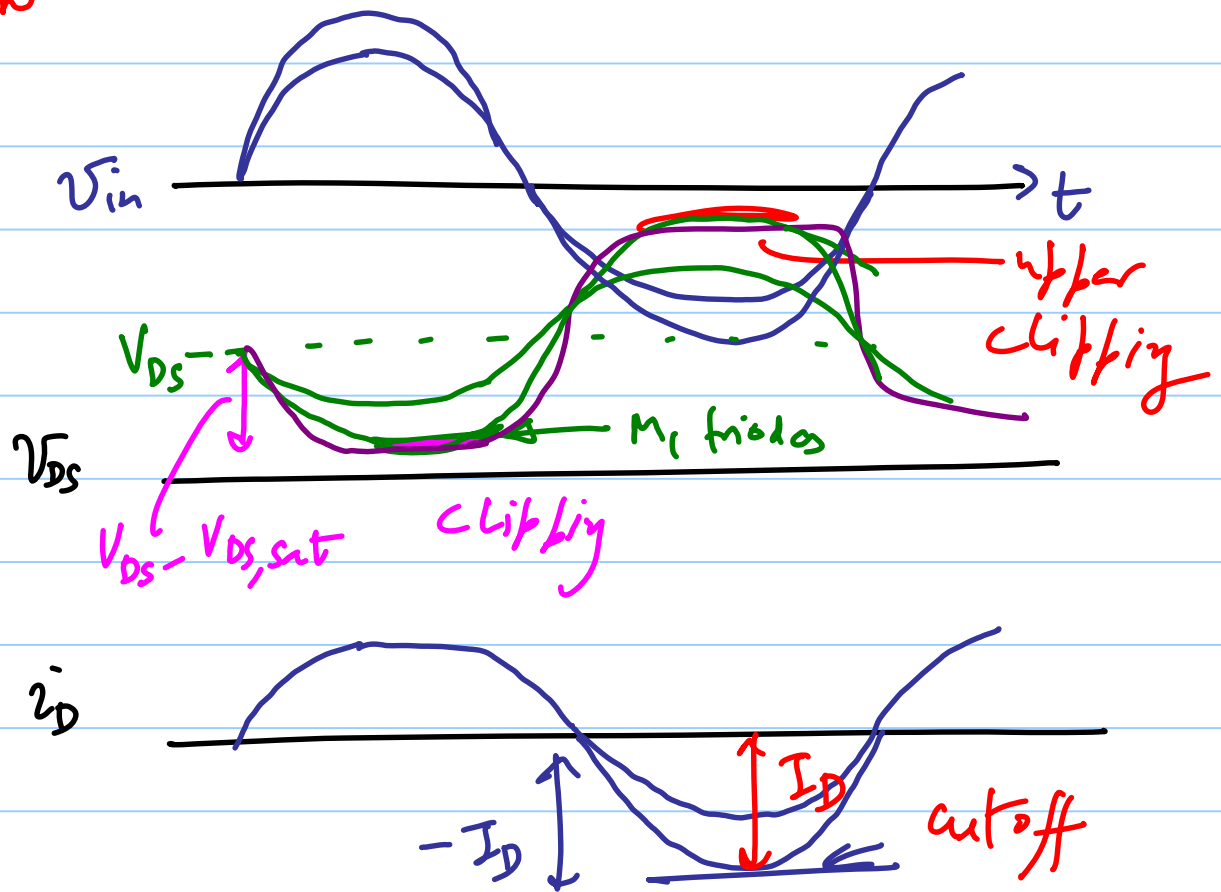
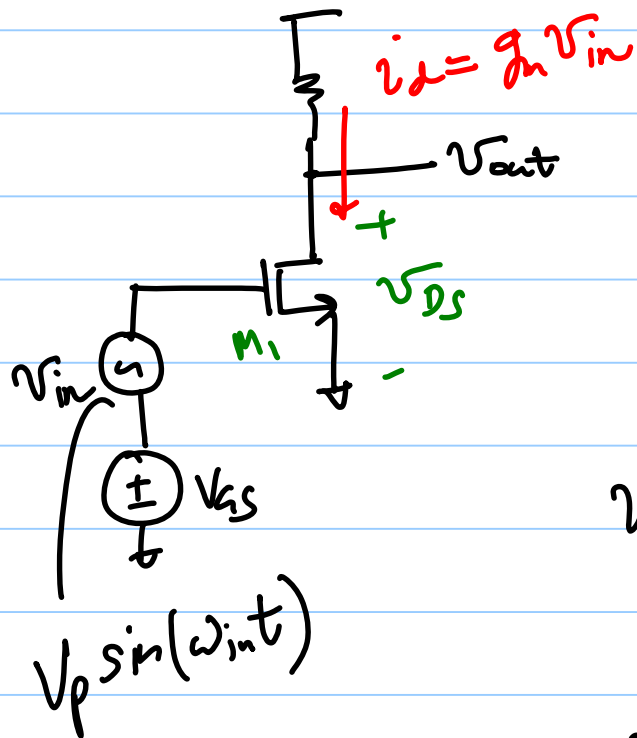
Asin(ωt)





$$\omega_{3dB} \ll \omega_{in}$$

$$\Rightarrow \frac{1}{R_{bij} C_{bij}} \leq \frac{\omega_{in}}{10}$$



true input cycle

$$V_{p,max,i} = \frac{(V_{DS} - V_{DS,sat})}{A_v}$$

Assuming
Linear device

-ve input cycle

$$V_{p,max_2} = \frac{I_D}{I_m}$$

$$i_L = -I_D \Rightarrow i_D = 0$$

max input amplitude
without clipping

$$\min \{ V_{p,max_1}, V_{p,max_2} \}$$

"Swing Limits"