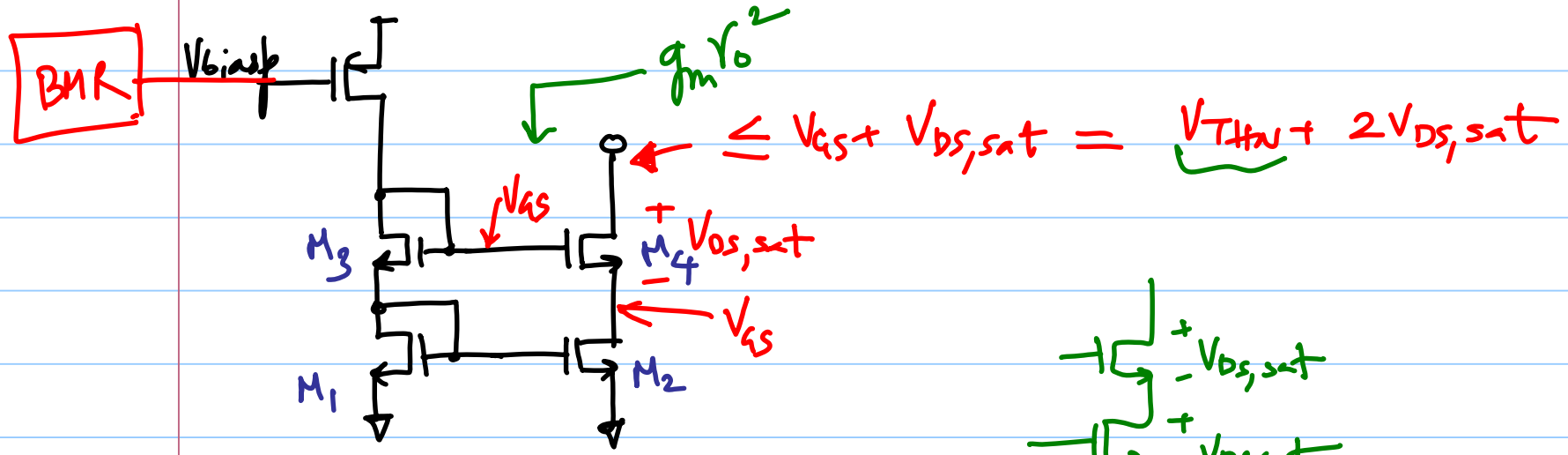
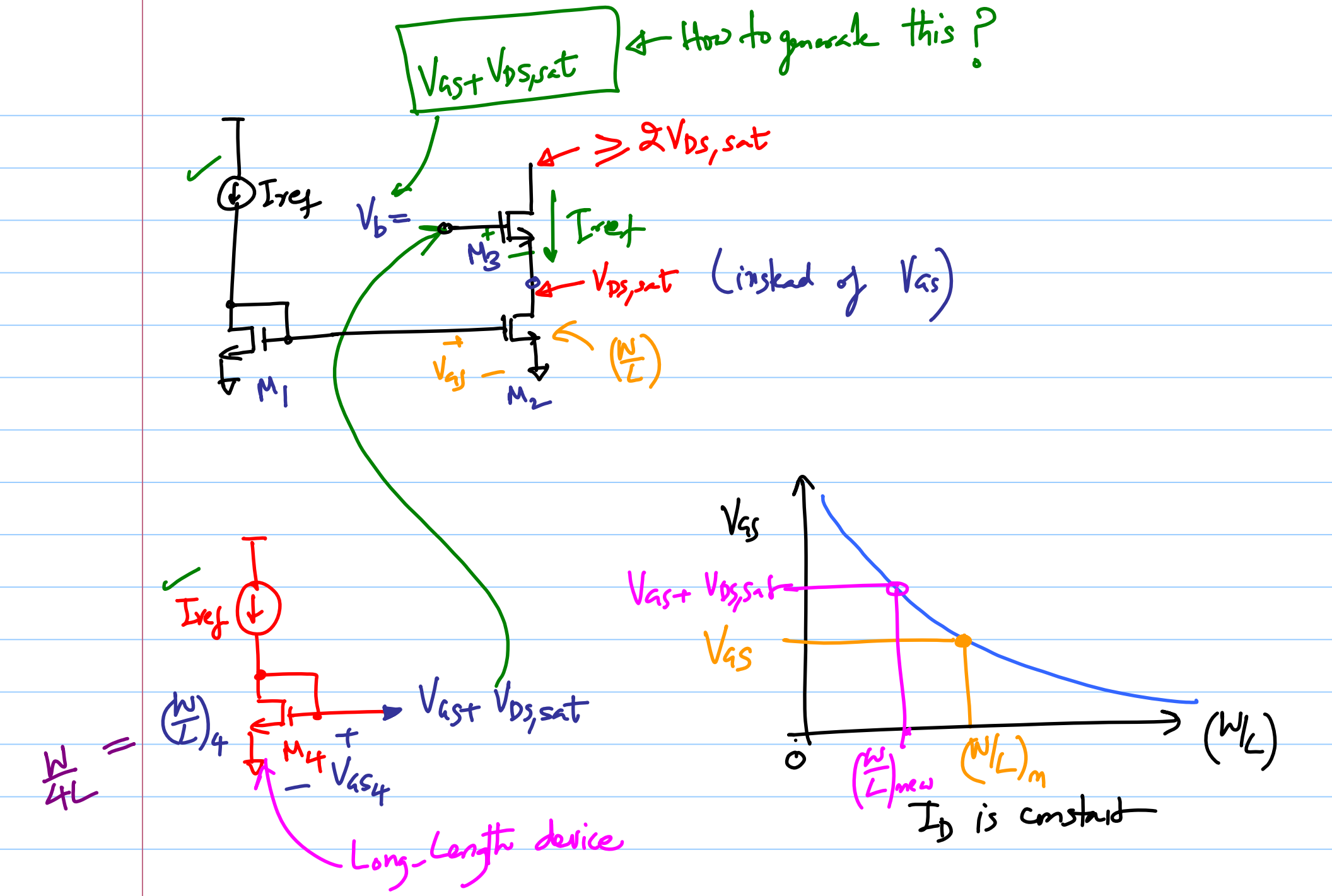
ECE 511 – Lecture 10

Note Title 2/20/2014



* Wide Swing Biasing schemes


$V_{GS}+V_{DS,sat}$
How to generate this ?
I_{ref}
$V_b =$
M_3
$\geq 2V_{DS,sat}$
I_{ref}
$V_{DS,sat}$ (instead of V_{GS})
M_1
V_{GS}
M_2
$\left(\frac{W}{L}\right)$
I_{ref}
$\left(\frac{W}{L}\right)_4$
$V_{GS}+V_{DS,sat}$
M_4
V_{GS4}
$\frac{W}{4L} =$
Long-Length device
V_{GS}
$V_{GS}+V_{DS,sat}$
V_{GS}
$\left(\frac{W}{L}\right)_{new}$
$\left(W/L\right)_n$
W/L
I_D is constant

$$V_{DS,sat} = V_{GS} - V_{THN}$$
$$= \sqrt{\frac{2I_D}{\beta}} + V_{THN} - V_{THN}$$

$$V_{GS_4} = 2(V_{DS,sat}) + V_{THN} = \sqrt{\frac{2I_{ref}}{\beta_4}} + V_{THN}$$

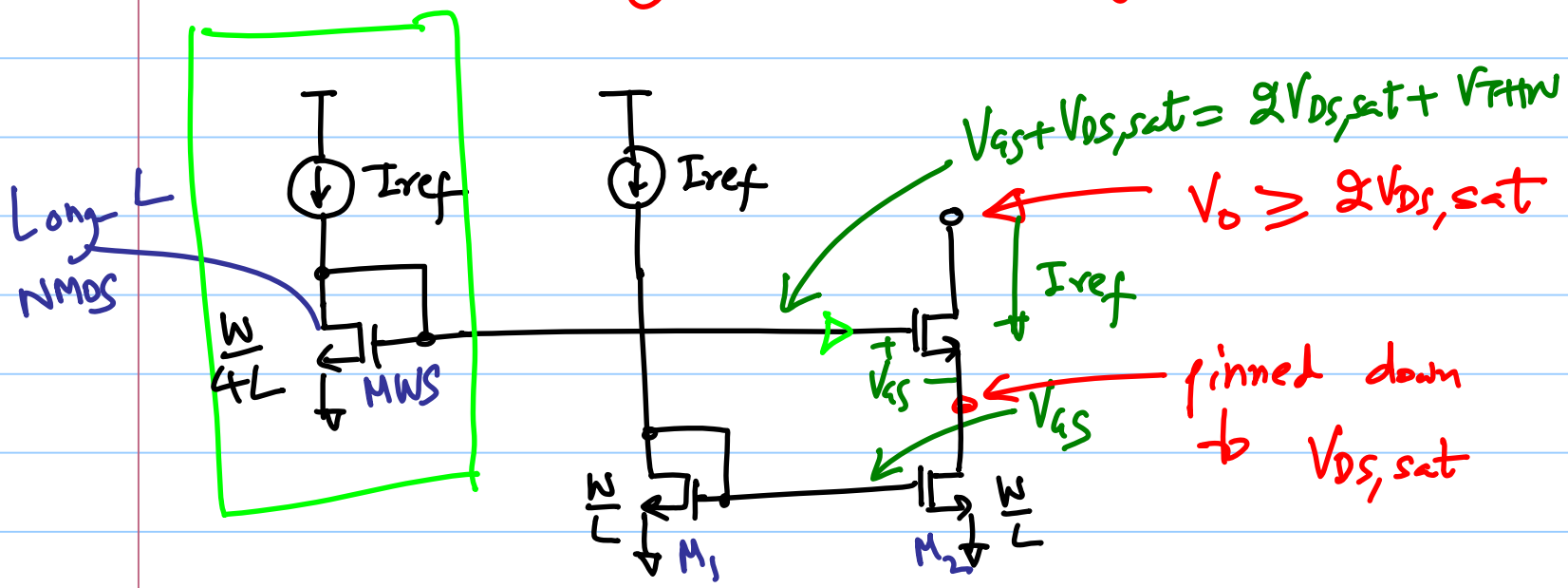
$$\sqrt{\frac{2I_{ref}}{\beta_2}}$$

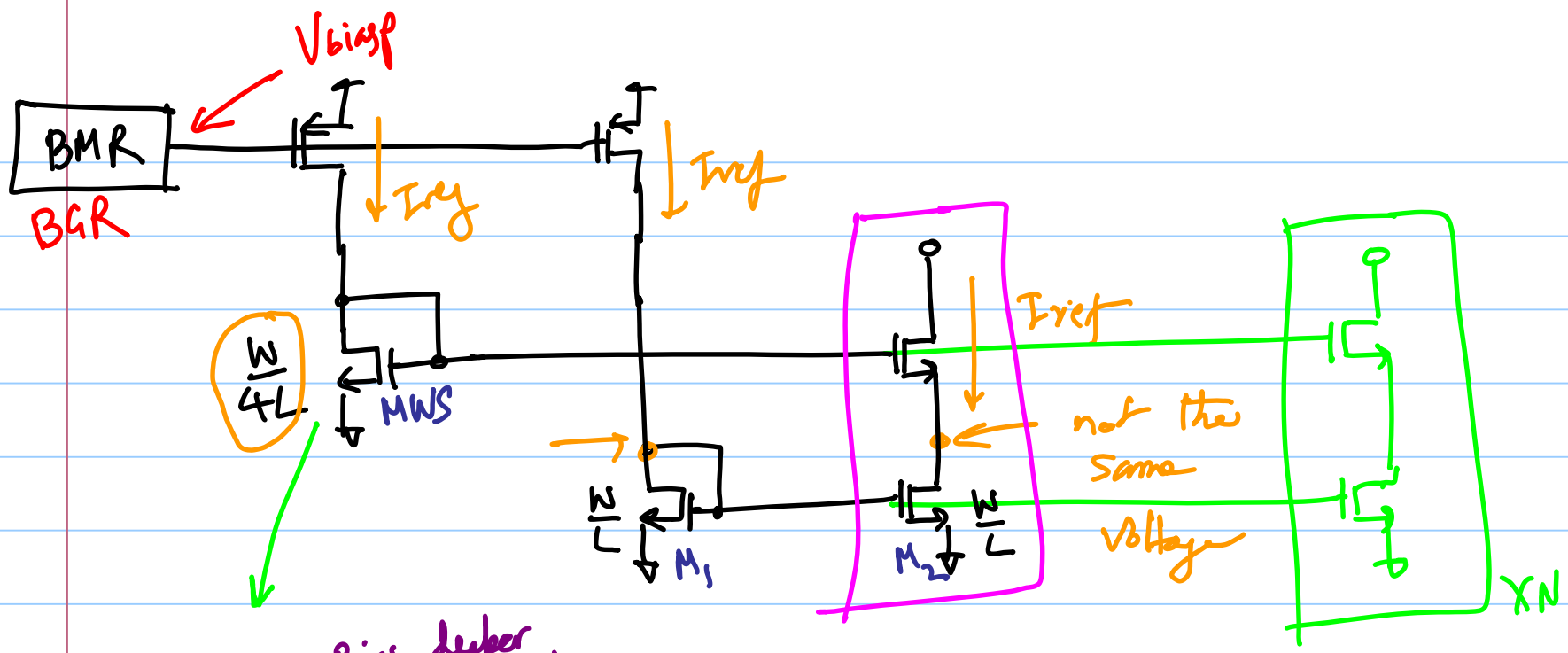
$$2\sqrt{\frac{2I_{ref}}{\beta_2}} = \sqrt{\frac{2I_{ref}}{\beta_4}}$$

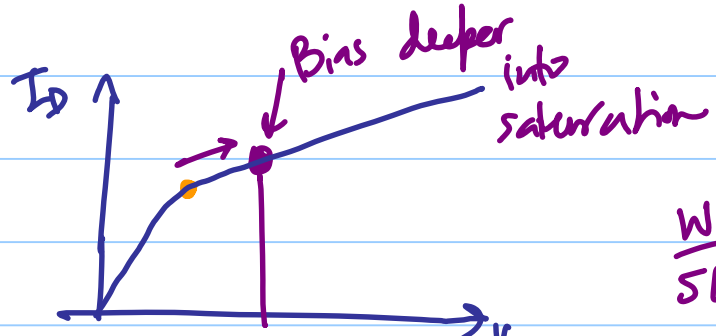
$$\beta_4 = \frac{\beta_2}{4}$$

$$\left(\frac{W}{L}\right)_4 = \frac{1}{4}\left(\frac{W}{L}\right)_2$$

Wide Swing Cascode Biasing

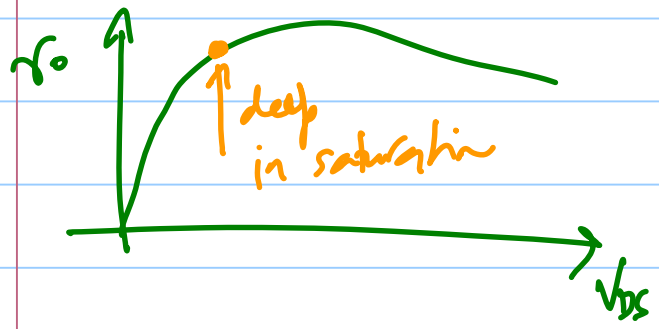




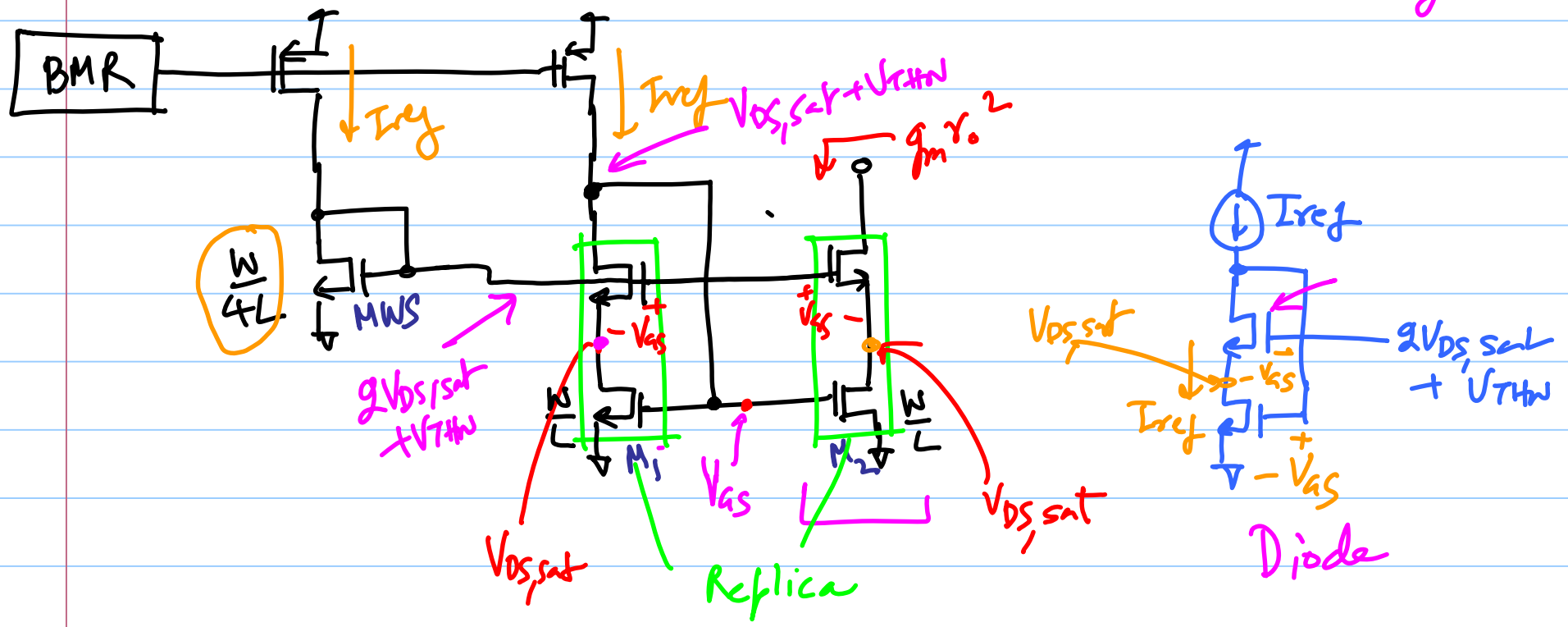


$\frac{W}{5L}$

50nm → $\frac{W}{25L}$ ← short-channel design

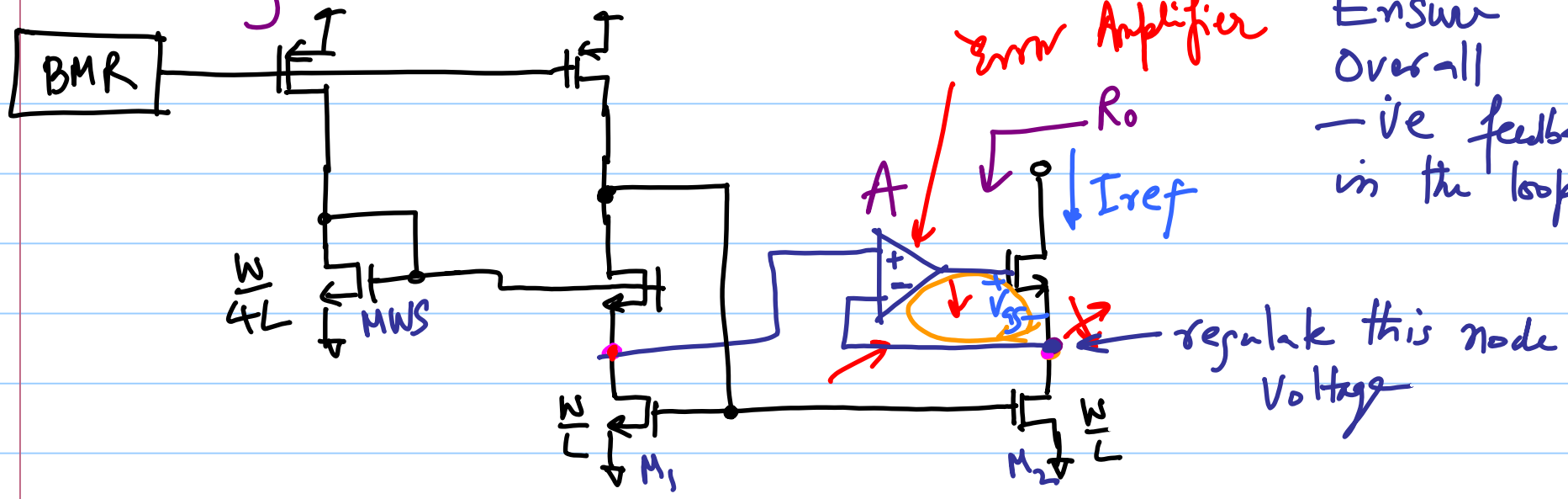


"Replica Biasing"

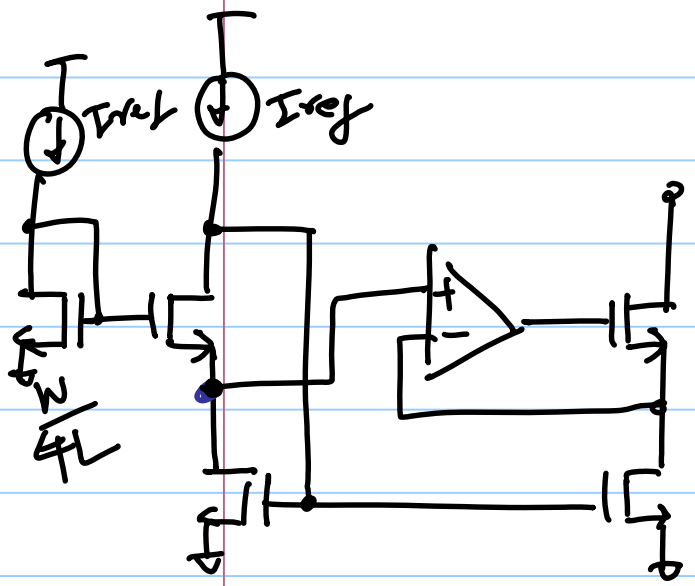


* Look at Sims from CMOS Chap 20

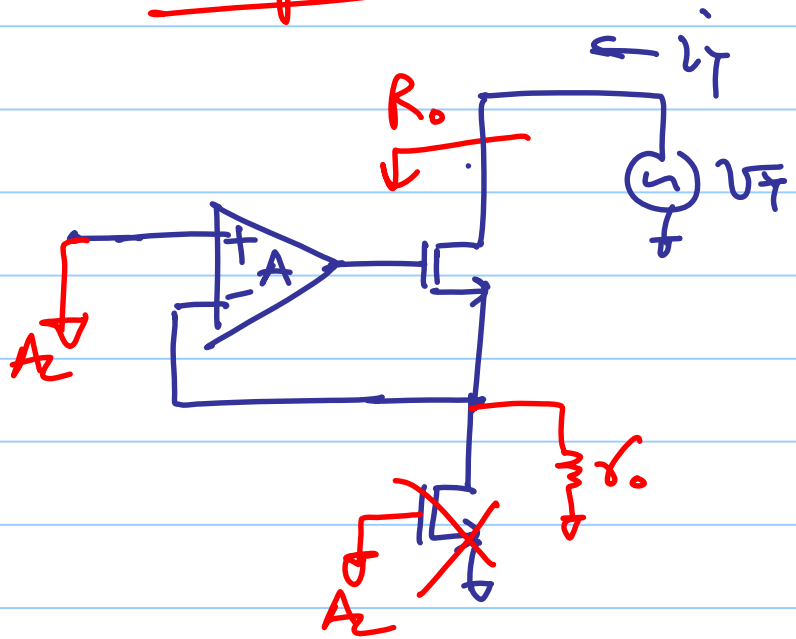
Regulated Drain Current Mirror

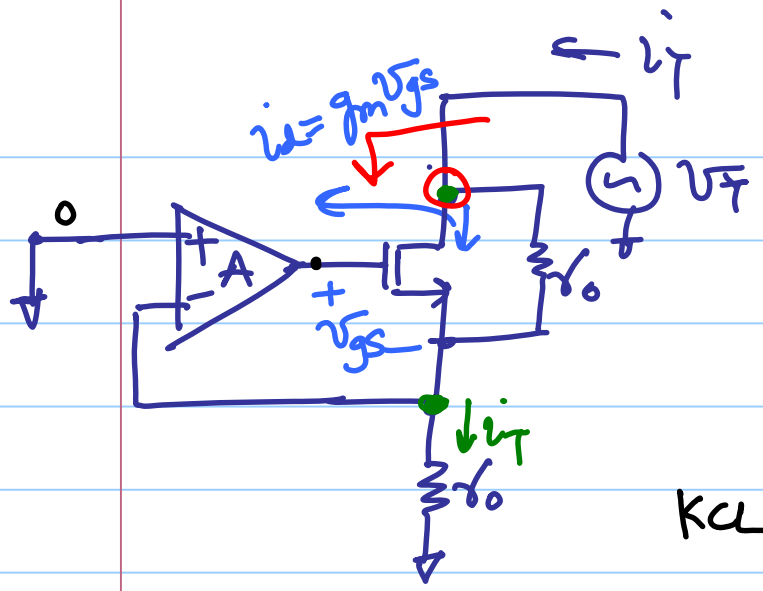


Ensure Overall -ve feedback in the loop



Az picture





KVL

$$v_{gs} = A(0 - i_T r_o) - i_T r_o$$

$$v_{gs} = -(A+1) i_T r_o \longrightarrow (1)$$

KCL at the output node

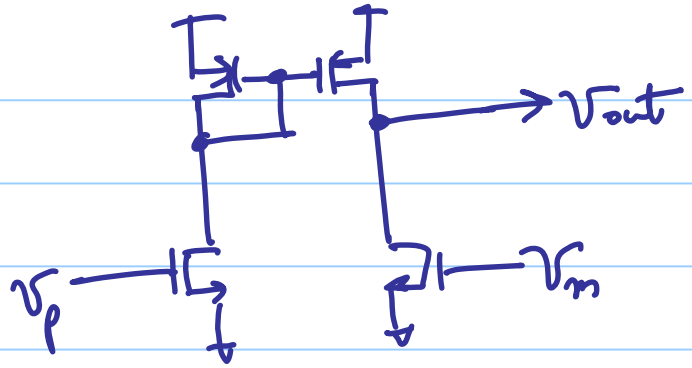
$$i_T - \underbrace{i_d}_{g_m v_{gs}} - \underbrace{\frac{(v_T - i_T r_o)}{r_o}}_{i_{r_o}} = 0$$

$$\Rightarrow \quad i_T + g_m r_o (A+1) v_T - \frac{v_T}{r_o} + i_T = 0$$

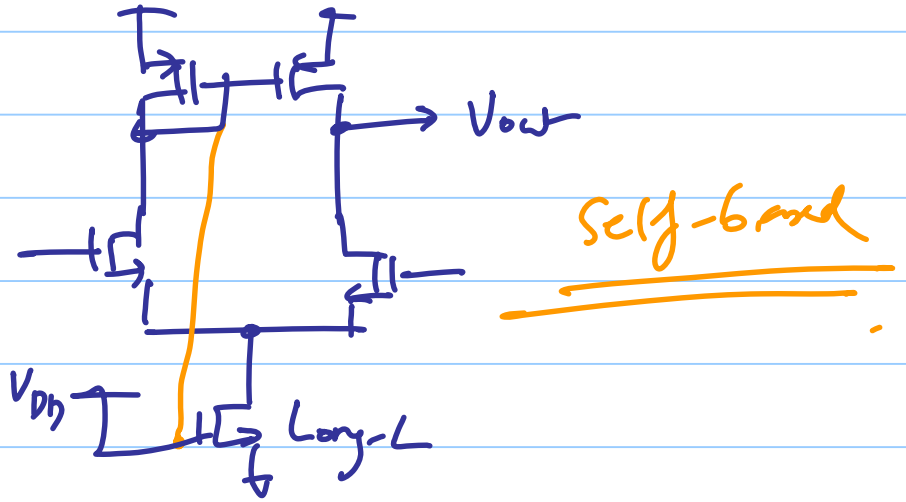
$$\Rightarrow \quad \frac{v_T}{r_o} = i_T (2 + g_m r_o (A+1))$$

for $|A| >> 1$

$$R_o = \frac{v_T}{i_T} = g_m r_o^2 (A+1) + 2 r_o \simeq \boxed{g_m r_o^2 \cdot A}$$



Self biased
Error Amplifier



Self-biased