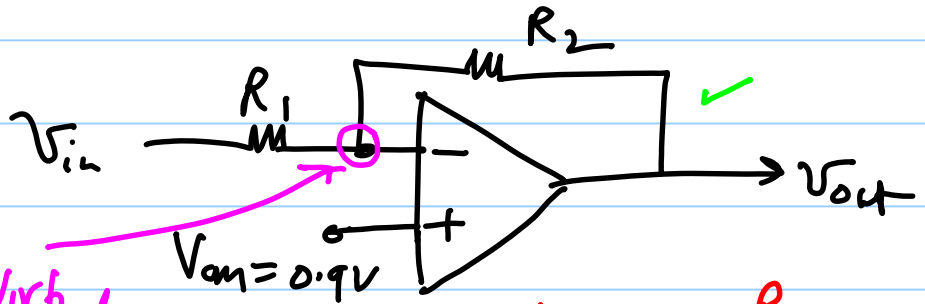
Project Help Session

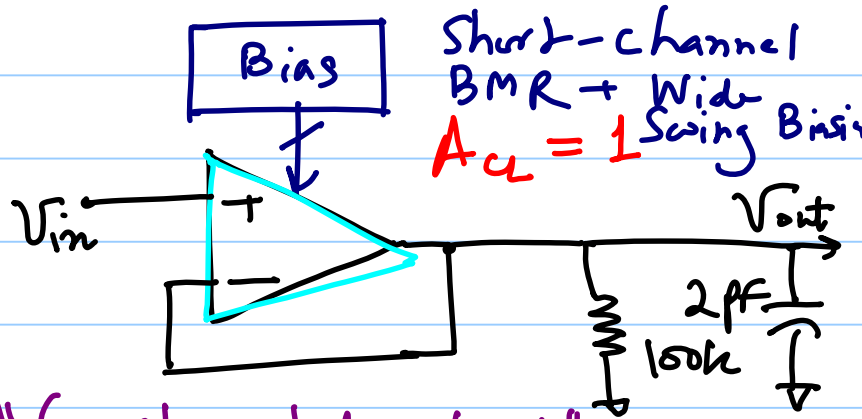
Note Title 4/19/2014

Table 1: Opamp design specifications.

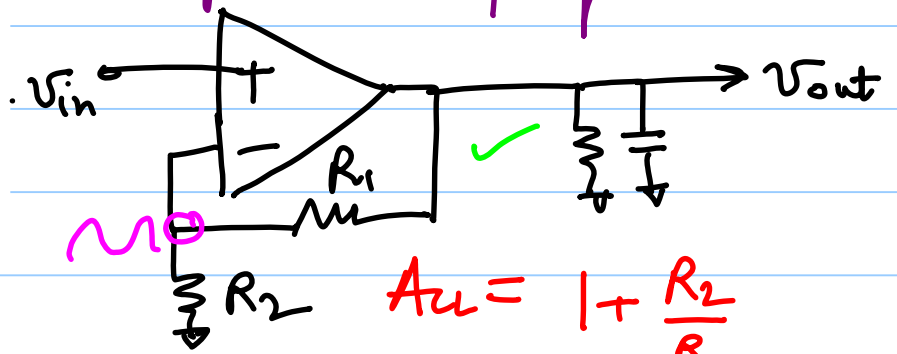
Parameter	Specified Value
Technology	TSMC 180n CMOS ✓
Supply voltage, V_{DD}	1.8 V ✓
Typical load	$100k\Omega \| \| 2pF$
Unit gain frequency (f_{un})	$> 50\,MHz$ *for ECE 411*
	$> 200\,MHz$ *for ECE 511*
Open-loop gain (A_{OL})	$> 75\,dB$
Slew-rate (SR)	$> 500\frac{V}{\mu s}$
Phase margin (ϕ_M)	$\gtrsim 63°$
Power consumption	Minimum possible



$$A_{CL} = -\frac{R_2}{R_1}$$



"Compensated opamp"



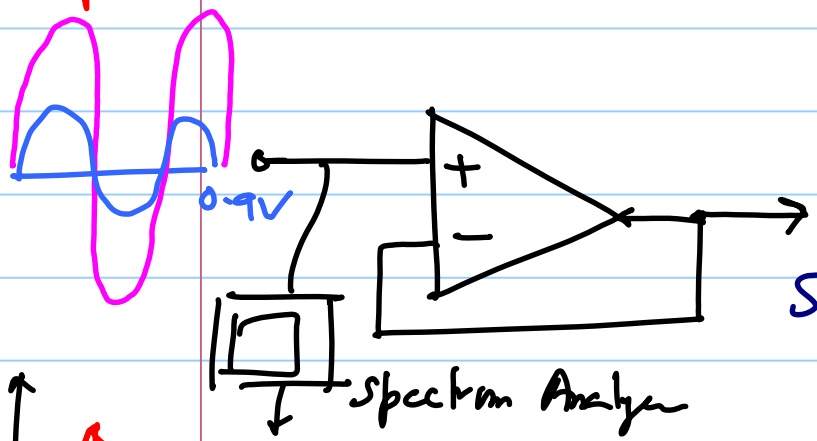
$$A_{CL} = 1 + \frac{R_2}{R_1}$$

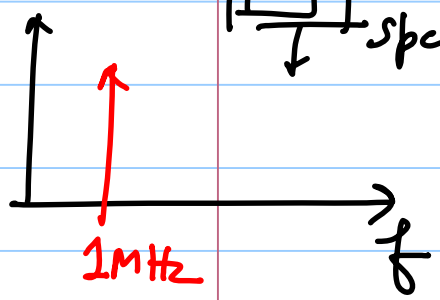
$$f_{un} = \frac{\omega_{un}}{2\pi} = 200\,MHz$$

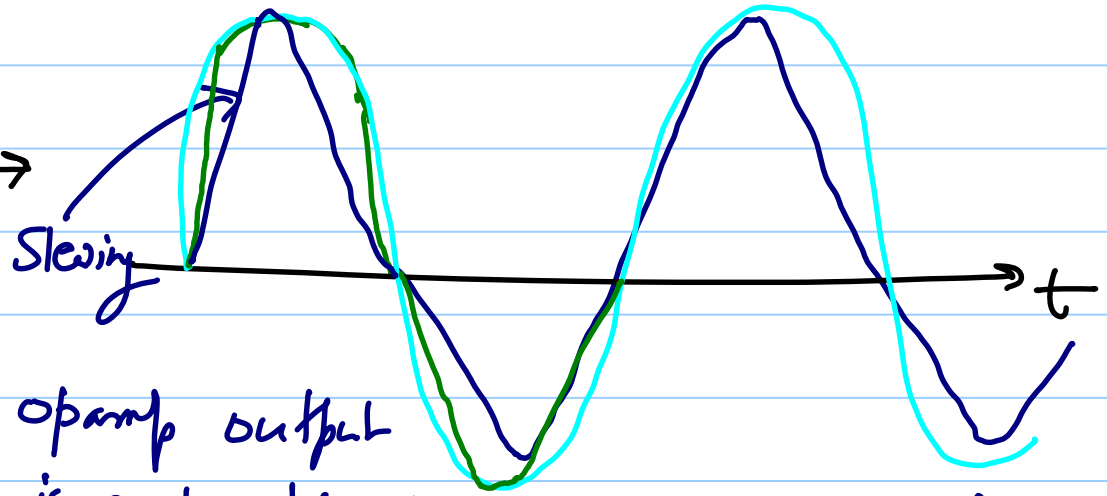
Slewing in opamps

UGB follower

@ 1MHz



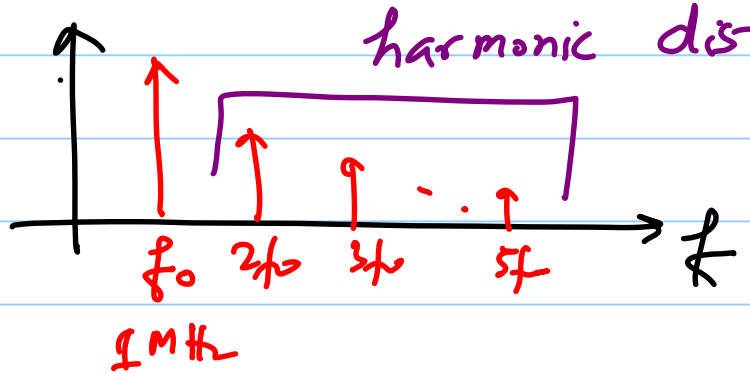


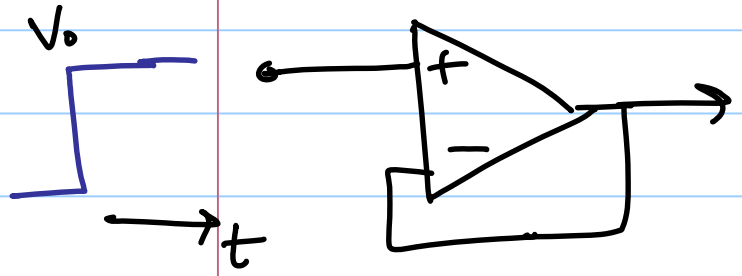


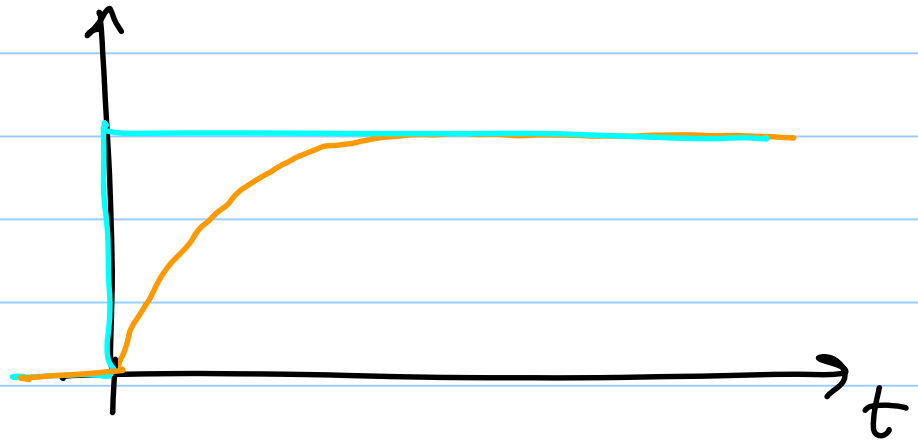
opamp output is not able to change at a faster rate

↳ SR limitation

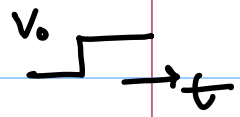
Slewing is a non linear behavior



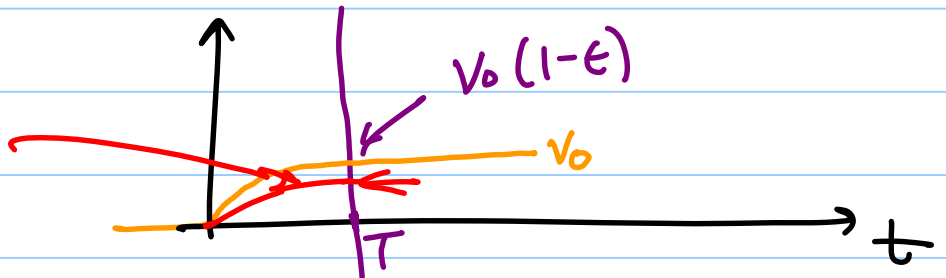


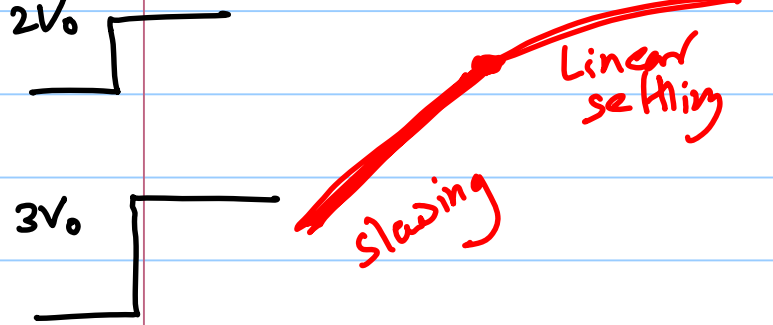


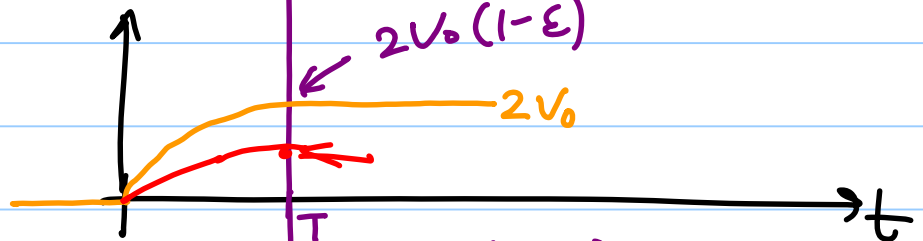
Non-linear settling behavior

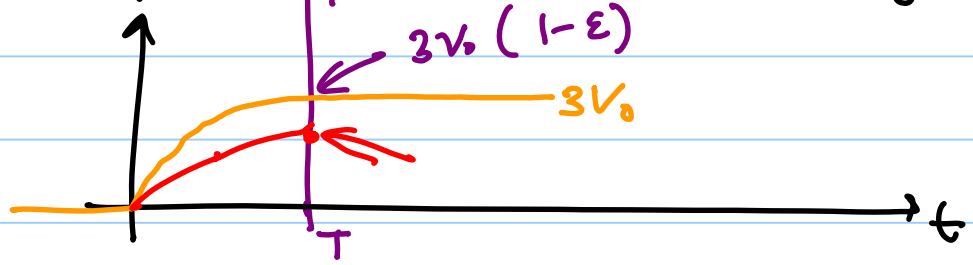


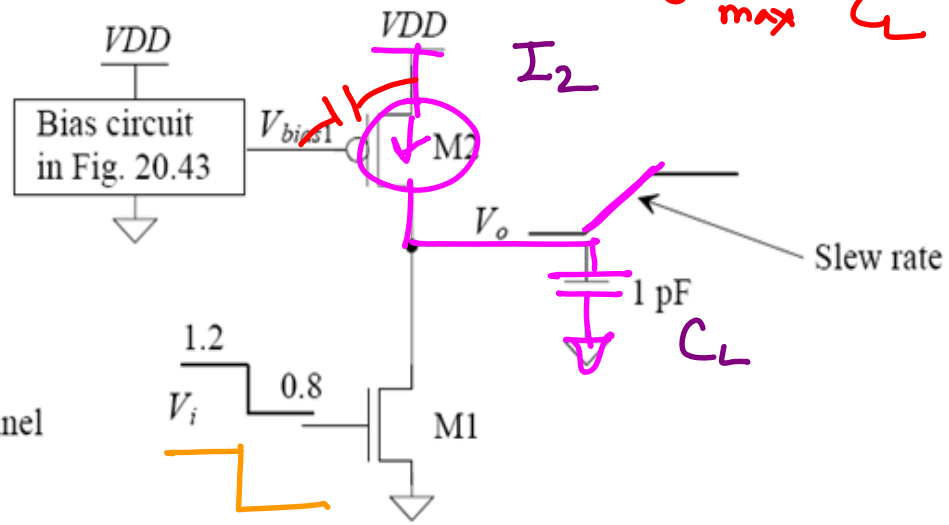
with slewing









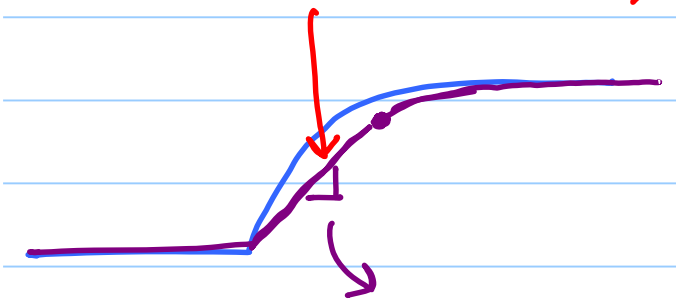


Use the long-channel sizes and biasing seen in Table 9.1.

Figure 21.18 Slew rate limitations in a class A amplifier.

$SR_{max} = \frac{I_2}{C_L}$

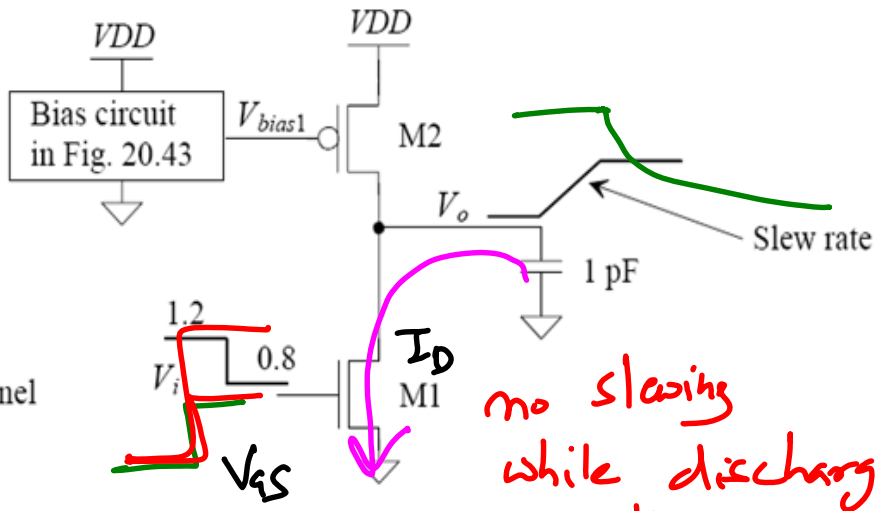
Slewing (non-linear settling)



$\frac{I_2}{C_L} = SR$

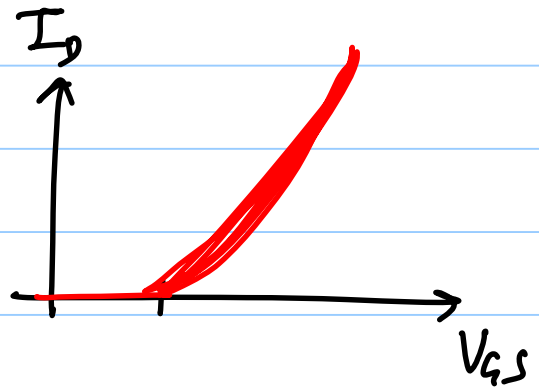
$\frac{dV_{out}}{dt} \leq SR$

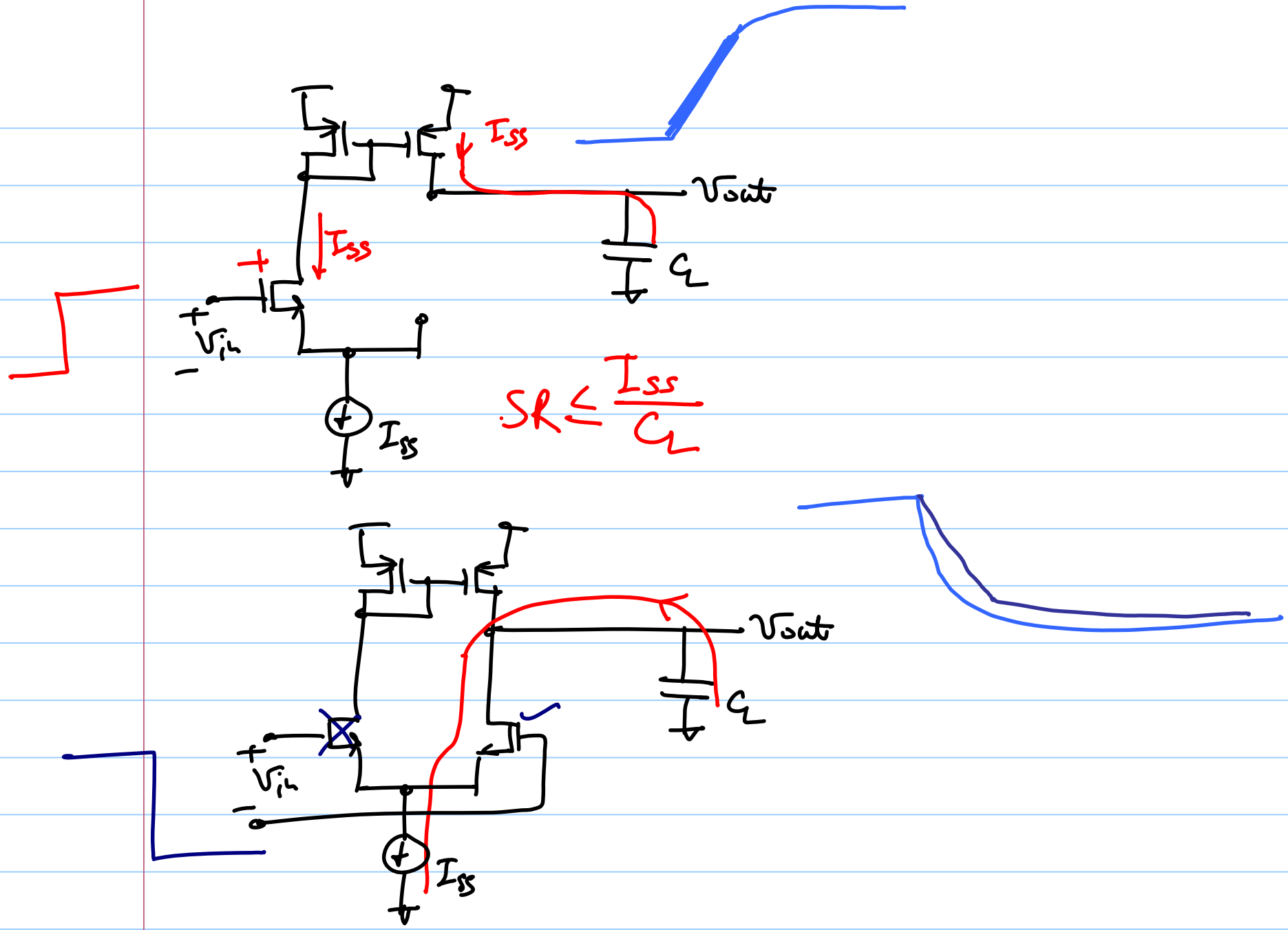
Slew rate limitations because of "current source charging sizable amount of capacitance"

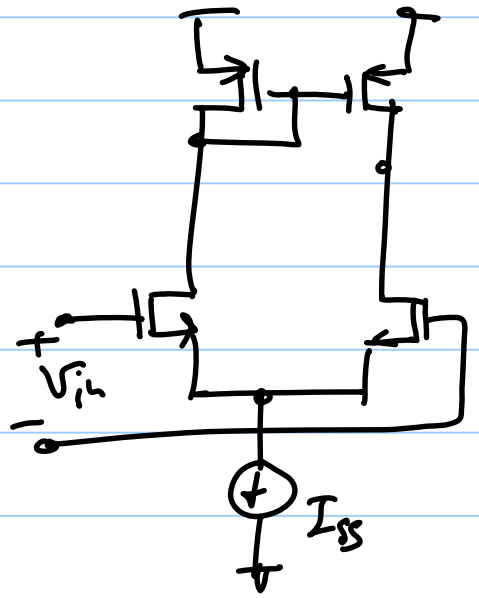


Use the long-channel sizes and biasing seen in Table 9.1.

Figure 21.18 Slew rate limitations in a class A amplifier




I_{SS}
V_{out}
I_{SS}
C_L
V_{in}
I_{SS}
$SR \leq \frac{I_{SS}}{C_L}$
V_{out}
C_L
V_{in}
I_{SS}



$\Rightarrow \frac{g_m r_o}{2}$

Telescopic

$g_m \left(\frac{g_m r_o^2}{2}\right)$

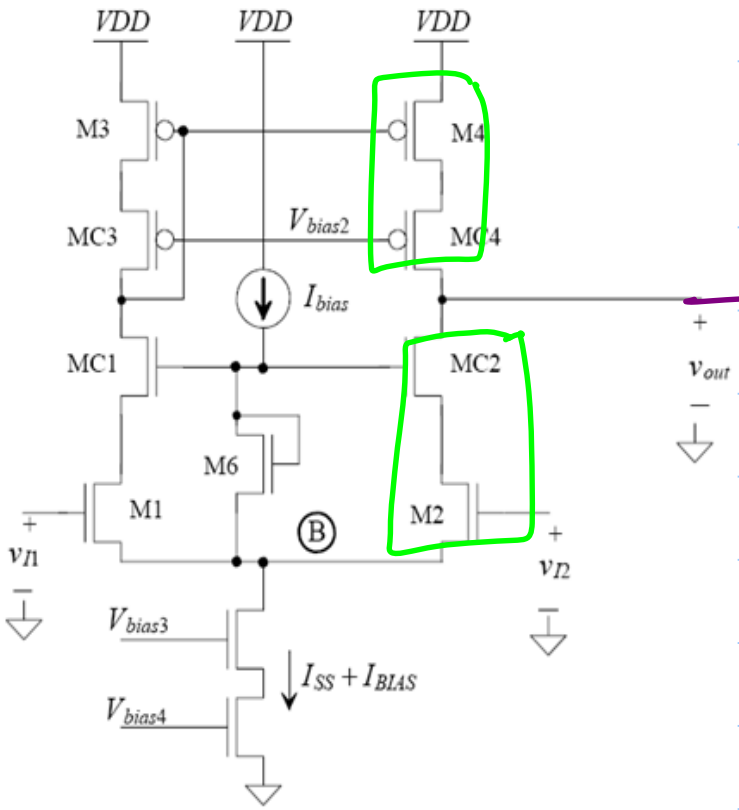


Figure 22.30 Cascode differential amplifier.

$R_{out} = (g_m r_o^2)_p \,||\, (g_m r_o^2)_n \,||\, R_L$

R_L

100k

100k 2pF

R_L