Opamp Design Project

Help Session

Boise, 19/Apr/2014

Vishal Saxena

Design Specifications

Table 1: Opamp design specifications.

Parameter	Specified Value
Technology	TSMC 180n CMOS
Supply voltage, V_{DD}	1.8 V
Typical load	$100k\Omega \| \| 2pF$
Unit gain frequency (f_{un})	$> 50\,MHz$ *for ECE 411*
	$> 200\,MHz$ *for ECE 511*
Open-loop gain (A_{OL})	$> 75\,dB$
Slew-rate (SR)	$> 500\frac{V}{\mu s}$
Phase margin (ϕ_M)	$\gtrsim 63°$
Power consumption	Minimum possible

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Two-Stage Opamp

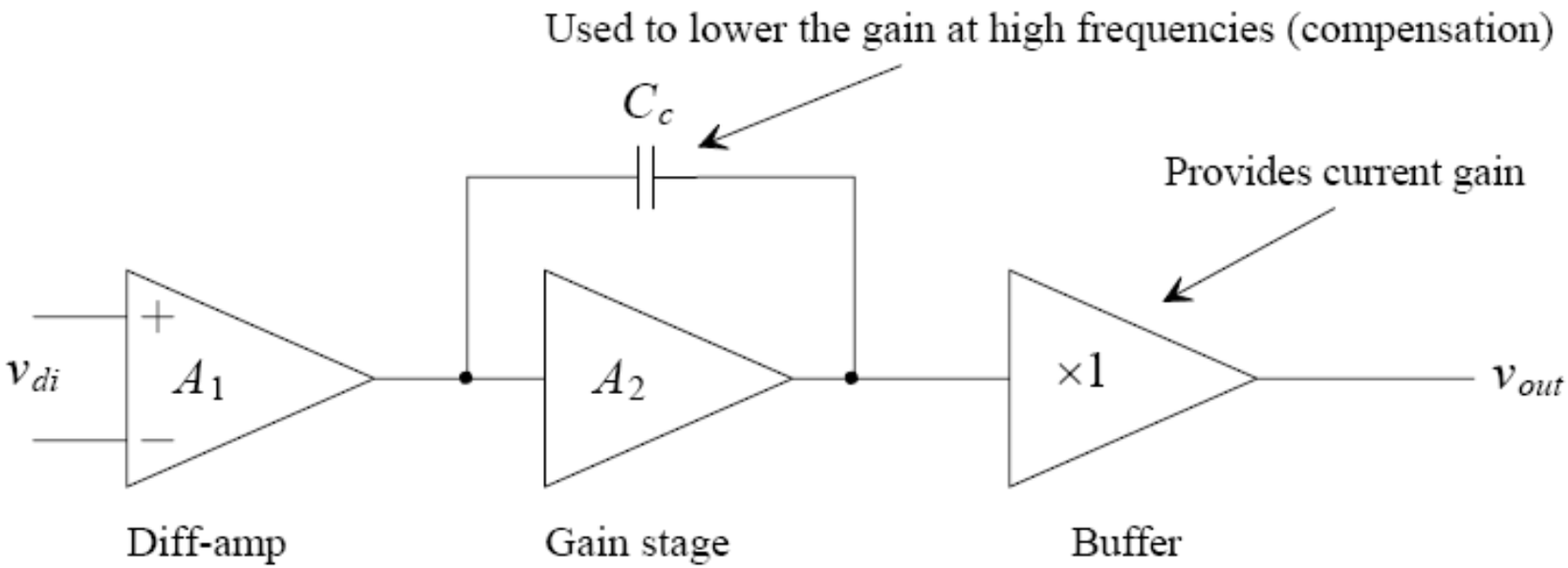
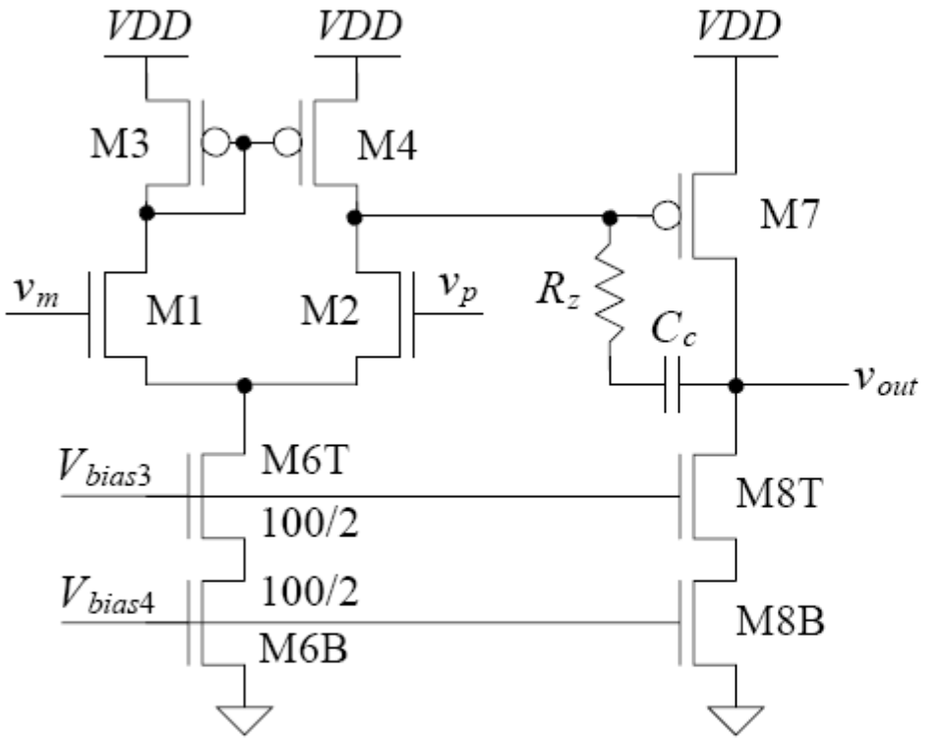
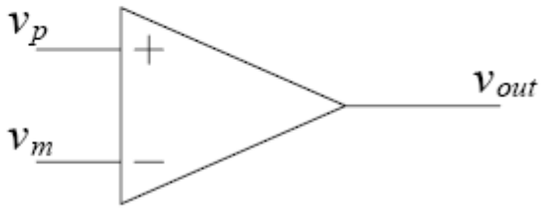


Figure 24.1 Block diagram of two-stage op-amp with output buffer.

Two-Stage Opamp



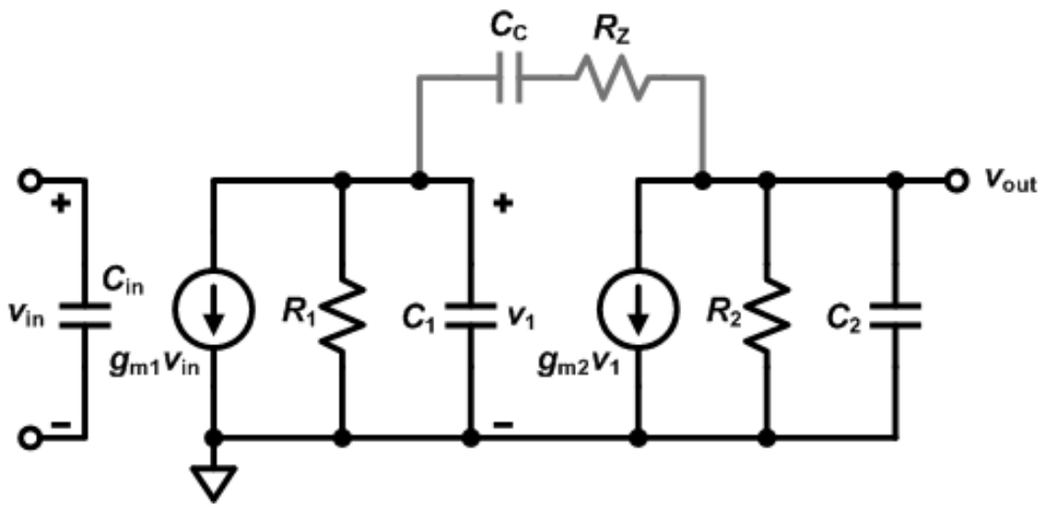
Parameters from Table 9.2 with biasing circuit from Fig. 20.47. Unlabeled NMOS are 50/2 and PMOS are 100/2. Scale factor is 50 nm.



Op-amp schematic symbol

Figure 24.2 Basic two-stage op-amp.

Design Equations



$$A_v = g_{m1}R_1g_{m2}R_2$$

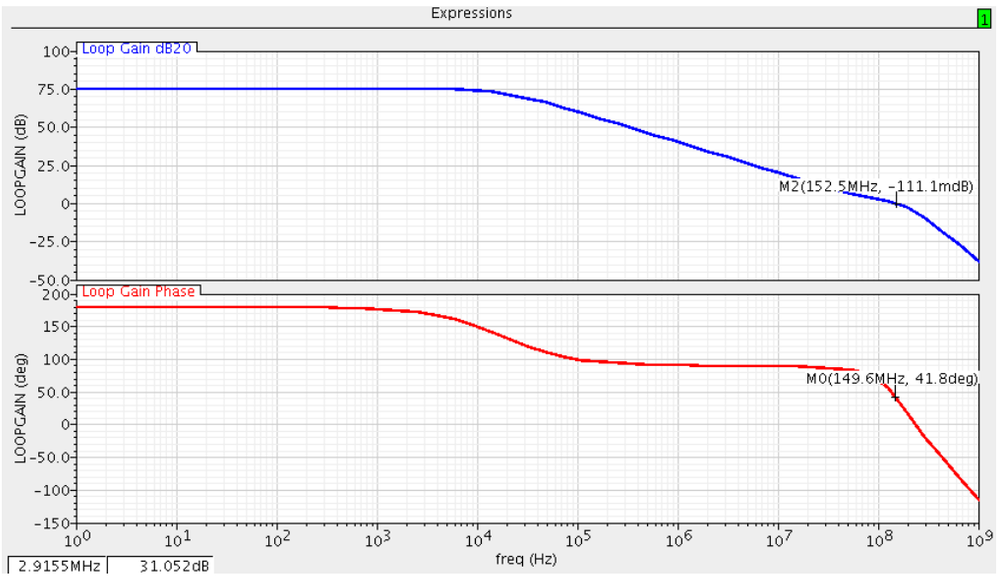
$$\omega_{p1} \approx \frac{1}{g_{m2}R_2R_1C_c}$$

$$\omega_{p2} \approx \frac{g_{m2}C_c}{C_2(C_1+C_C)+C_CC_1} = f\left(\frac{g_{m2}}{C_2}\right)$$

$$\omega_z \approx \frac{g_{m2}}{C_c}$$

$$\omega_{un} \approx \frac{g_{m1}}{C_c}$$

$$\omega_{z,nulling-R} \approx \frac{1}{(\frac{1}{g_{m2}-R_z})C_c}$$



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Two-Stage Opamp –Zero-Nulling R

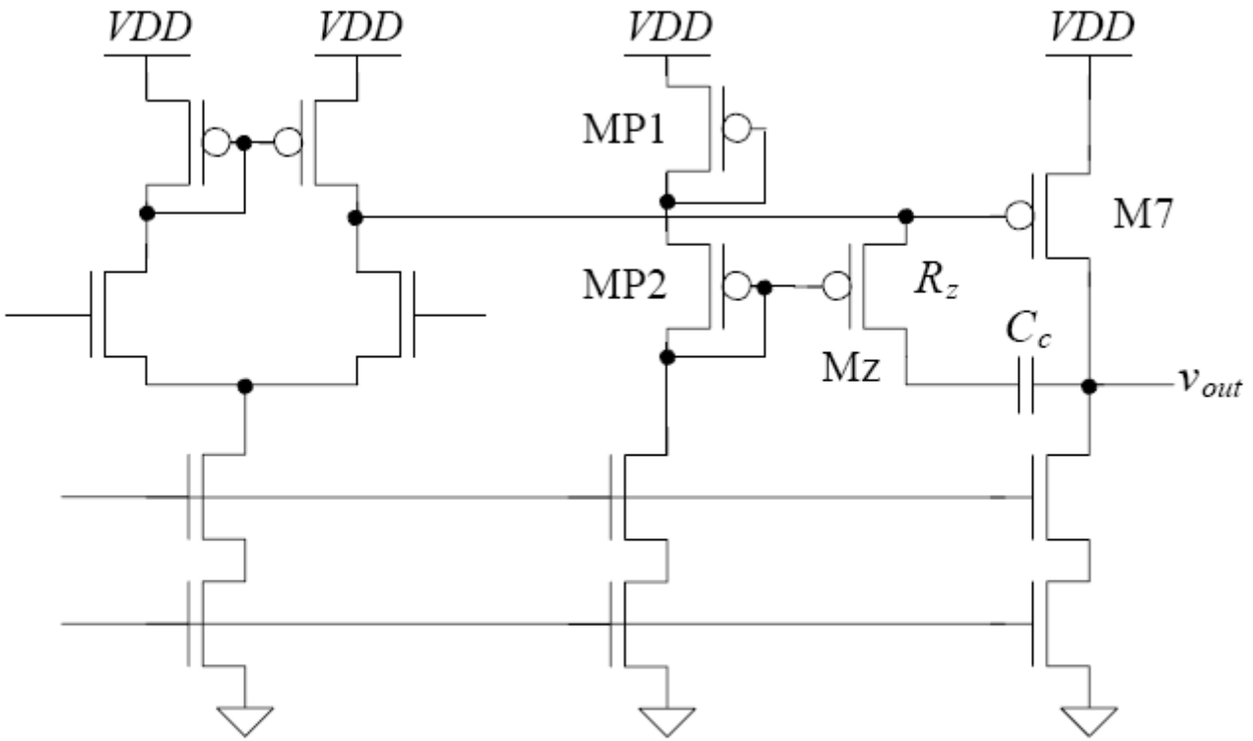


Figure 24.15 Making the zero-nulling resistor process independent.

Two-Stage Opamp –Voltage Buffer Compensation

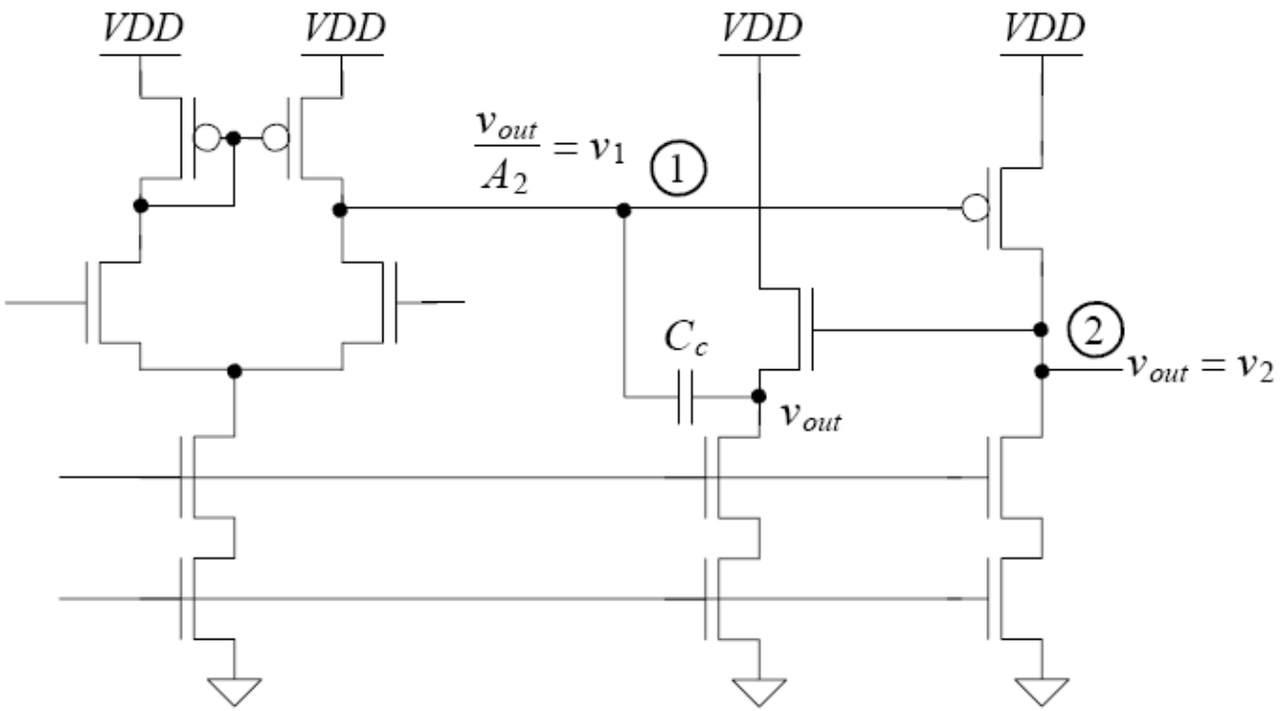


Figure 24.16 Using an amplifier to eliminate forward signal feedthrough via the compensation capacitor.

Two-Stage Opamp –Common Gate Compensation

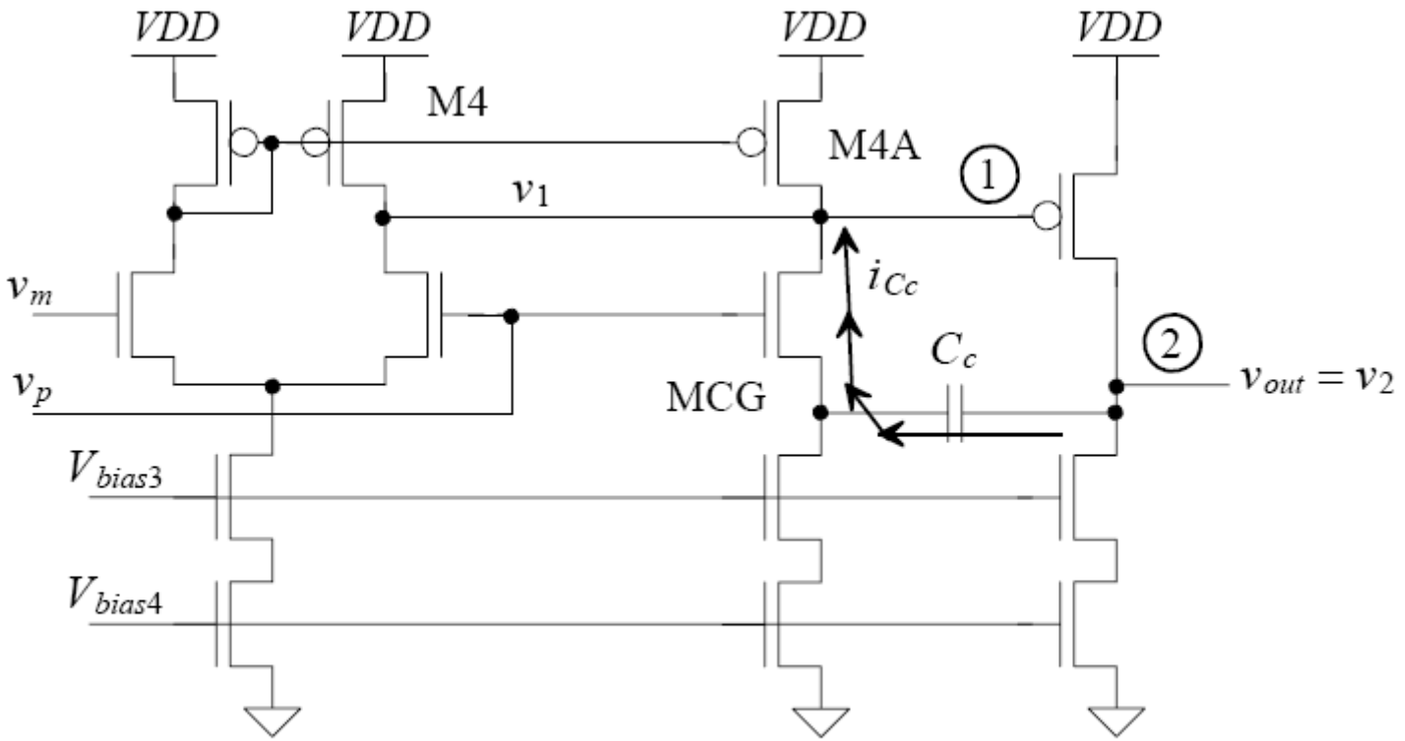


Figure 24.17 Feeding back a current indirectly to avoid the RHP zero.

Class-A Stage: Slewing

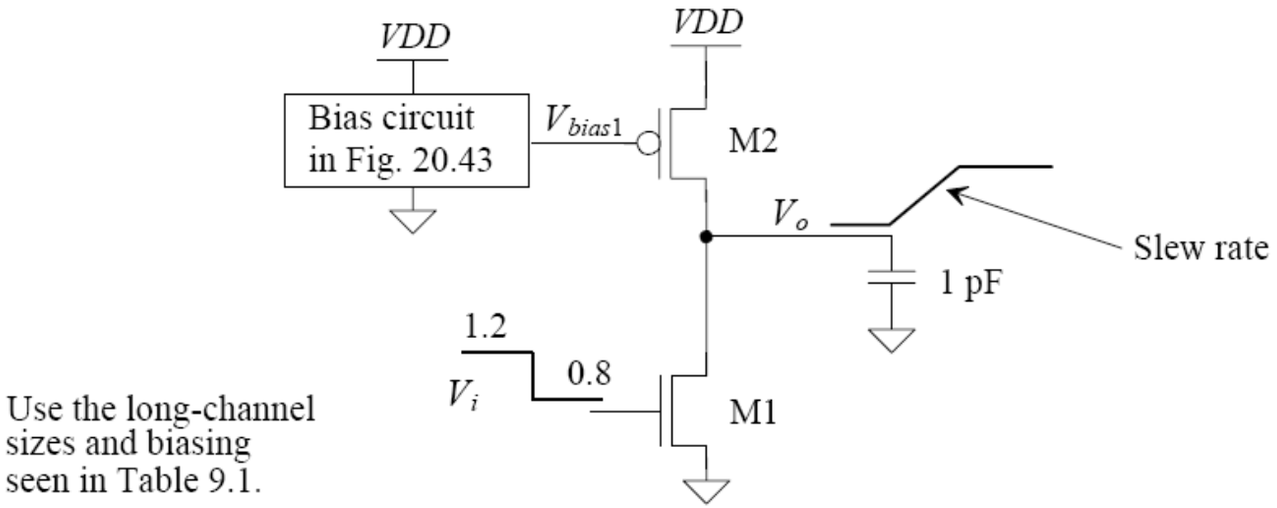


Figure 21.18 Slew rate limitations in a class A amplifier.

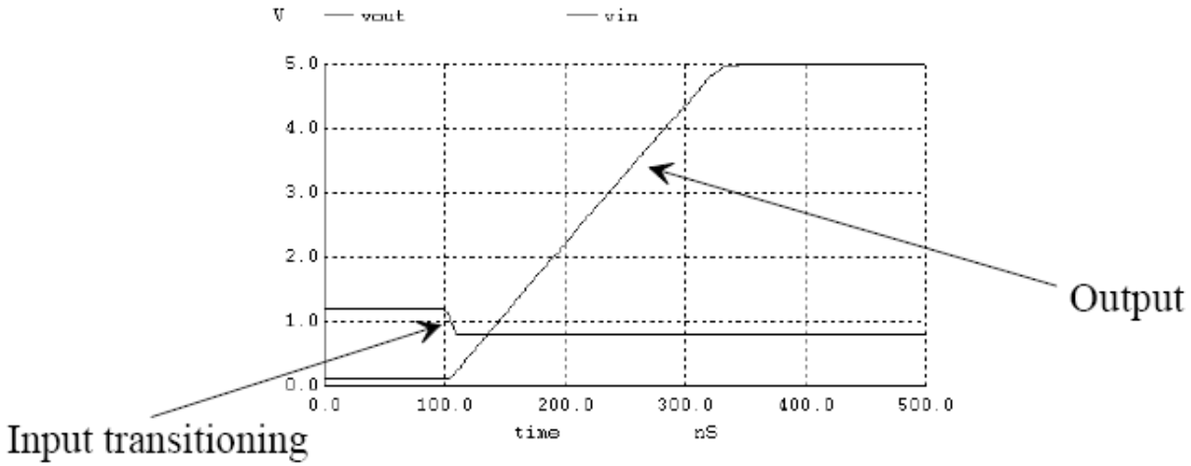
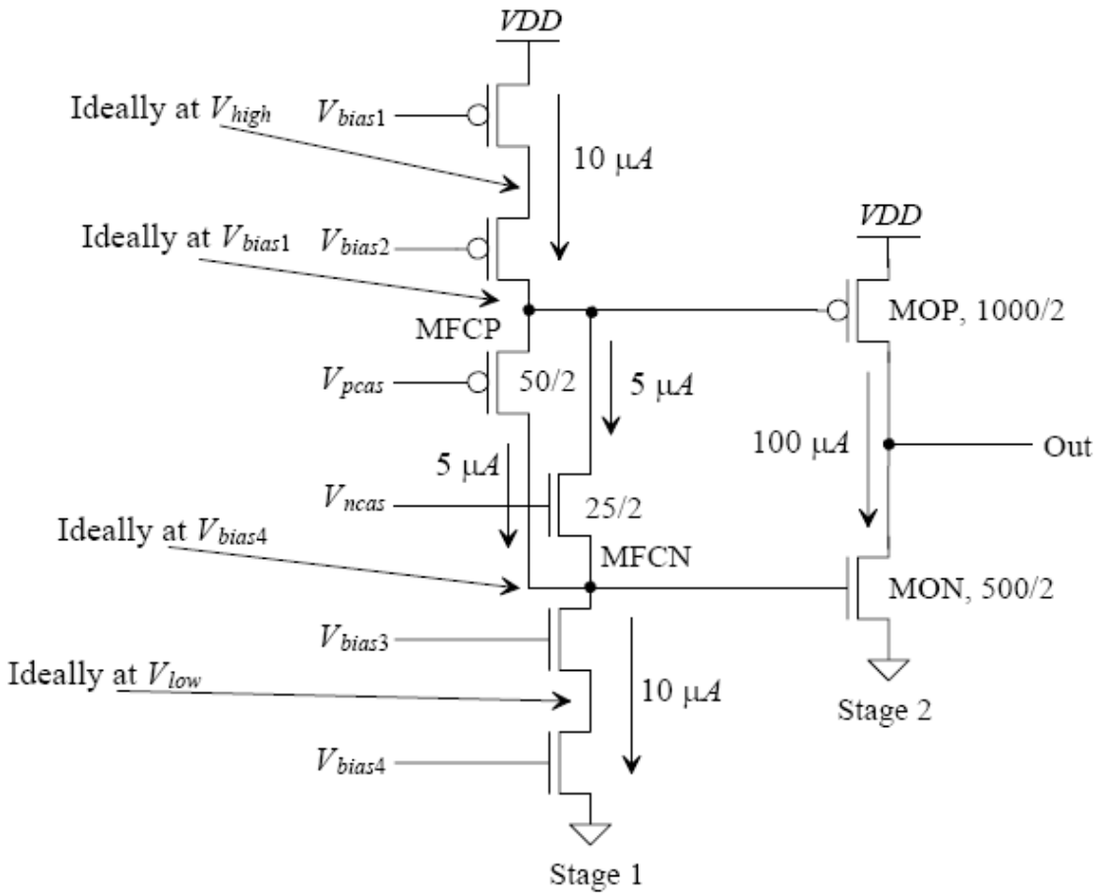


Figure 21.19 Verifying the results in Ex. 21.5

Class-AB Stage: Floating Current Mirror



Bias voltages come from Fig. 20.47 (short-channel parameters in Table 9.2). Unlabeled NMOS are 50/2, while unlabeled PMOS are 100/2.

Figure 20.49 Biasing with a floating current source.

Two-Stage Opamp –Telescopic with Class-AB Stage

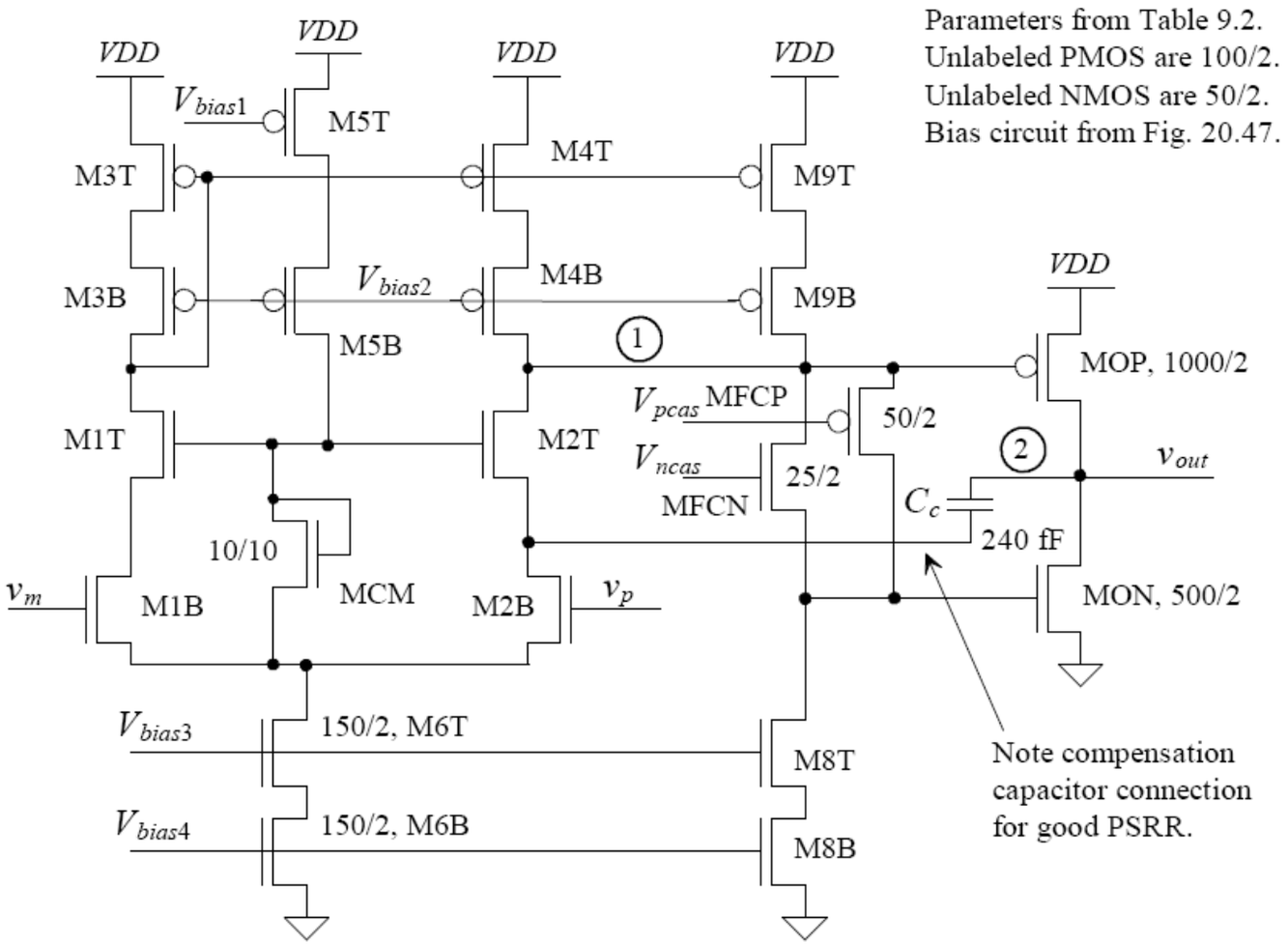


Figure 24.29 A CMOS op-amp with output buffer.

Folded Cascode OTA

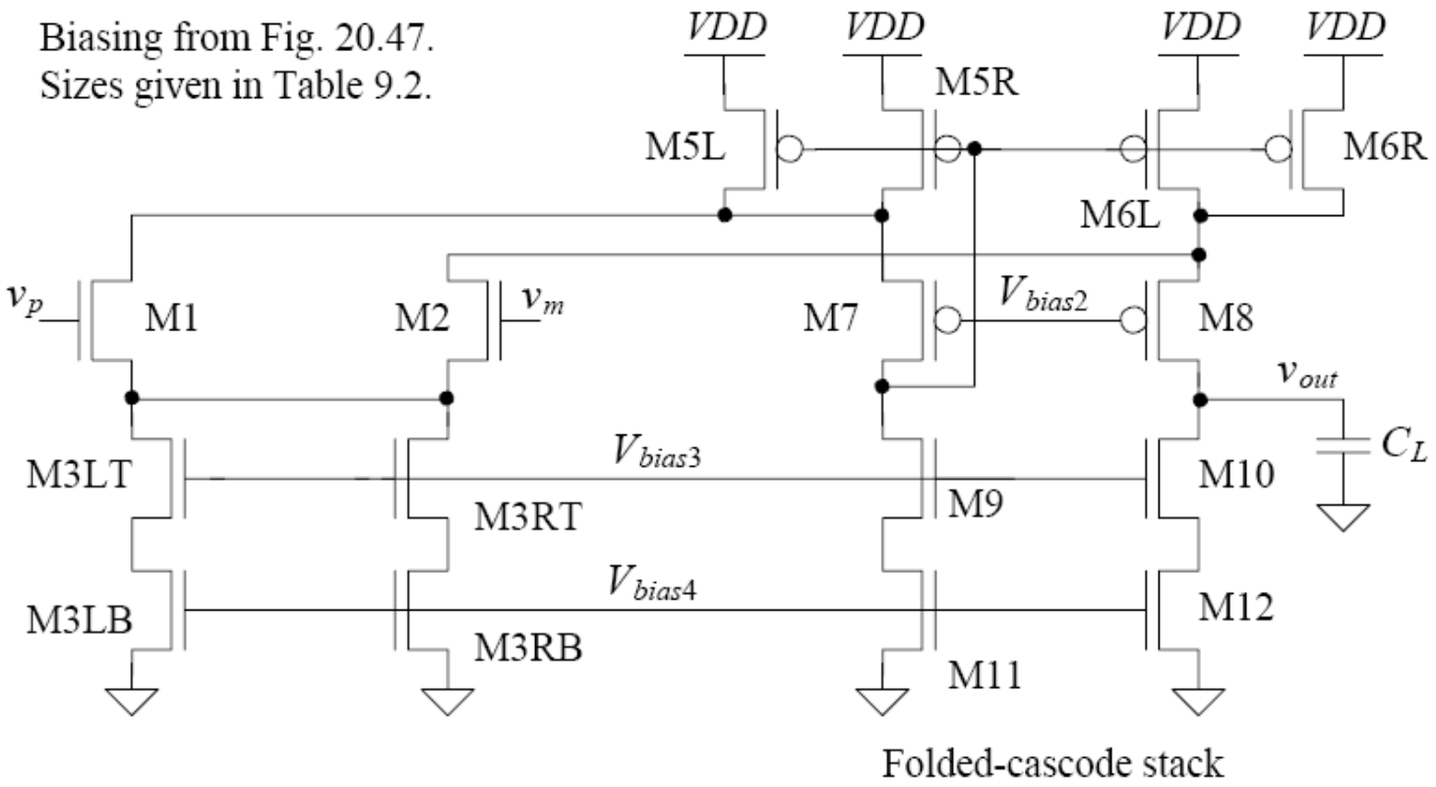


Figure 24.42 A folded-cascode OTA.

Two-Stage Opamp –Folded-Cascode with Class-AB Stage

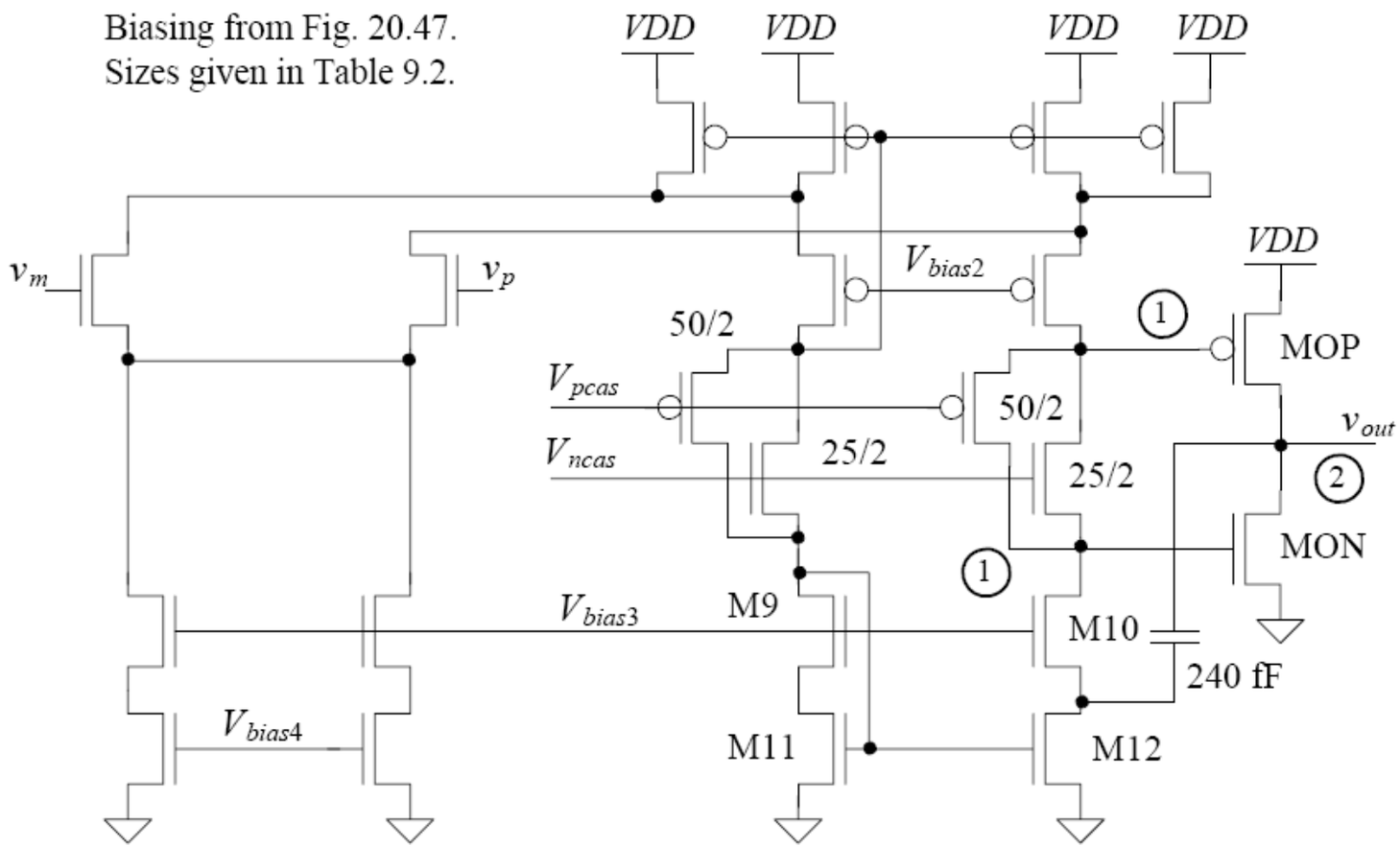
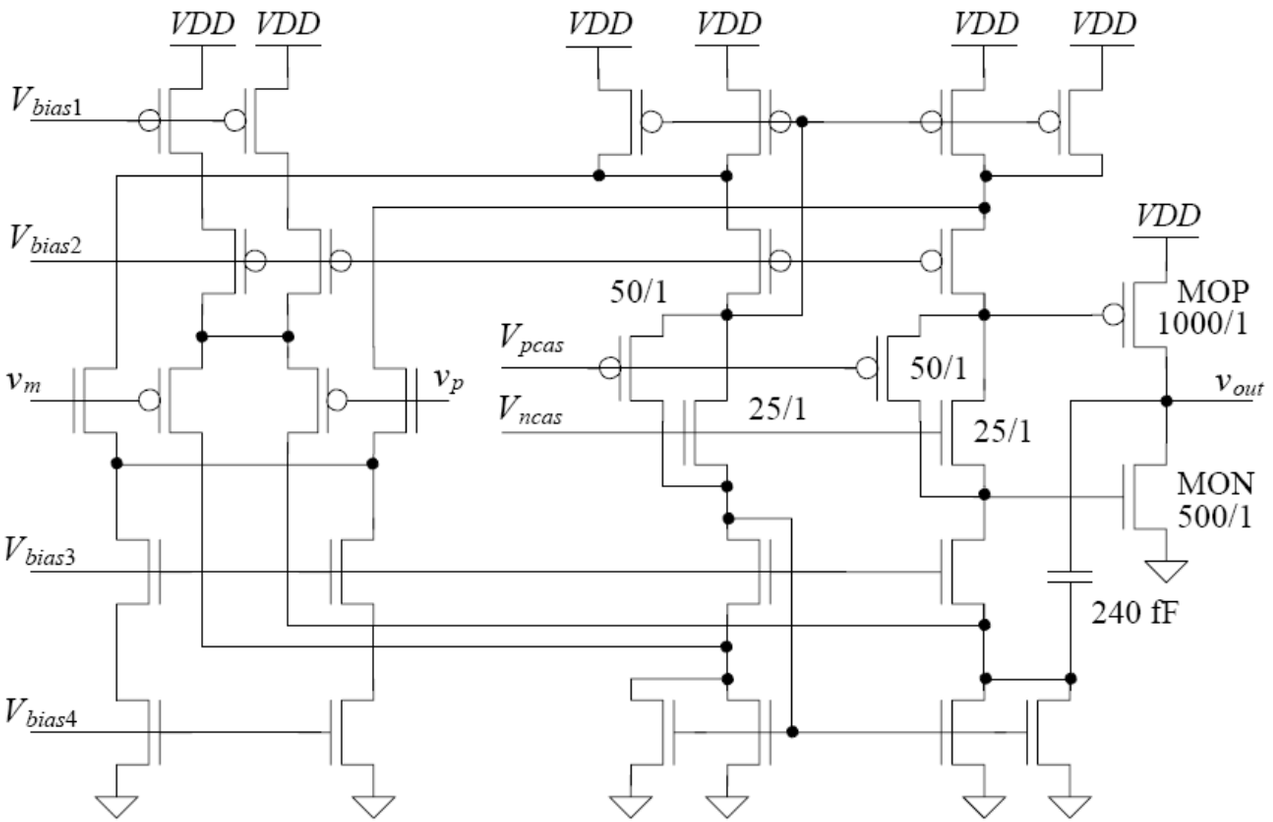


Figure 24.44 Folded-cascode op-amp with class AB output buffer.

Two-Stage Opamp –Folded-Cascode + Class-AB Stage, Full-rail input CMR



Biasing from Fig. 20.47.
Unlabeled NMOS are 50/1.
Unlabeled PMOS are 100/1.

Figure 24.48 An op-amp with an input common-mode range that extends beyond the power supply rails and that can drive heavy loads.

Two-Stage Opamp –Gain Enhancement

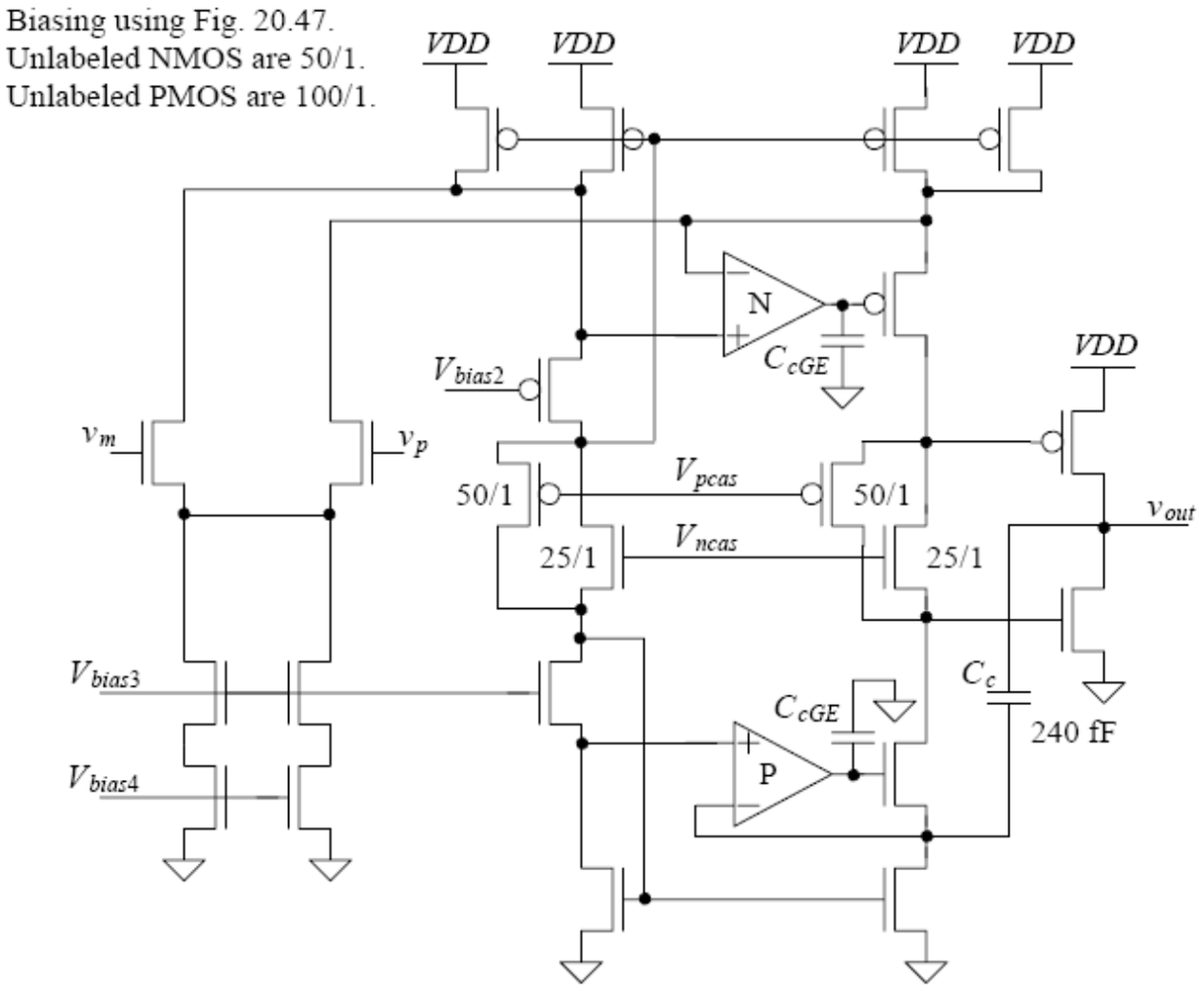


Figure 24.51 Folded-cascode op-amp with class AB output buffer and gain-enhancement.

Two-Stage Opamp –AC Response

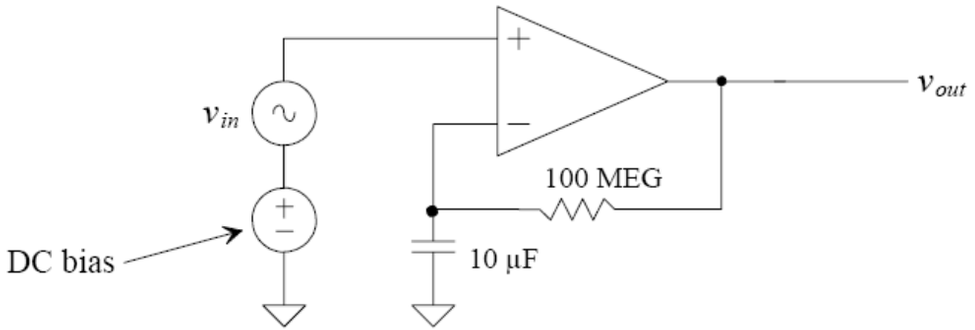


Figure 24.9 Circuit configuration used to simulate open-loop frequency response.

Caveat:

- **Don't use this method.**
- **Use STB analysis with *iprobe* instead.**

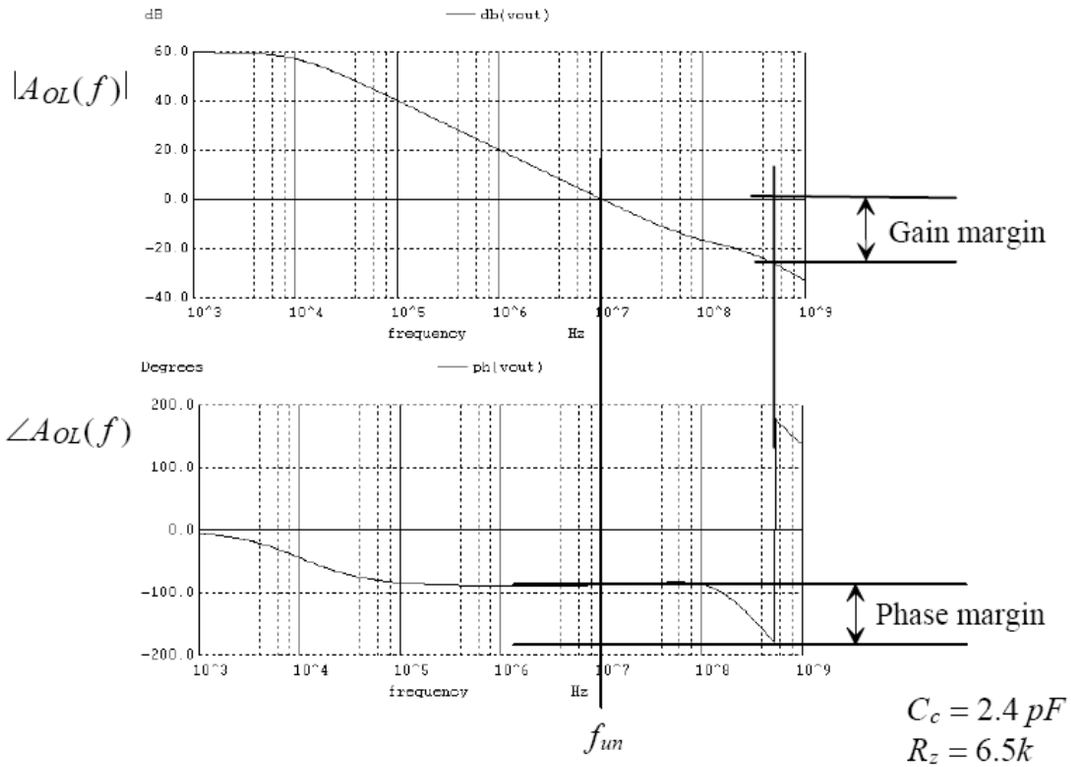
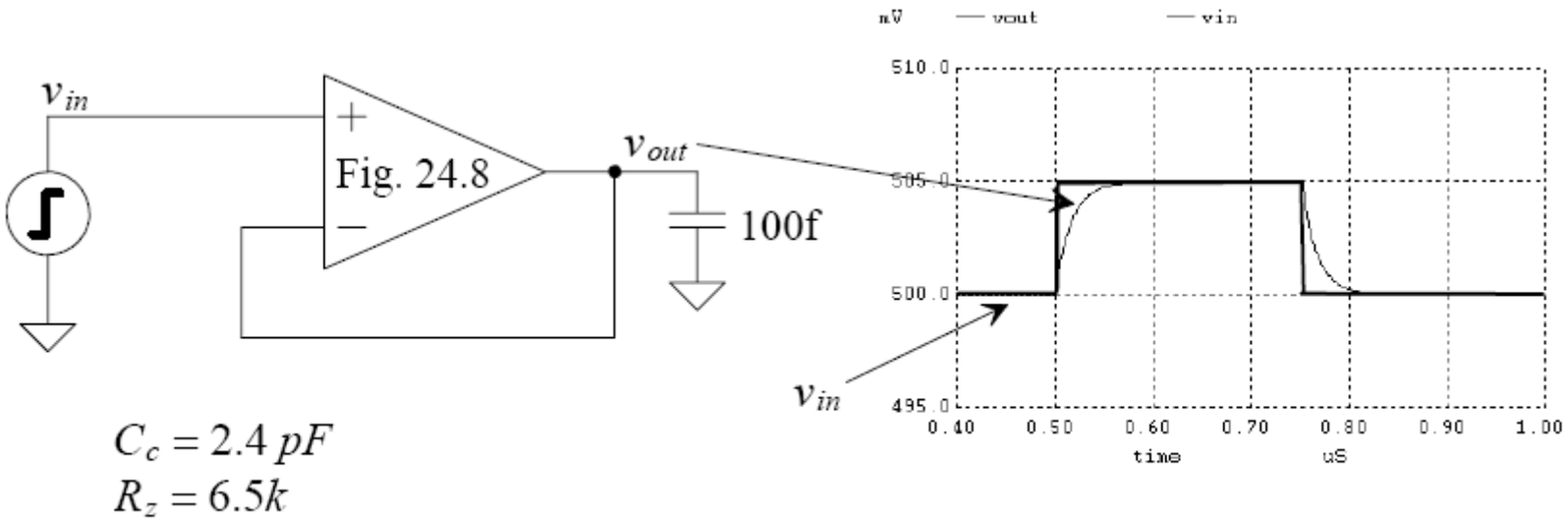


Figure 24.13 Adding a zero nulling resistor to the op-amp in Fig. 24.8.

Two-Stage Opamp –Step Response



$C_c = 2.4\,pF$

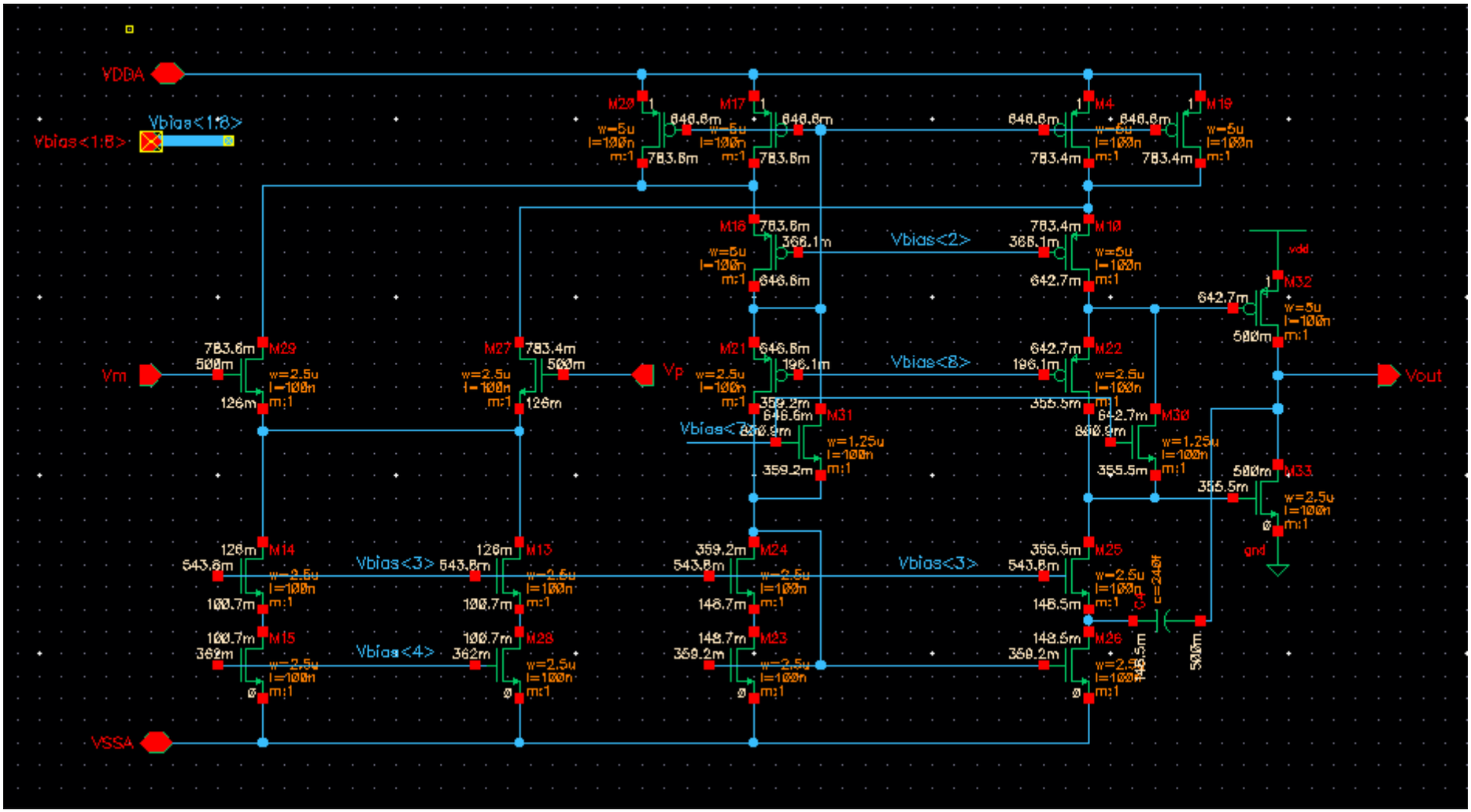
$R_z = 6.5k$

Figure 24.14 Good step response of the op-amp with the zero absent.

Spectre STB Analysis

- The STB analysis linearizes the circuit about the DC operating point and computes the loop-gain, gain and phase margins (if the sweep variable is frequency), for a feedback loop or a gain device [1].
- Refer to the Spectre Simulation Refrence [1] and [2] for details.

Example Single-ended Opamp Schematic



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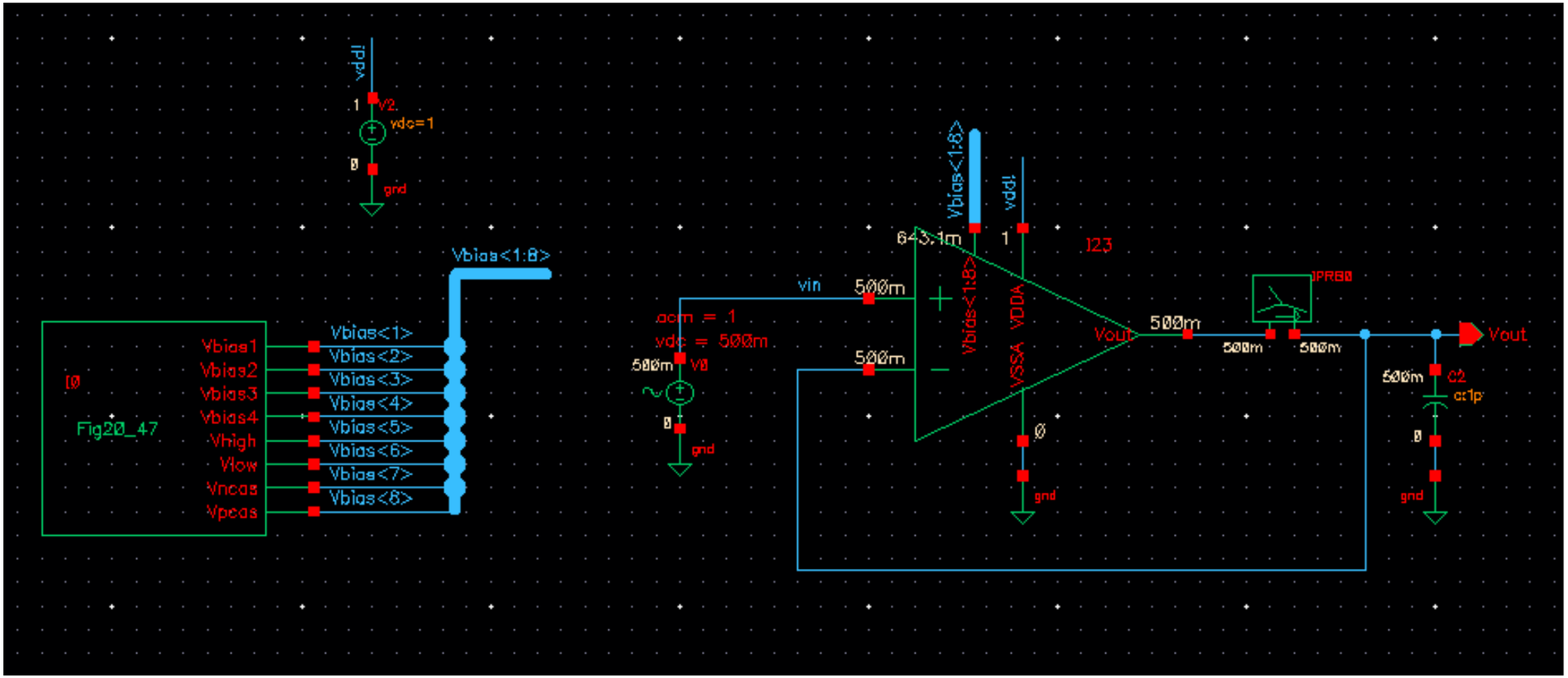
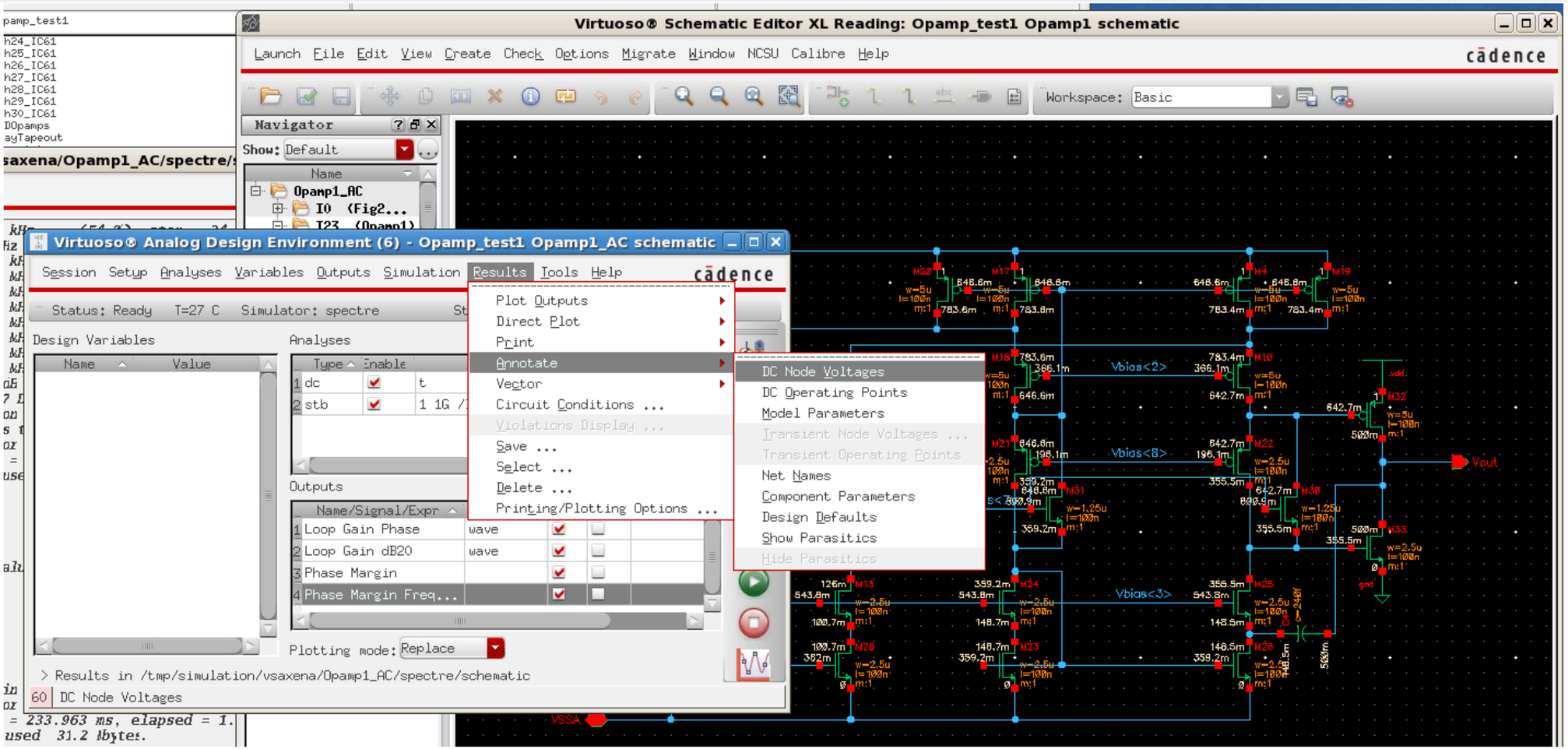
STB Analysis Test Bench



- Pay attention to the **iprobe** component (from analogLib)
  - Acts as a short for DC, but breaks the loop in stb analysis
- Place the probe at a point where it completely breaks (all) the loop(s).

DC Annotation



- Annotating the node voltages and DC operating points of the devices helps debug the design
  - Check device gds to see if its in triode or saturation regions

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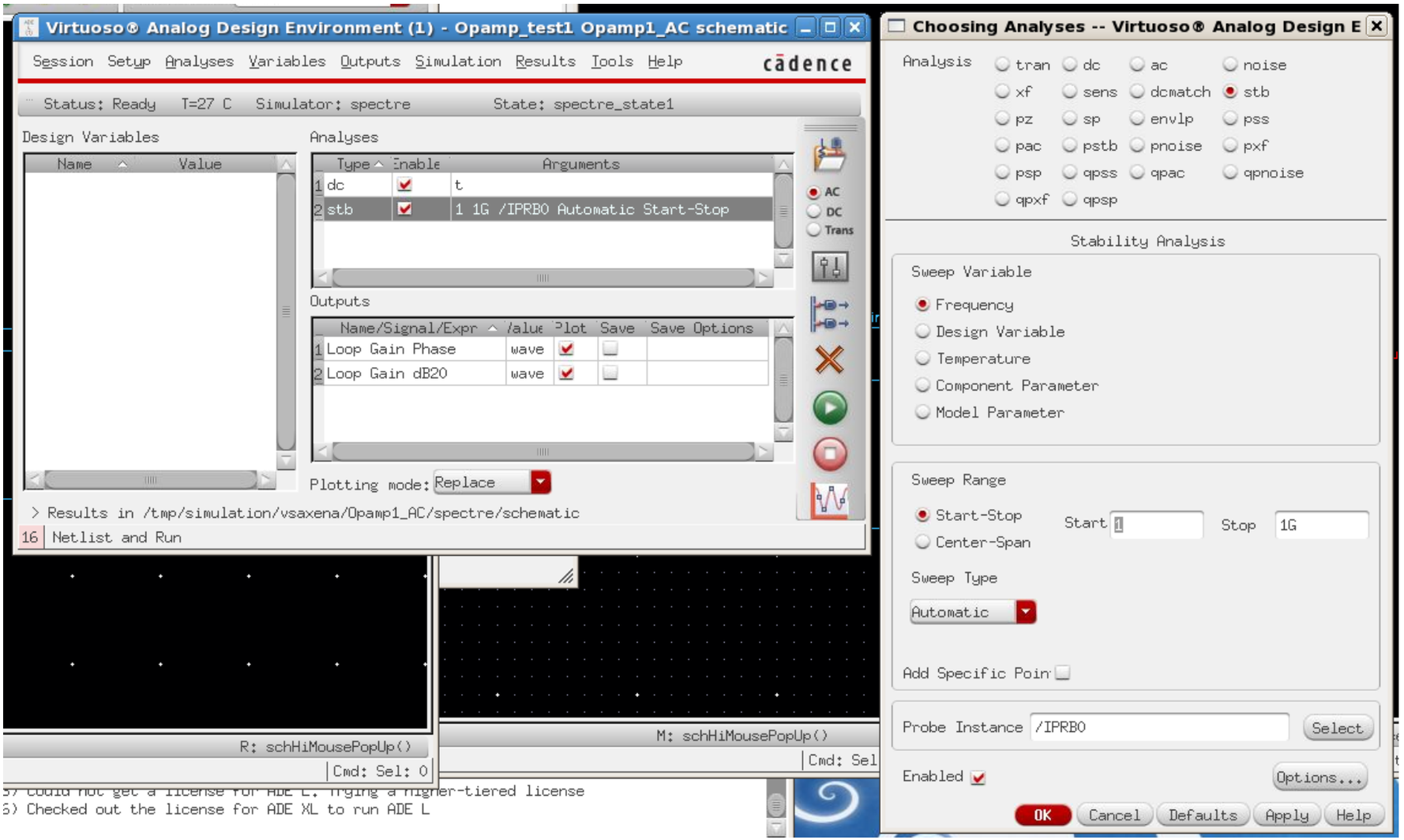
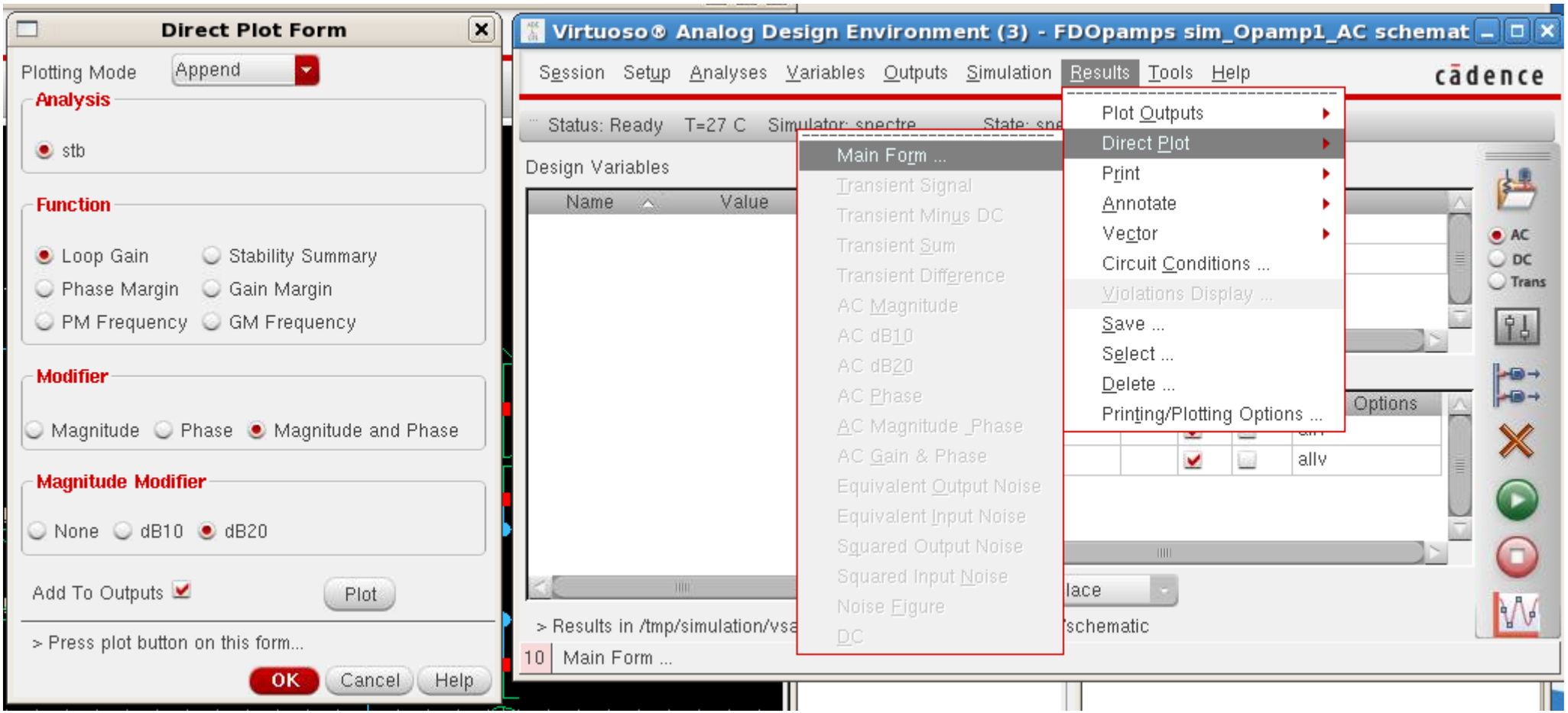
Simulation Setup



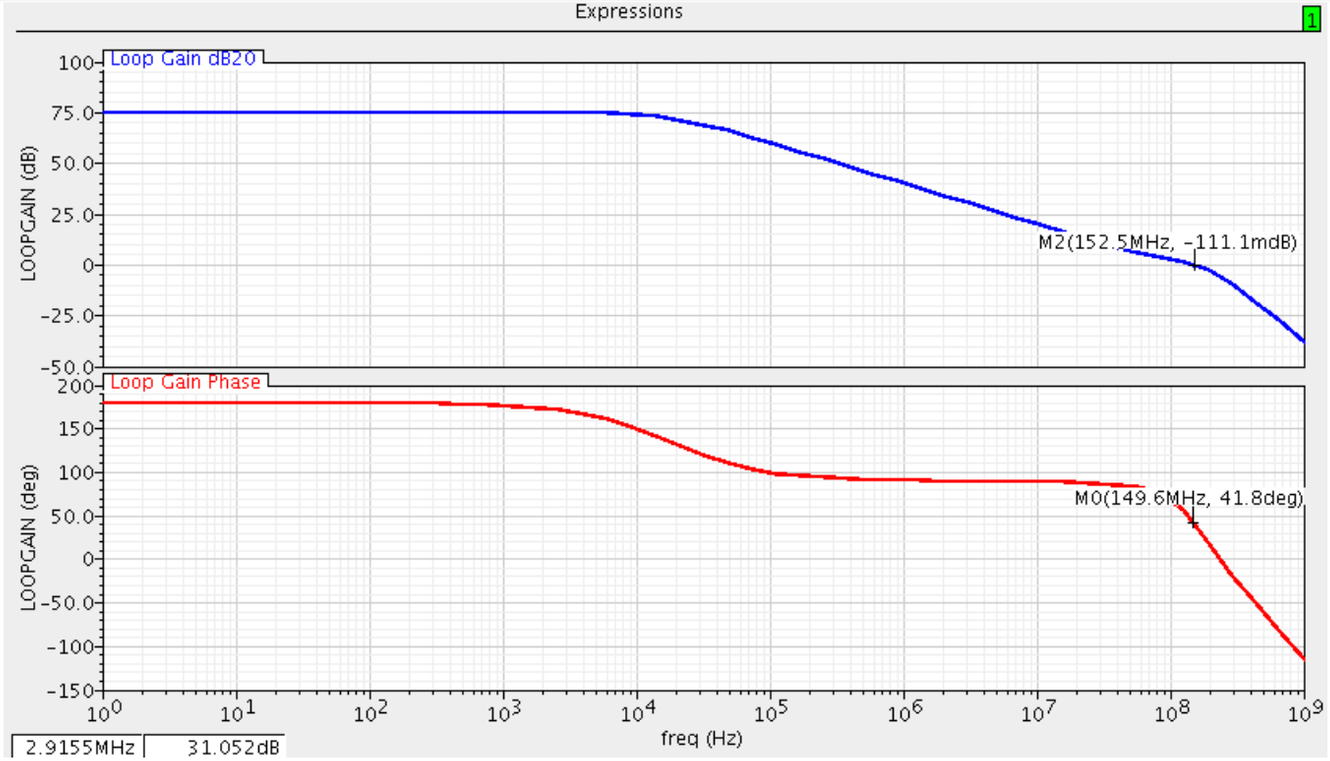
- Always have dc analysis on for debugging purpose

Bode Plot Setup



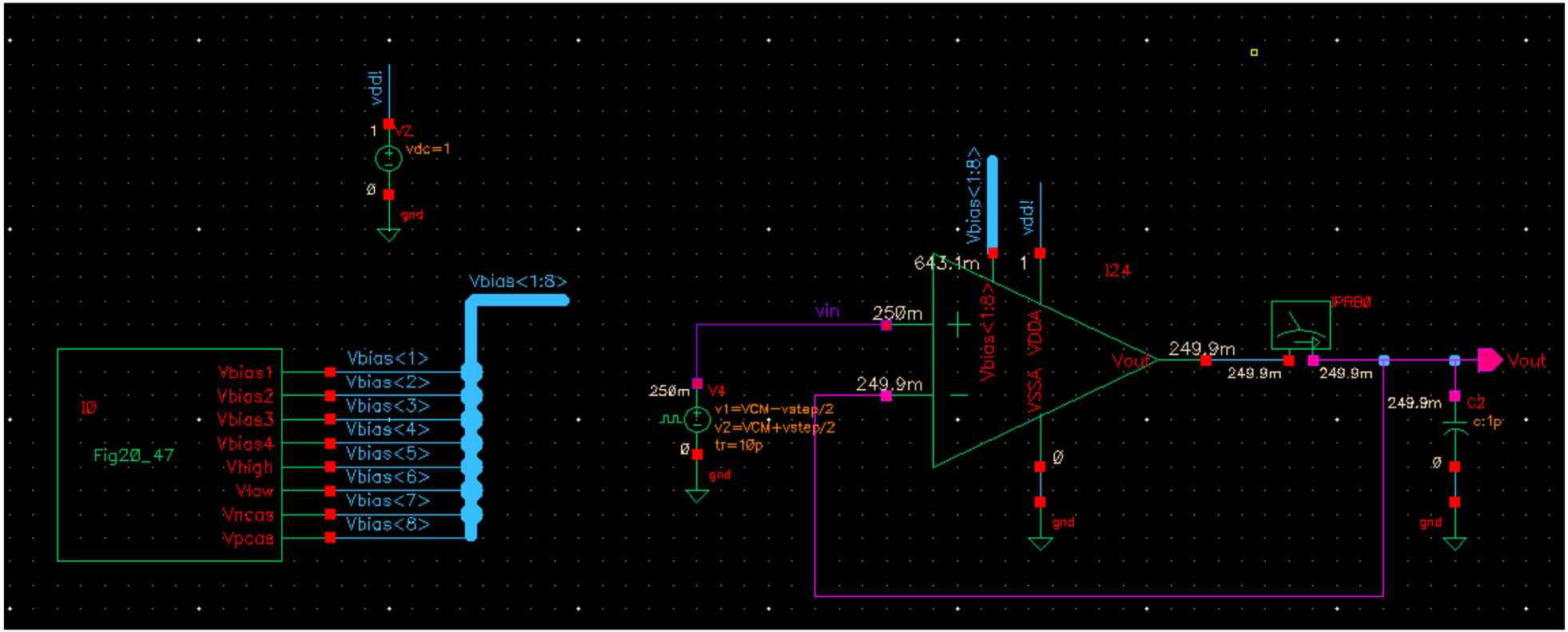
- **Results->Direct Plot-> Main Form**

Open Loop Response Bode Plots



- Here, f_{un}=152.5 MHz, PM=41.8º
- Try to use the stb analysis while the circuit is in the desired feedback configuration
  - Break the loop with realistic DC operation points

Transient Step Response Test Bench



- Transient step-response verifies the closed-loop stability
- Use small as wells as large steps for characterization
- iprobe acts as a short (can remove it)

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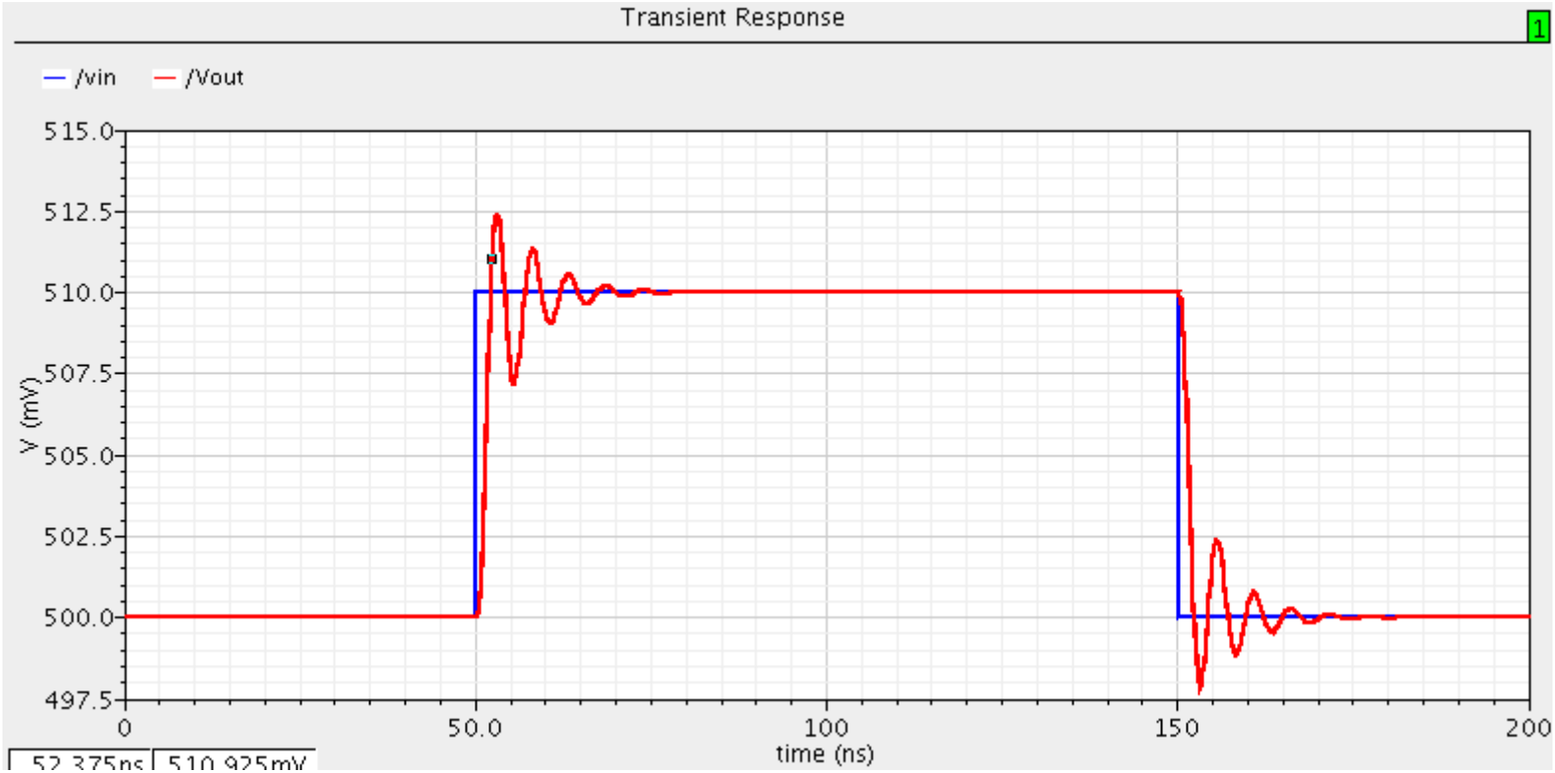
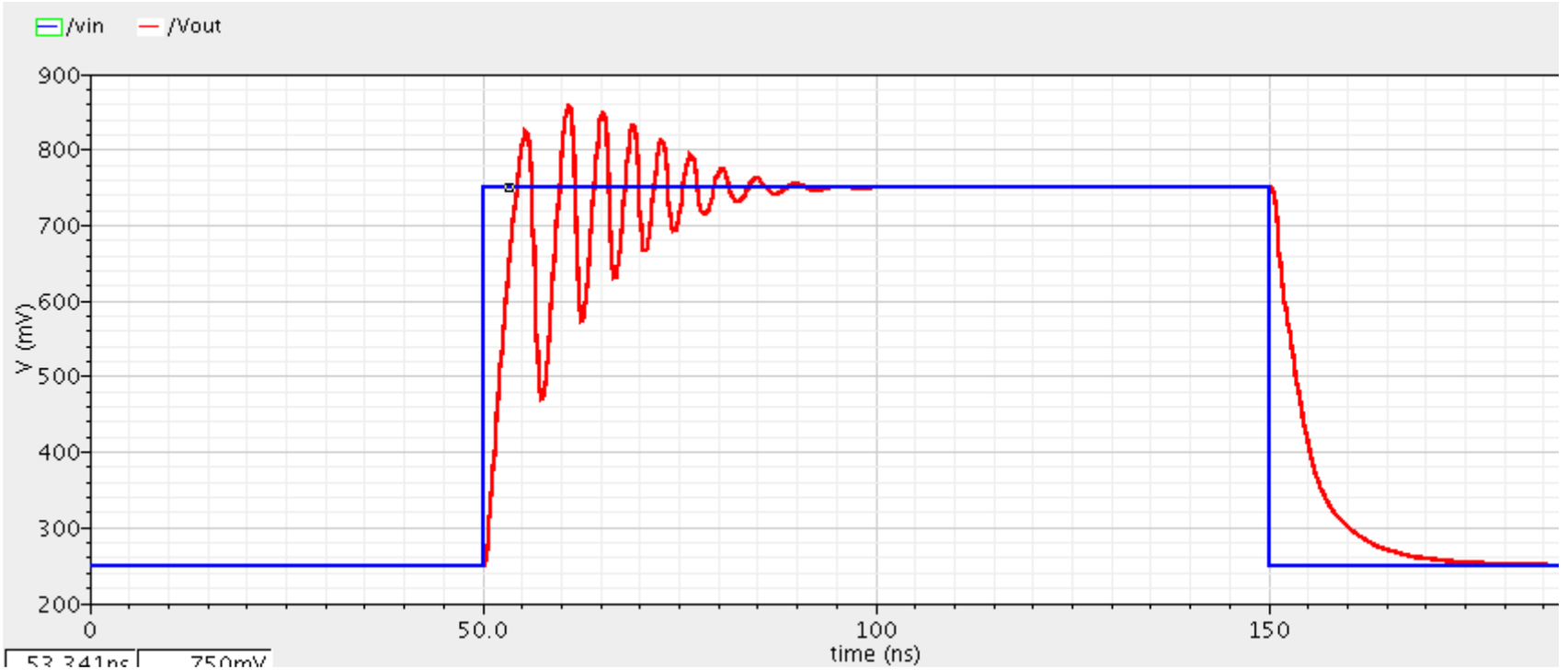
Small Step Response



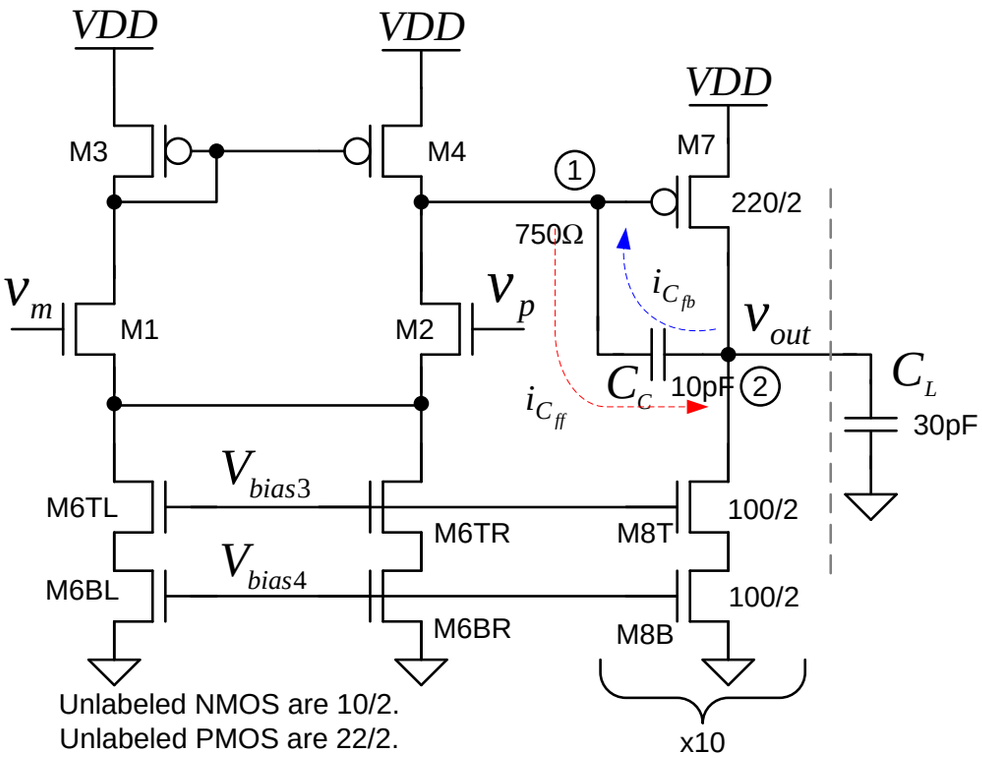
- Observe the ringing (PM was 41º)
  - Compensate more

Large Step Response



- Note the slewing in the output

Miller Compensation



- Compensation capacitor (C_c) between the output of the gain stages causes pole-splitting and achieves dominant pole compensation.
- An RHP zero exists at $z_1 = \frac{g_{m2}}{C_c}$
  - Due to feed-forward component of the compensation current (i_C).
- The second pole is located at $-\frac{g_{m2}}{C_1 + C_2}$
- The unity-gain frequency is $f_{un} = \frac{g_{m1}}{2\pi C_c}$
- A benign undershoot in step-response due to the RHP zero

❖All the op-amps presented have been designed in AMI C5N 0.5µm CMOS process with scale=0.3 µm and L_{min}=2. The op-amps drive a 30pF off-chip load offered by the test-setup.

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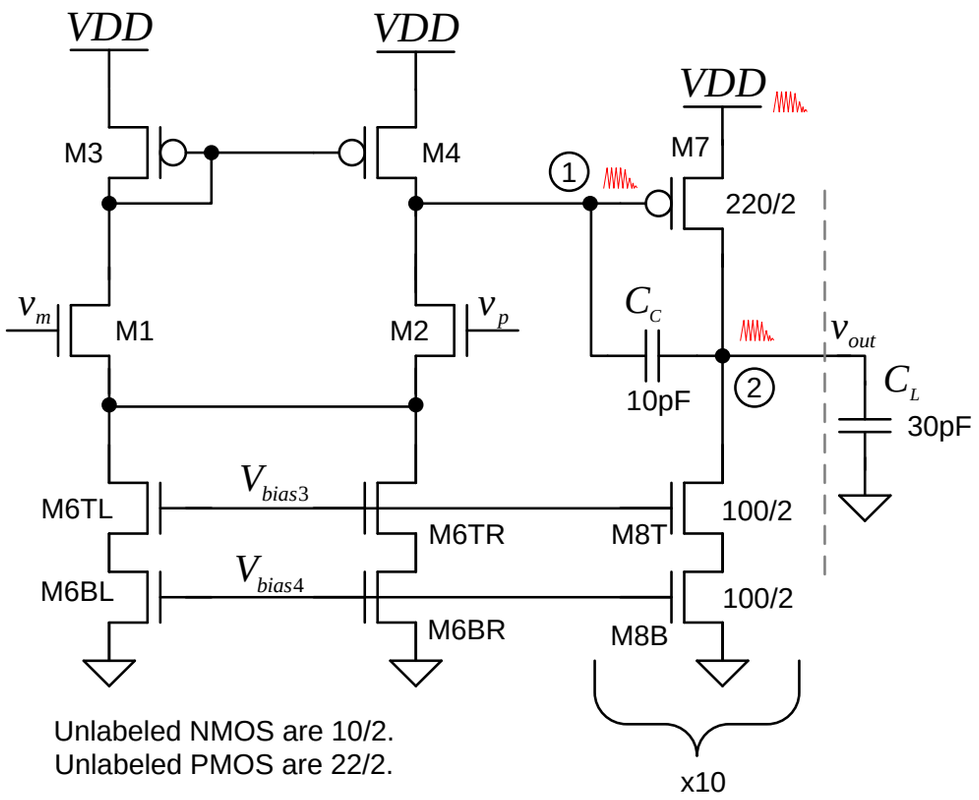
Drawbacks of Direct (Miller) Compensation



- The RHP zero decreases phase margin
  - Requires large C_C for compensation (10pF here for a 30pF load!).
- Slow-speed for a given load, C_L.
- Poor PSRR
  - Supply noise feeds to the output through C_C.
- Large layout size.

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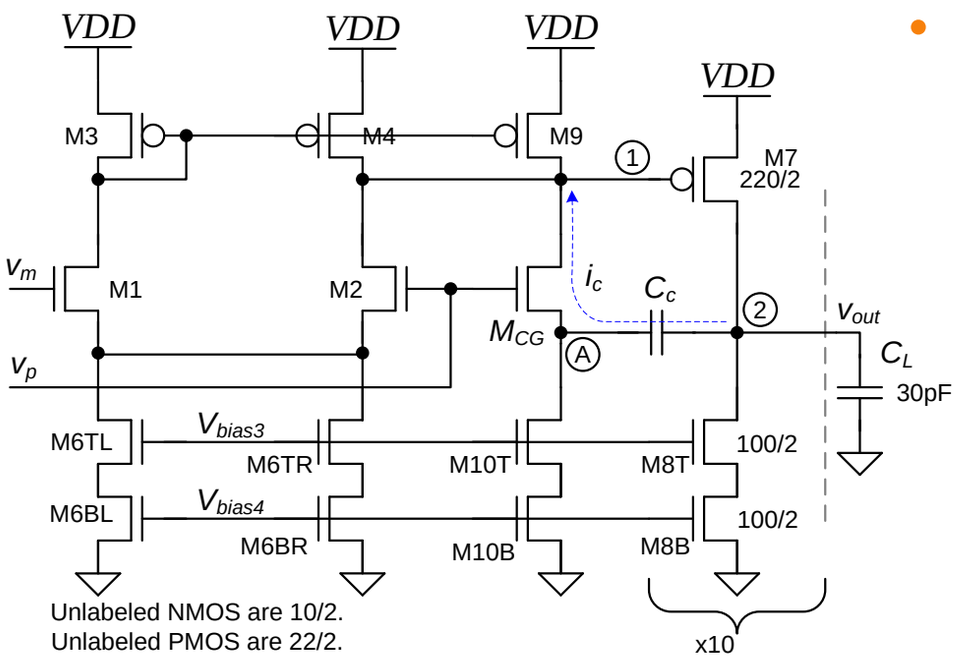
Indirect (or Ahuja) Compensation



An indirect-compensated op-amp using a common-gate stage.

- **The RHP zero can be eliminated by blocking the feed-forward compensation current component by using**
  - **A common gate stage,**
  - **A voltage buffer,**
  - **Common gate "embedded" in the cascode diff-amp, or**
  - **A current mirror buffer.**
- **Now, the compensation current is fed-back from the output to node-1 indirectly through a low-Z node-A.**
- **Since node-1 is not loaded by C_C, this results in higher unity-gain frequency (f_{un}).**

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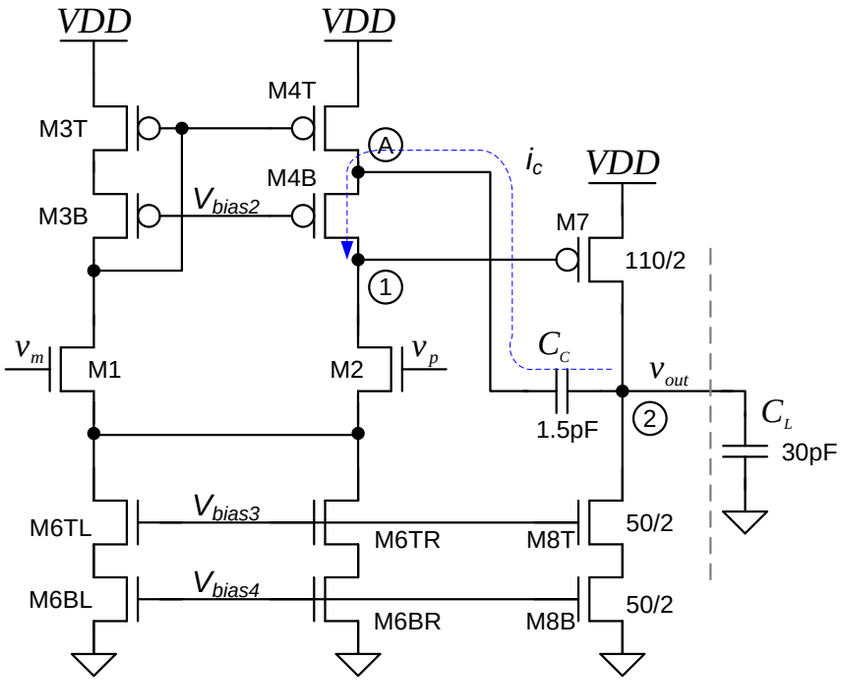
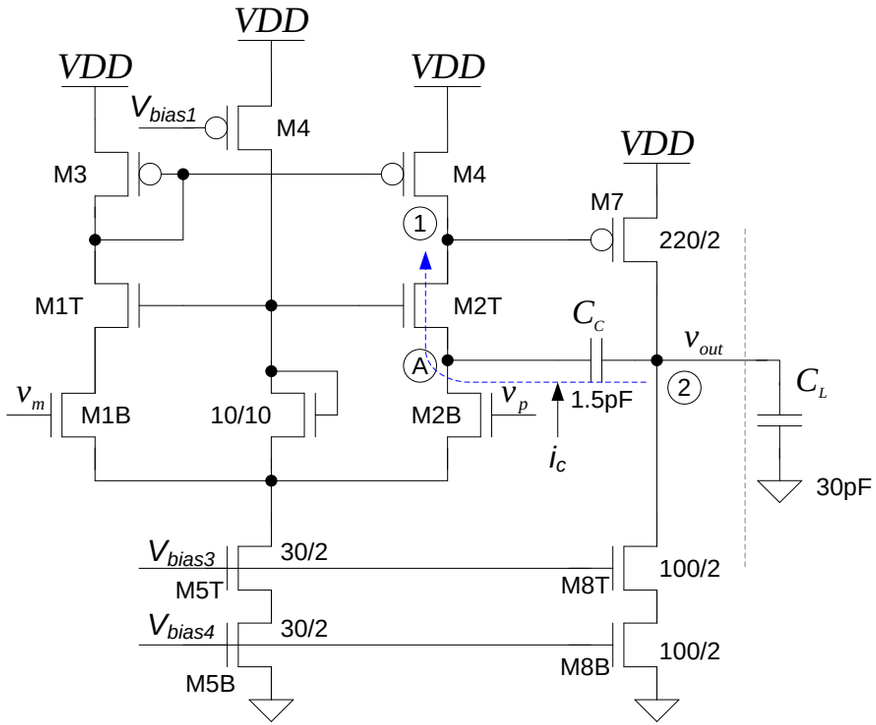
Indirect Compensation in a Cascoded Op-amp



Unlabeled NMOS are 10/2.
Unlabeled PMOS are 44/2.

Indirect-compensation using cascoded current mirror load.



Unlabeled NMOS are 10/2.
Unlabeled PMOS are 22/2.

Indirect-compensation using cascoded diff-pair.

- Employing the common gate device "embedded" in the cascode structure for indirect compensation avoids a separate buffer stage.
  - ✓ Lower power consumption.
  - ✓ Also voltage buffer reduces the swing which is avoided here.

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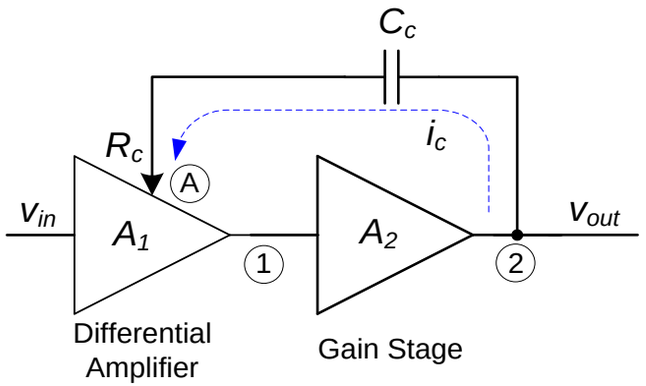
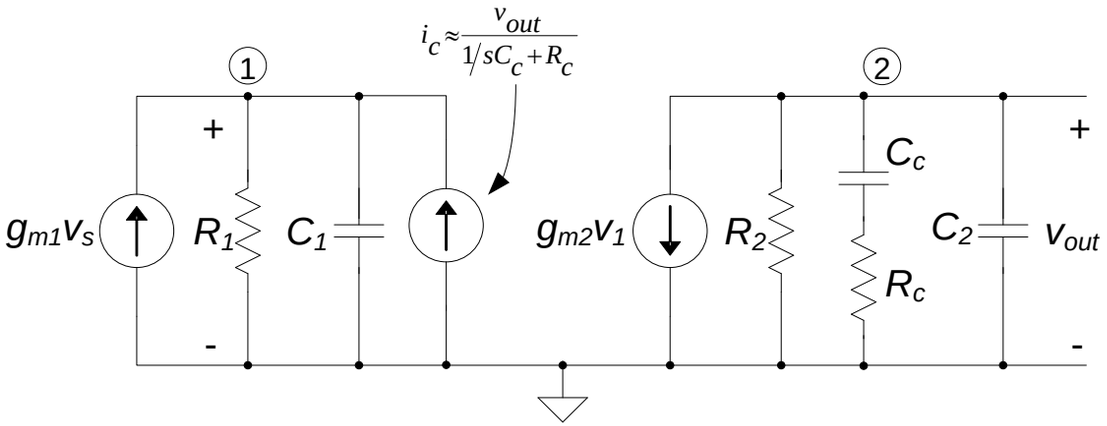
Analytical Modeling of Indirect Compensation



Block Diagram

The compensation current (i_C) is indirectly fed-back to node-1.



Small signal analytical model

R_C is the resistance attached to node-A.

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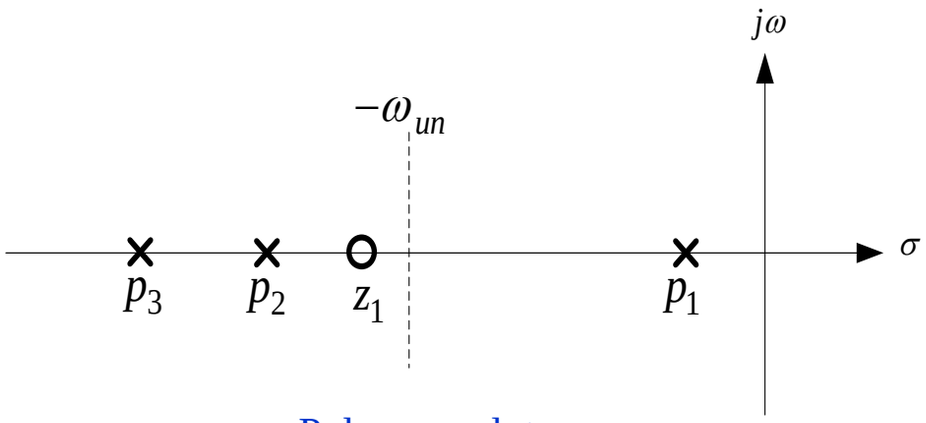
Analytical Results for Indirect Compensation



Pole-zero plot

- Pole p_2 is much farther away from f_{un}.
  - ✓ Can use smaller g_{m2}=>less power!
- LHP zero improves phase margin.
- Much faster op-amp with lower power and smaller C_C.
- Better slew rate as C_C is smaller.

$$\frac{v_{out}}{v_s} = -A_v\left(\frac{1+b_1 s}{1+a_1 s+a_2 s^2+a_3 s^3}\right)$$

$$z_1 \approx -\frac{1}{R_c C_c} \quad \text{LHP zero}$$

$$p_1 \approx -\frac{1}{a_1} = -\frac{1}{g_{m2}R_2R_1C_c}$$

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2}R_1C_c}{C_2(R_cC_c+R_1C_1)} \approx -\frac{g_{m2}C_c}{C_LC_1}$$

$$p_3 \approx -\frac{a_2}{a_3} = -\left[\frac{1}{R_cC_c}+\frac{1}{R_1C_1}\right]$$

$$f_{un} = \frac{|p_1|A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_c}$$

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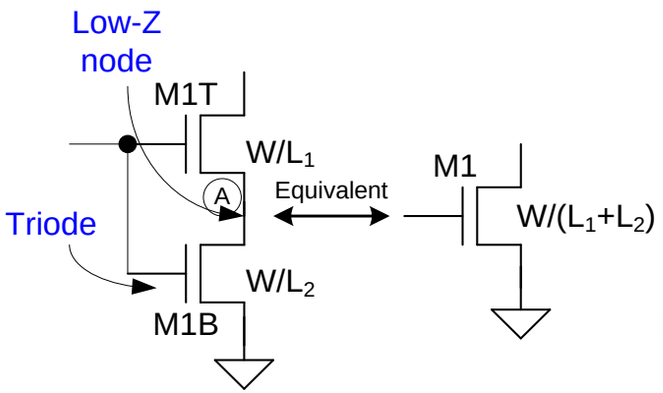
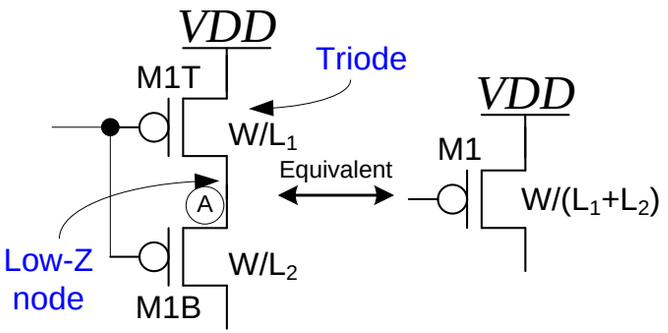
Indirect Compensation Using Split-Length Devices

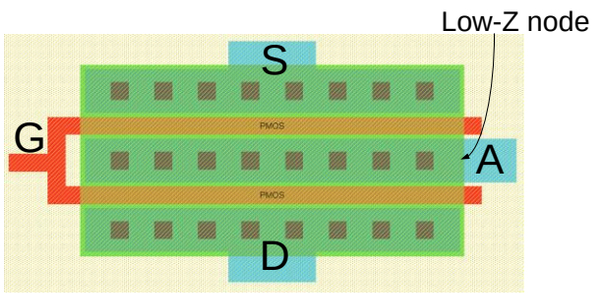
- As VDD scales down, cascoding is becoming tough. Then how to realize indirect compensation as we have no low-Z node available?
- Solution: Employ split-length devices to create a low-Z node.
  - Creates a pseudo-cascode stack but its really a single device.
- In the NMOS case, the lower device is always in triode hence node-A is a low-Z node. Similarly for the PMOS, node-A is low-Z.



NMOS



PMOS



Split-length 44/4(=22/2) PMOS layout

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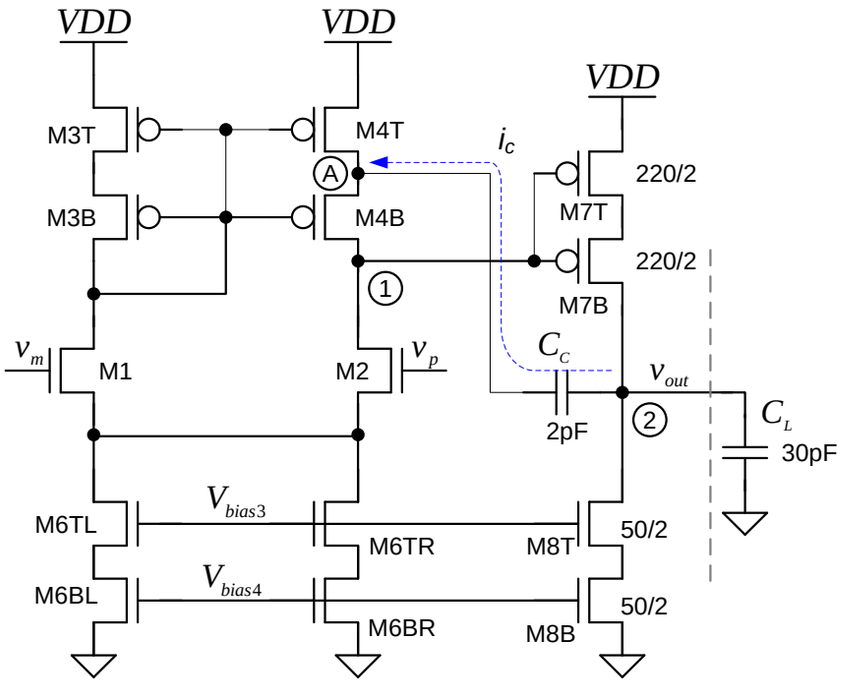
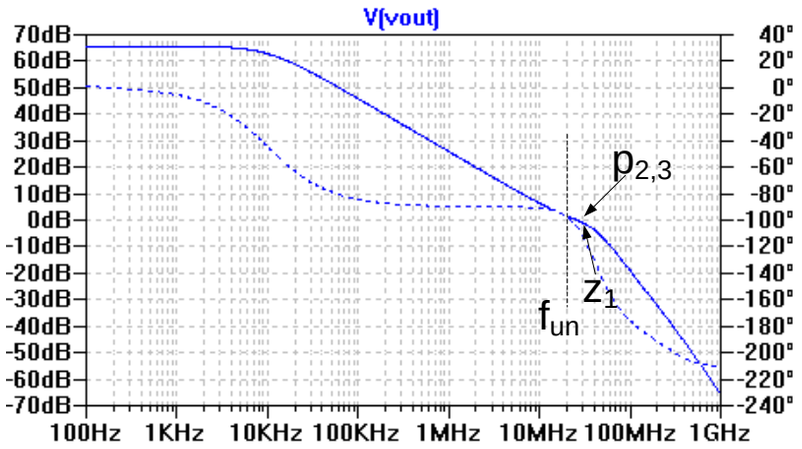
Split-Length Current Mirror Load (SLCL) Op-amp

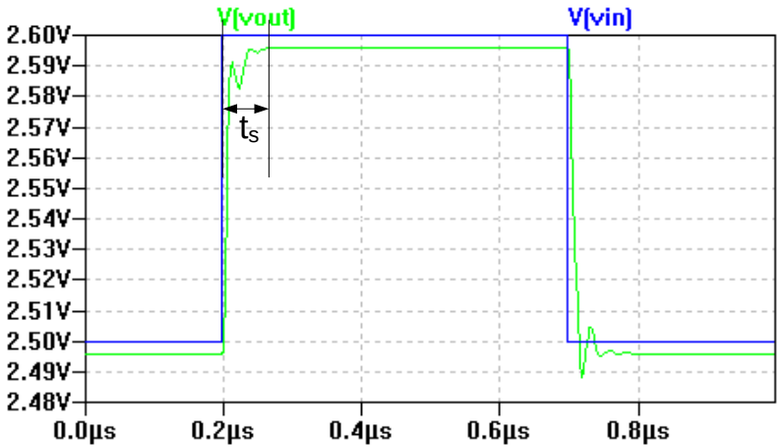


Unlabeled NMOS are 10/2.
Unlabeled PMOS are 22/2.

- The current mirror load devices are split-length to create low-Z node-A.
- Here, f_{un}=20MHz, PM=75° and t_s=60ns.



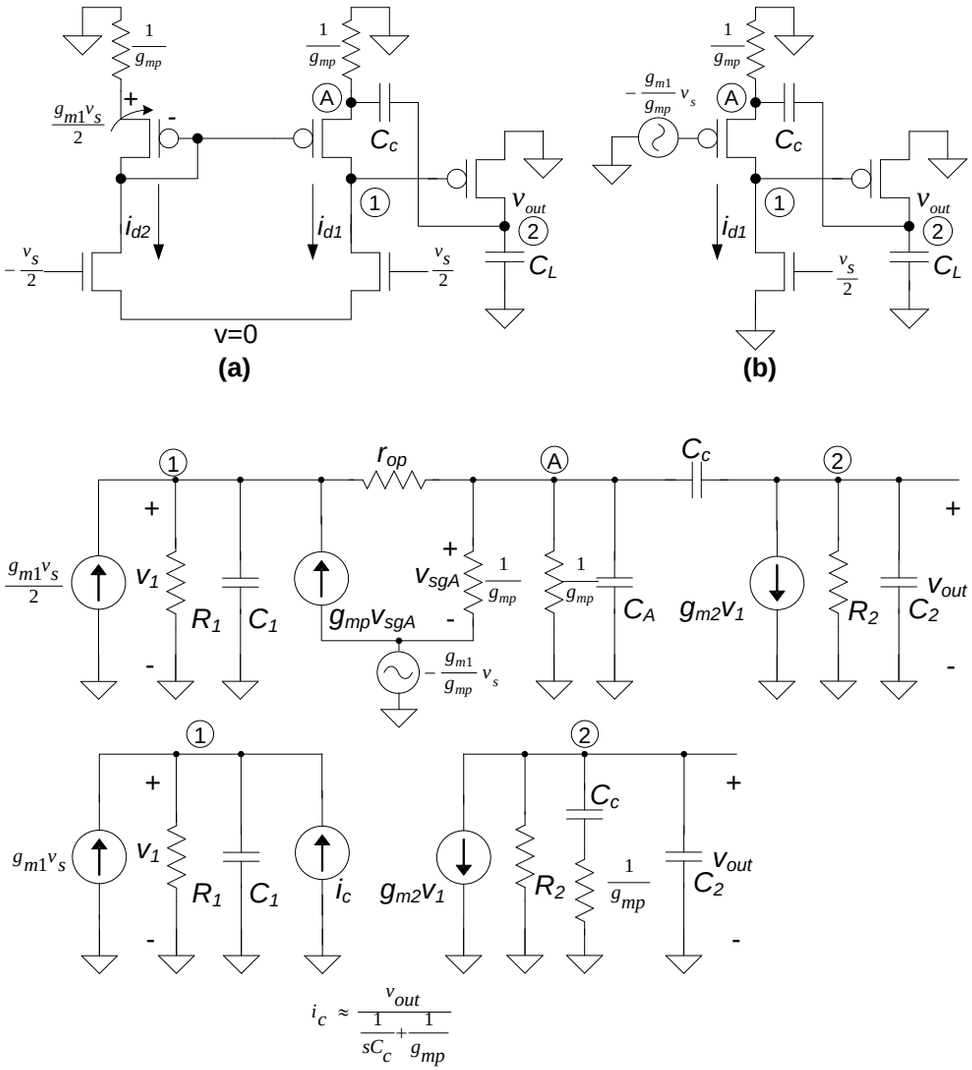
Frequency Response



Small step-input settling in follower configuration

Saxena

SLCL Op-amp Analysis



$$f_{un} = \frac{g_{m1}}{2\pi(2C_c)}$$

$$p_1 \approx -\frac{1}{2g_{m2}R_2R_1C_c}$$

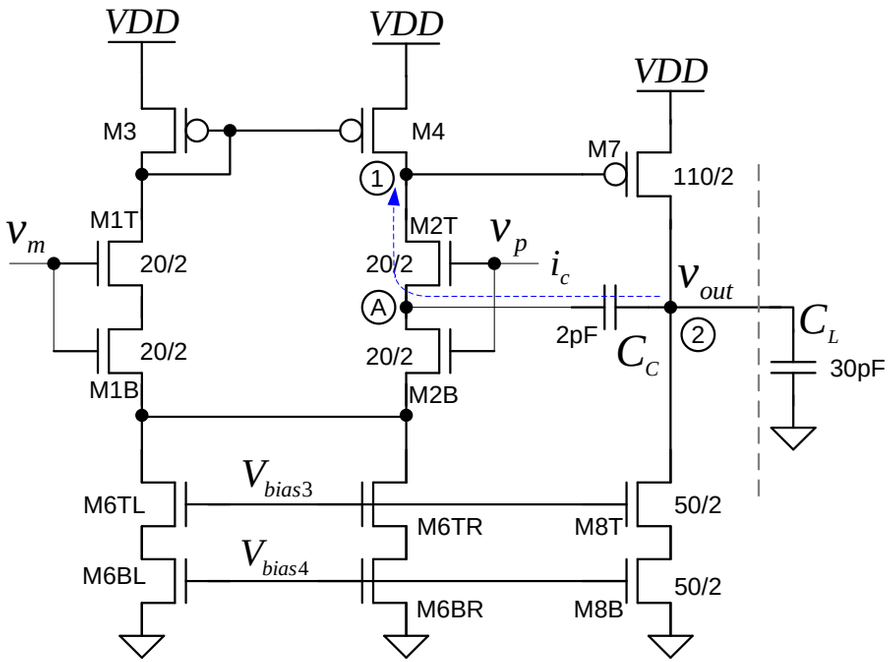
$$\left|Re(p_{2,3})\right| = \frac{g_{m2}}{C_L}\sqrt{\frac{g_{mp}C_L}{g_{m2}C_1}}$$

$$z_1 \approx -\frac{4g_{mp}}{3(C_c+C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_c+C_A)} \approx \frac{8\sqrt{2}}{3}\omega_{un}$$

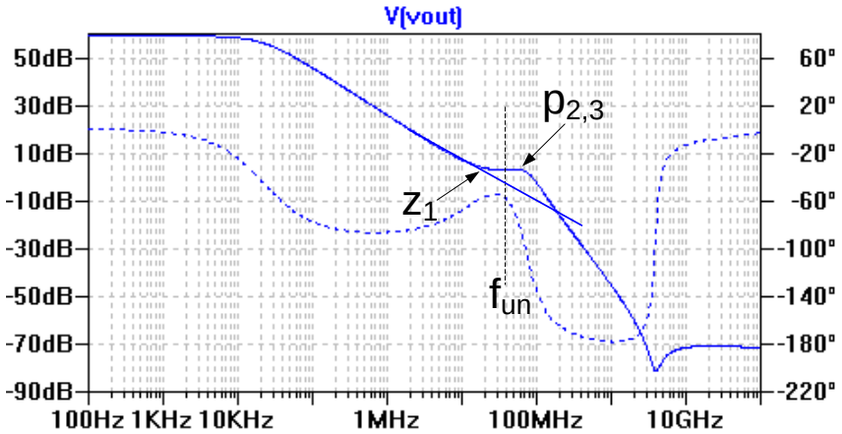
- Here $f_{z1}=3.77f_{un}$
  - ✓ LHP zero appears at a higher frequency than f_{un}.

Saxena

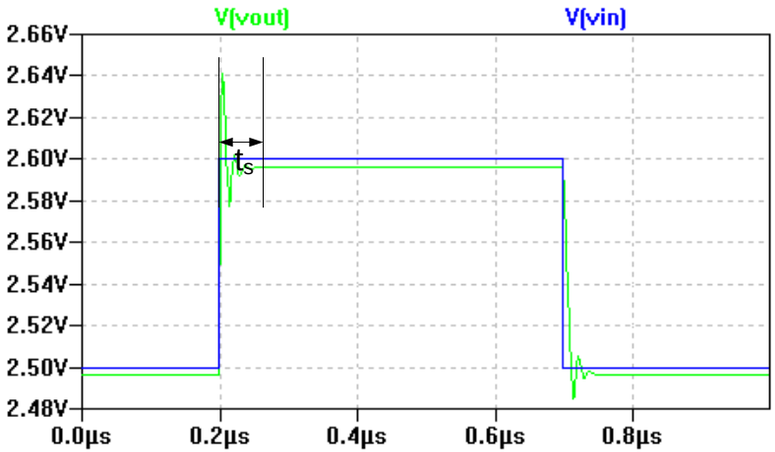
Split-Length Diff-Pair (SLDP) Op-amp



Unlabeled NMOS are 10/2.
Unlabeled PMOS are 22/2.



Frequency Response

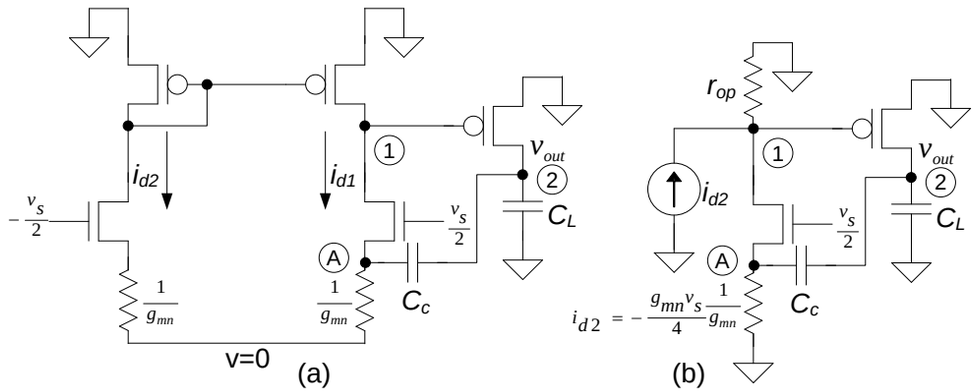


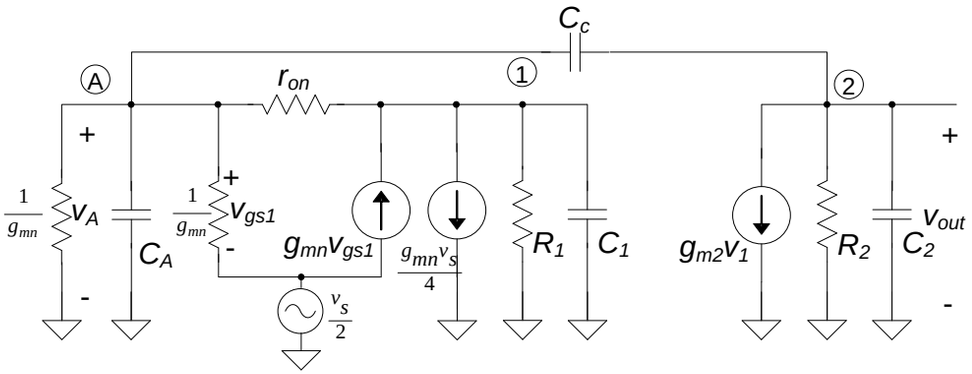
Small step-input settling in follower configuration

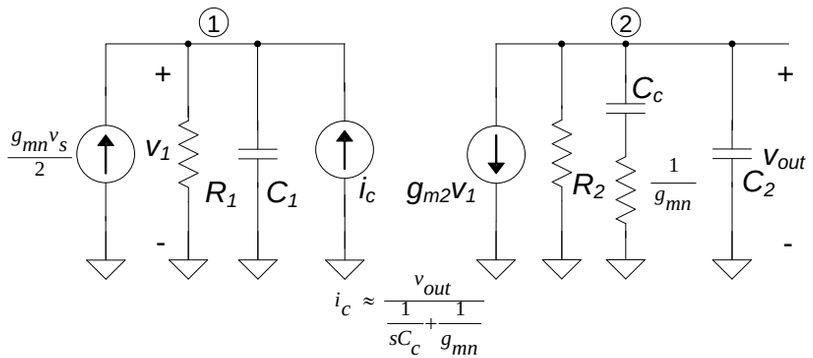
- The diff-pair devices are split-length to create low-Z node-A.
- Here, f_{un}=35MHz, PM=62°, t_s=75ns.
- Better PSRR due to isolation of node-A from the supply rails.

Saxena

SLDP Op-amp Analysis







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$$f_{un} = \frac{2g_{m1}}{2\pi C_c}$$

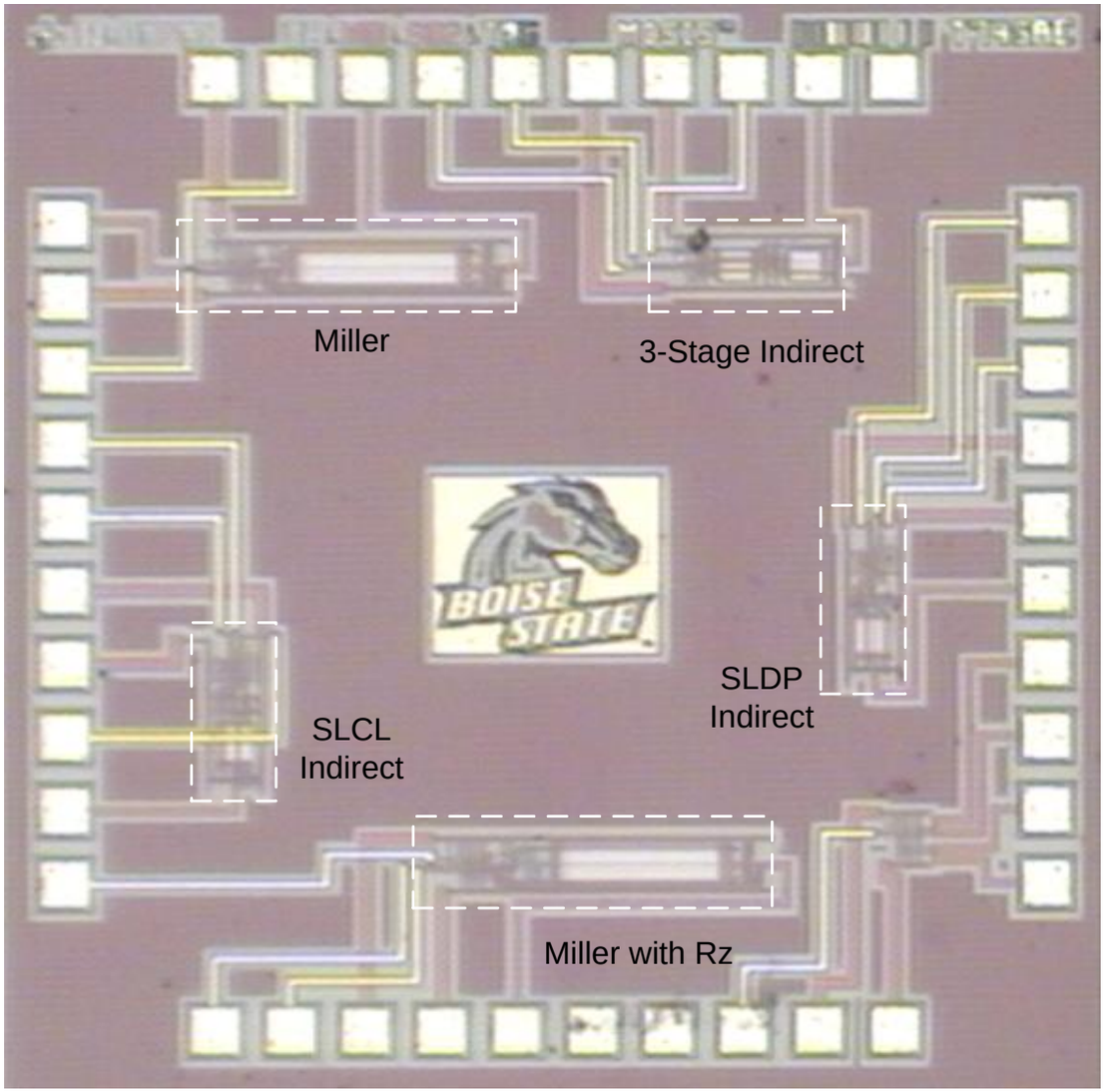
$$p_1 \approx -\frac{2}{g_{m2}R_2R_1C_c}$$

$$\left|Re(p_{2,3})\right| = \frac{g_{m2}}{C_L}\sqrt{\frac{g_{mp}C_L}{g_{m2}C_1}}$$

$$z_1 \approx -\frac{4g_{mn}}{3(C_c+C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_c+C_A)} \approx \frac{2\sqrt{2}}{3}\omega_{un}$$

- Here $f_{z1}=0.94f_{un}$,
  - ✓ LHP zero appears slightly before f_{un} and flattens the magnitude response.
  - ✓ This may degrade the phase margin.
- Not as good as SLCL, but is of great utility in multi-stage op-amp design due to higher PSRR.

Test Chip 1: Two-stage Op-amps



- AMI C5N 0.5µm CMOS, 1.5mmX1.5mm die size.

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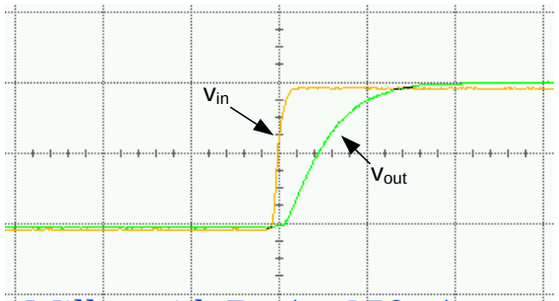
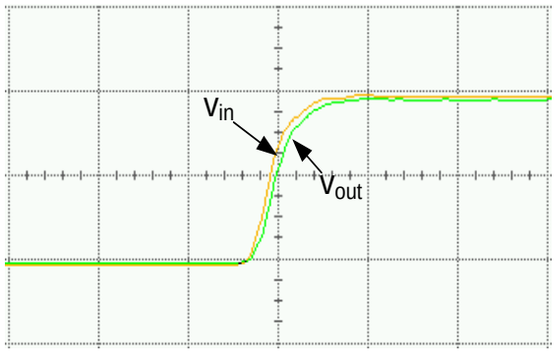
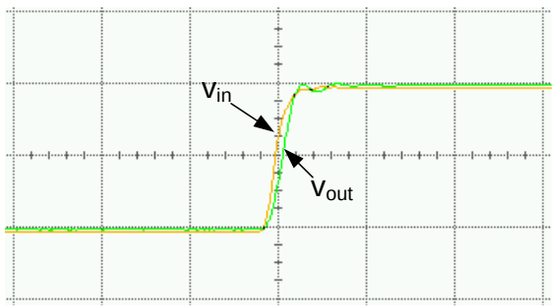
.Test Results and Performance Comparison



Miller with Rz (t_s=250ns)



SLCL Indirect (t_s=60ns)



SLDP Indirect (t_s=75ns)

Performance comparison of the op-amps for C_L=30pF.

Op-amp Topology	A_{DC} (dB)	f_{un} (MHz)	C_C (pF)	PM	t_s (ns)	Power (mW)	Layout area (mm^2)
Miller	57	2.5	10	74°	270	1.2	0.031
Miller with R_Z	57	2.7	10	85°	250	1.2	0.034
SLCL (this work)	66	20	2	75°	60	0.7	0.015
SLDP (this work)	60	35	2	62°	75	0.7	0.015

- 10X gain bandwidth (f_{un}).
- 4X faster settling time.
- 55% smaller layout area.
- 40% less power consumption.

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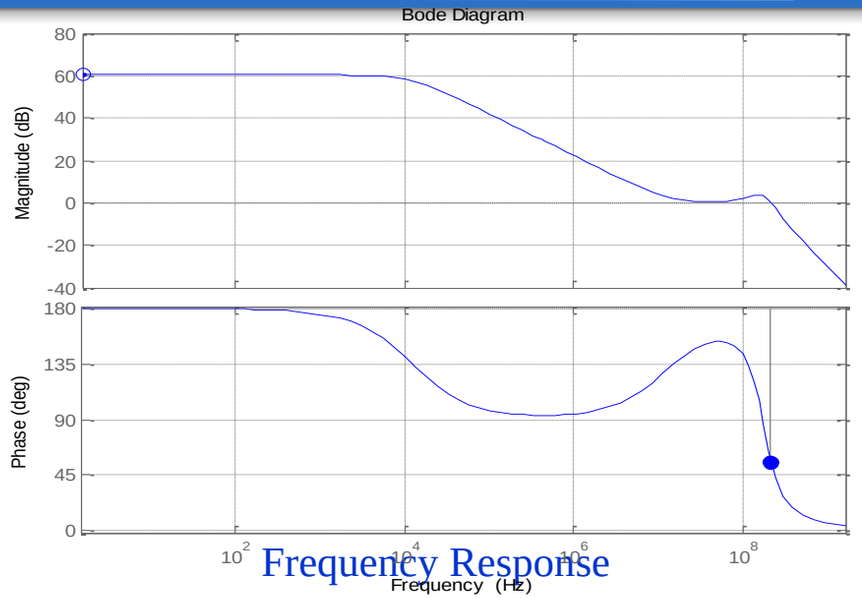
Effect of LHP-zero on Settling

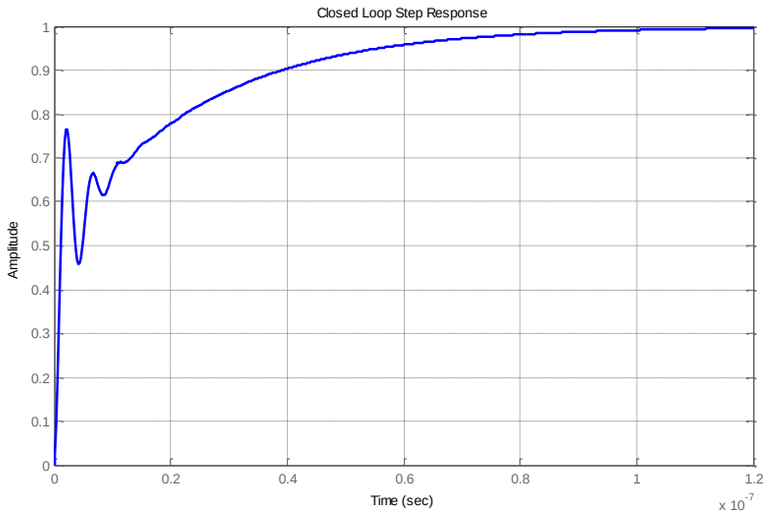
- In certain cases with indirect compensation, the LHP-zero ($\omega_{z,LHP}$) shows up near f_{un}.
  - ✓ Causes gain flattening and degrades PM
  - ✓ Hard to push out due to topology restrictions
- Ringing in closed-loop step response
  - ✓ This ringing is uncharacteristic of the 2nd order system.
  - ✓ Used to be a benign undershoot with the RHP zero, here it can be pesky
  - ✓ Is this settling behavior acceptable?
- Watch out for the $\omega_{z,LHP}$ for clean settling behavior!

Caveat:

- **When using indirect compensation be aware of the LHP-zero induced transient settling issues**



Frequency Response



Small step-input settling in follower configuration

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References

[1] Spectre User Simulation Guide, pages 160-165

http://www.designers-guide.org/Forum/YaBB.pl?num=1170321868

[2] M. Tian, V. Viswanathan, J. Hangtan, K. Kundert, “Striving for Small-Signal Stability: Loop-based and Device-based Algorithms for Stability Analysis of Linear Analog Circuits in the Frequency Domain,” Circuits and Devices, Jan 2001.

http://www.kenkundert.com/docs/cd2001-01.pdf

[3] https://secure.engr.oregonstate.edu/wiki/ams/index.php/Spectre/STB