Homework 5

ECE 5/411 – CMOS Analog IC Design (Spring 2014)

Due on Tuesday, March 4, 2014.

Note:
1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.
2. Use the 1 μm CMOS parameters from Table 1 posted on the site, along with the corresponding Spectre models.

Problem 1: The beta-multiplier references (BMR) are used for constant-g_m biasing, where the goal is to stabilize the transconductance of a transistor. For example, in Fig. 1 (a), the g_m of M1 will be 'copied' to a current mirror device (not shown here).

a) Derive expressions for I_{ref}, V_{GS_1} and g_{m1} in Fig. 1 (a). Note that M3 is K times wider than M4 and M1 and M2 are the same size. Draw the schematic for a start-up circuit for this BMR.

b) Will the circuit shown in Fig. 1 (b) work as a constant-g_m reference? Explain.

c) Fig. 1 (c) shows a fix for the body effect problem in the bottom NMOS in the BMR. Derive an equation for I_{ref} in this circuit. Run a temperature sweep on I_{ref} and compare it with the results from the BMR seen in class. Explain your observations.

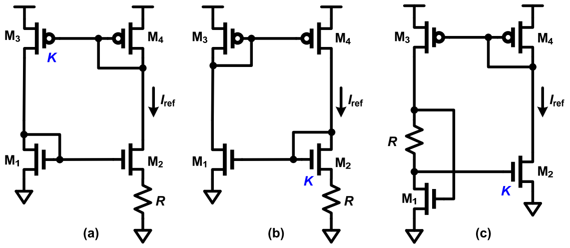

Figure 1

Problem 2: Consider the PMOS-version of the regulated drain current mirror shown in Fig 2.

a) Find expressions (in terms of V_{THN} and $V_{DS,sat}$) for all the DC levels in the circuit.

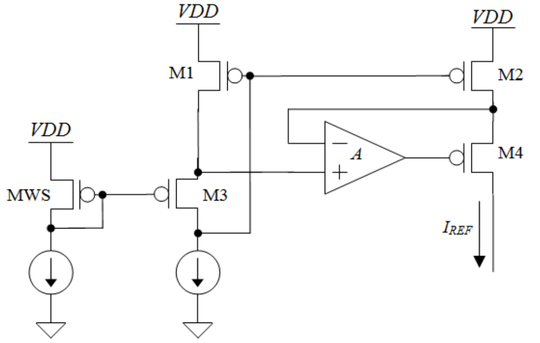

Figure 2

b) Estimate the small-signal output resistance, R_o, of the current mirror.

c) What the allowed swing across the current mirror, to ensure all transistors are in saturation?

Problem 3: The concept of cascoding can be further extended to realize a *triple-cascode* current mirror as shown below.

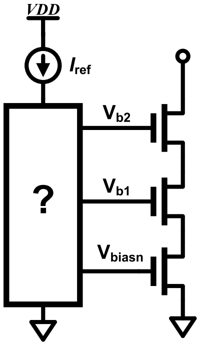

Figure 3

a) Assuming all devices to be identical, find an expression for the output resistance of this double-cascode current mirror? What are the trade-offs involved if double-cascoding is used in designs?

b) Given an ideal reference (I_{ref}) and using long-channel equations, design a wide-swing double-cascode current mirror such that the minimum allowed output voltage is $3V_{DS,sat}$. Neatly show the schematics and the steps for calculating the sizes of the long-length devices used in the design.

Problem 4: Using the 180nm CMOS process and the characterization data from HW3, design and simulate:

a) A beta-multiplier current reference (BMR) as seen in Fig. 20.18 in the CMOS textbook. Plot the currents in the BMR when V_{DD} is swept. Comment on the supply sensitivity of the circuit.

b) Repeat part (a), by using an ideal amplifier to regulate the drain voltages of the bottom NMOS devices in the BMR.

c) Replace the ideal amplifier model by a transistor-level self-biased amplifier as in CMOS book Fig. 20.22. Simulate and comment on the supply sensitivity of this circuit. Apply a step input to V_{DD} and plot the response to verify the stability of the circuit.