

Homework 2

ECE 5/411 – CMOS Analog IC Design (Spring 2014)

Due on Tuesday, Feb 4, 2014.

Note:

1. Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.
2. Use the following $1\mu\text{m}$ CMOS parameters and corresponding spectre models.

Table 1: Long-channel MOSFET parameters.

Parameter	NMOS	PMOS
Scale factor (L_{min})	$1\mu\text{m}$	
V_{DD}	5 V	
V_{THN} and V_{THP}	0.8	0.9
KP_n and KP_p	$120 \frac{\mu\text{A}}{\text{V}^2}$	$40 \frac{\mu\text{A}}{\text{V}^2}$
$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$	$1.75 \frac{\text{fF}}{\mu\text{m}^2}$	

Problem 1: For the circuit shown in Figure 1, sketch I_x as V_x varies from 0 to $V_{DD} = 5\text{ V}$. Not required, but feel free to verify using simulations.

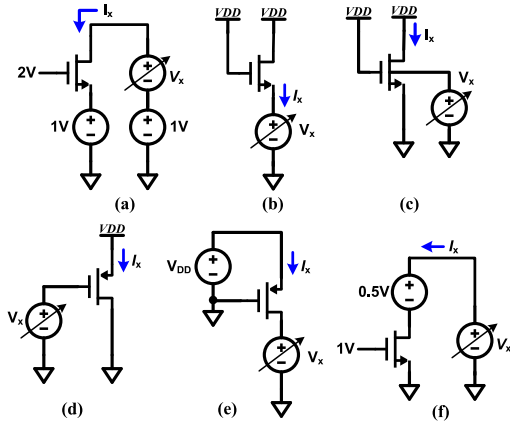


Figure 1

Problem 2: Using square law equations for a MOSFET, determine the DC voltage, V_x , in each of the circuits shown in Figure 2. Verify your calculations with simulations.

Problem 3: For the circuit shown in Figure 3(a), determine the minimum value of I required to make the NMOS operate at the edge of the saturation region. In the circuit (b), determine

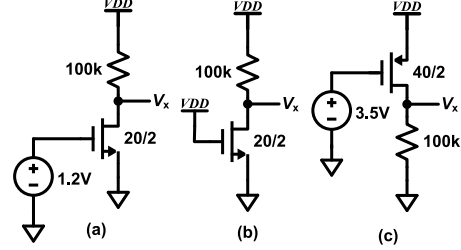


Figure 2

the small-signal voltage v_2 , in terms of the small-signal current i (assuming saturation). How will you choose R to make v_2 independent of i .

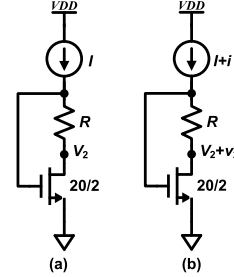


Figure 3