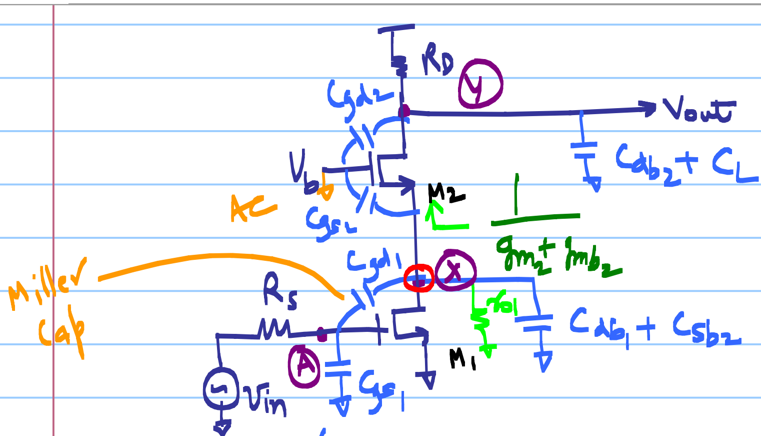
Note Title 3/21/2013

ECE 511 - Lecture 17

Cascode Amplifier



$$A_v = -g_{m_1} \cdot \left(R_D \| \underbrace{g_{m_2} r_{o_2} r_{o_1}}_{g_m r_o^2} \right)$$

Miller effect of C_{gd_1}

* gain from A to X

(Assume $R_D \ll r_o$)

$$A_{A \to X} = -g_{m_1} \cdot \frac{1}{g_{m_2} + g_{mb}} = -1$$

$M_1 \triangleq M_2$

$\gamma = 0$

$C_{in} = 2 \cdot C_{gd_1}$

↳ Miller effect is less significant in cascode amplifiers than a CS stage

Pole @ A:

$$\omega_{pA} = \frac{1}{R_s\left[C_{gs_1} + \left(1 + \frac{g_{m_1}}{g_{m_2} + g_{mb_2}}\right) C_{gd_1}\right]}$$

$\rightarrow |A_v|$ for $A \rightarrow X$

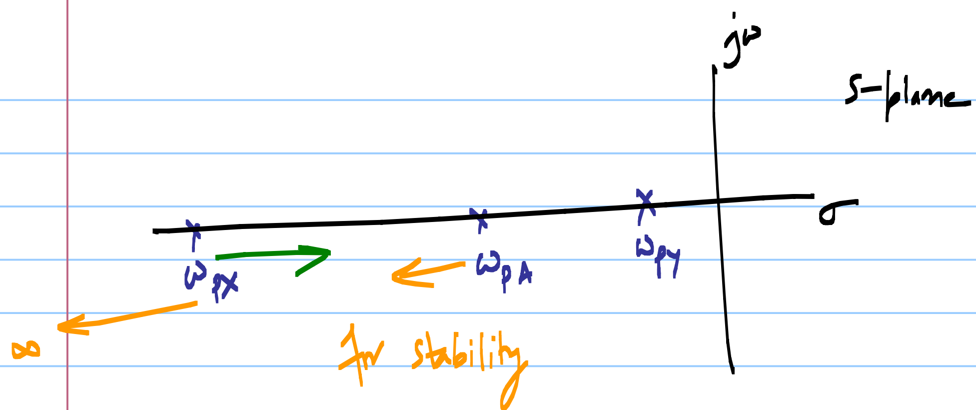
Pole @ X:

$$\omega_{px} = \frac{1}{R_x \cdot C_x} = \frac{(g_{m_2} + g_{mb_2})}{2C_{gd_1} + C_{db_1} + C_{sb_2} + C_{gs_2}}$$

$\left(1 + \frac{1}{|A|}\right) C_c$

Pole @ Y:

$$\omega_{py} = \frac{1}{R_D\,(C_{db_2} + C_{gd_2} + C_L)}$$



Choose ω_{px} to be farther away from the other two poles.

* What if R_D is replaced by a cascode current source load.

$$A_V = -g_{m1}\left[(g_m r_o^2)_n \,\|\, (g_m r_o^2)_p \right] \leftarrow \text{higher DC gain}$$

$\Rightarrow$ impedance at node 'X' $\Rightarrow r_{o1} \,\|\, \left[\frac{R_D}{(g_m r_o)_n} \right]$

↳ pole at X moves closer

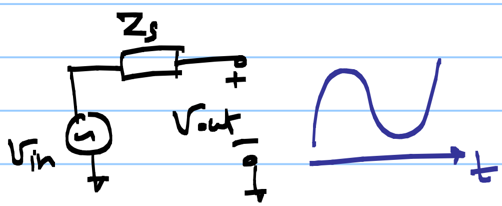
$$= r_{o1} \,\|\, \frac{(g_m r_o^2)_p}{(g_m r_o)_n} \approx \frac{r_o}{2}$$

$\frac{1}{g_{m2}} \rightarrow \frac{r_o}{2}$

* But, in practice this pole doesn't degrade stability much.

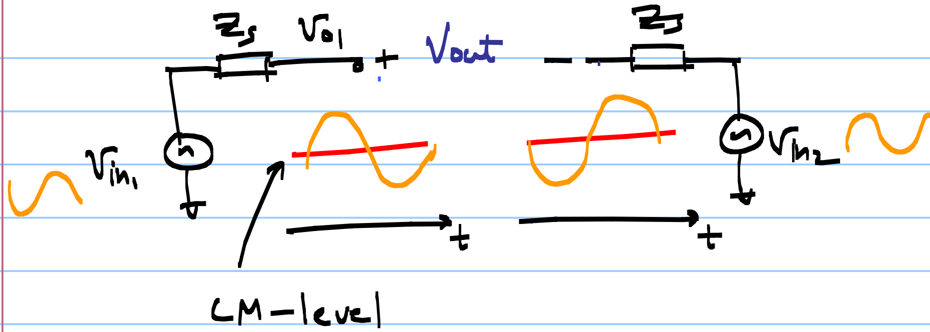
Differential Amplifier:

* Single-ended signal is defined as one that is measured w.r.t. a fixed potential → usually ground



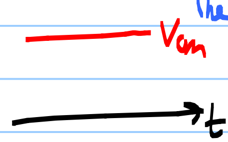
* A differential signal is defined as one measured between two nodes that have equal and opposite signal excursions around a fixed potential

$V_{out} = V_{o1} - V_{o2}$

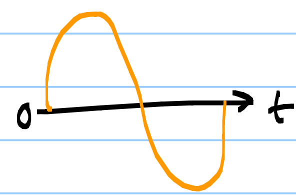


The center potential in differential signalling is called the "common-mode" level

Common mode → $V_{cm} = \frac{V_{o1} + V_{o2}}{2}$

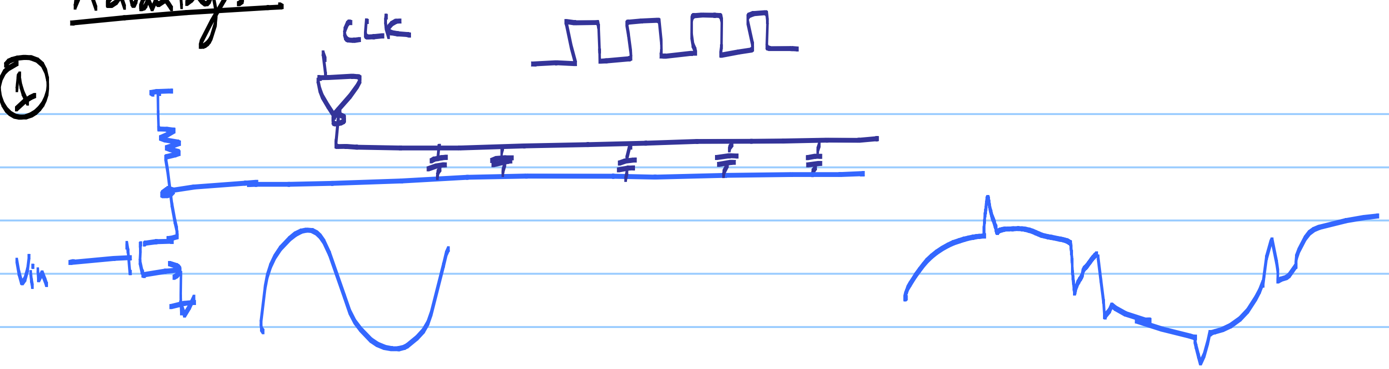


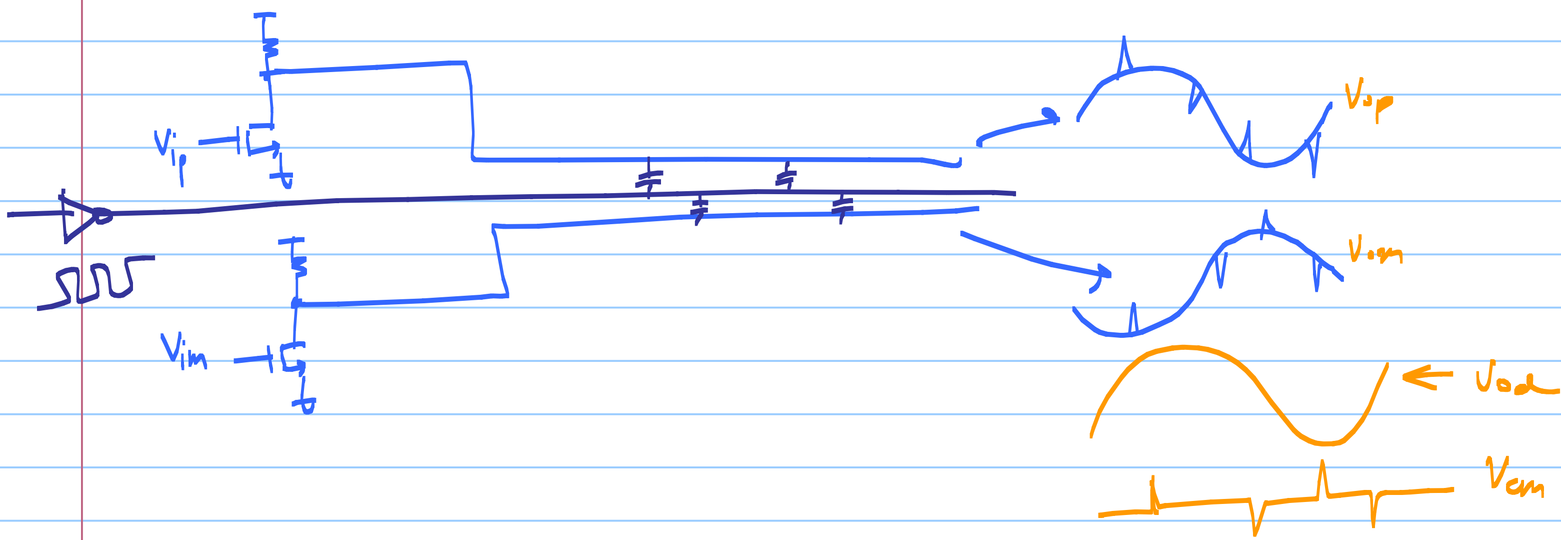
Differential → $V_d = (V_{o1} - V_{o2})$



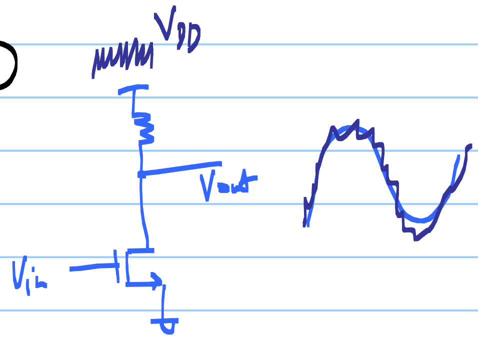
Advantages:

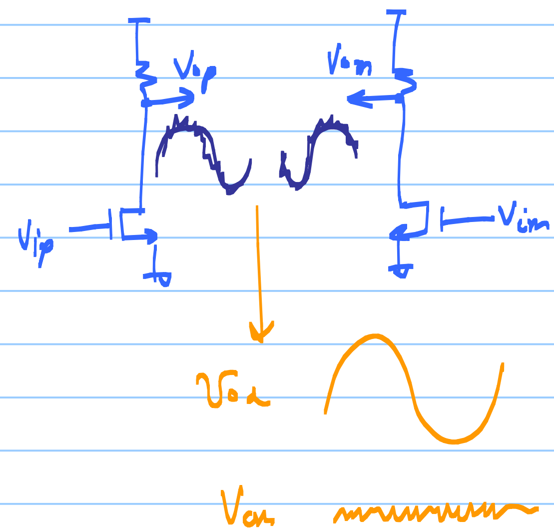
①





⇒ Differential signalling rejects "common-mode noise".

② 



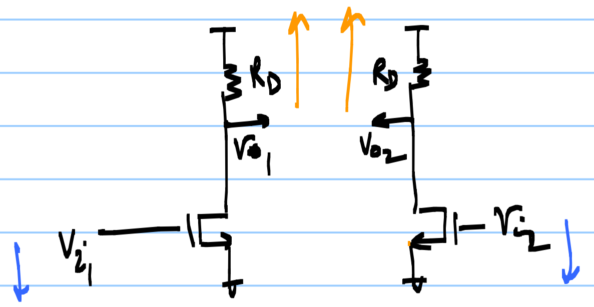
Better "PSRR"
power supply rejection

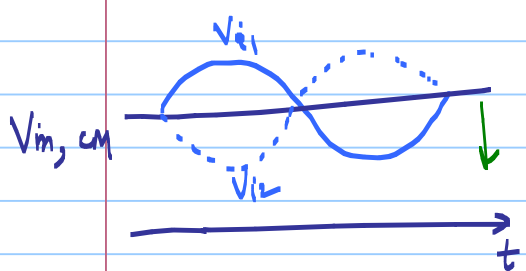
③ Simple biasing

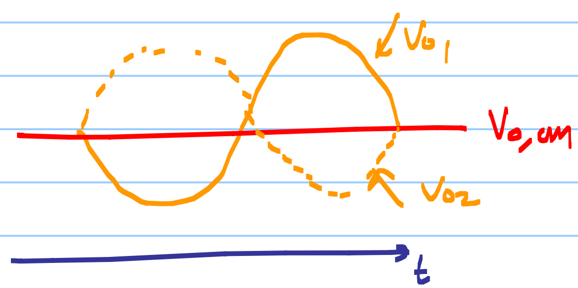
(−) 2X Area
↳ not an issue

Basic Diff-pair

2 - identical SE signal paths to process both phases



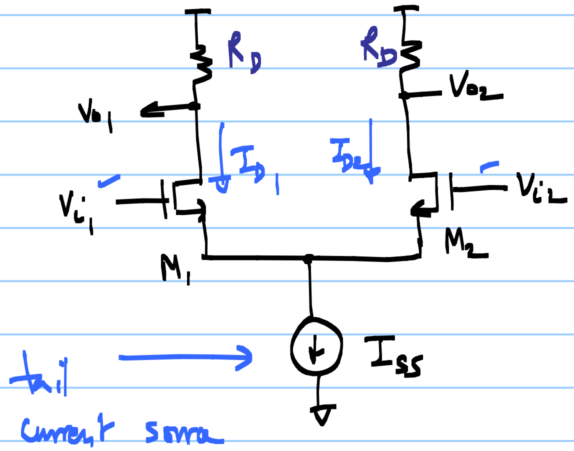


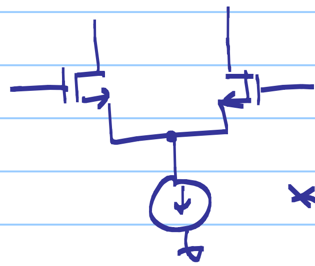


* What if is $V_{in,CM}$ is not well defined

Bad ⇒ bias current in both the halves are dependent on $V_{in,cm}$.

↳ Need the diff-pair bias current to be independent of the input CM-level.





× Basic Differential pair

In DC picture

$$I_{D_1} = I_{D_2} = \frac{I_{SS}}{2}$$

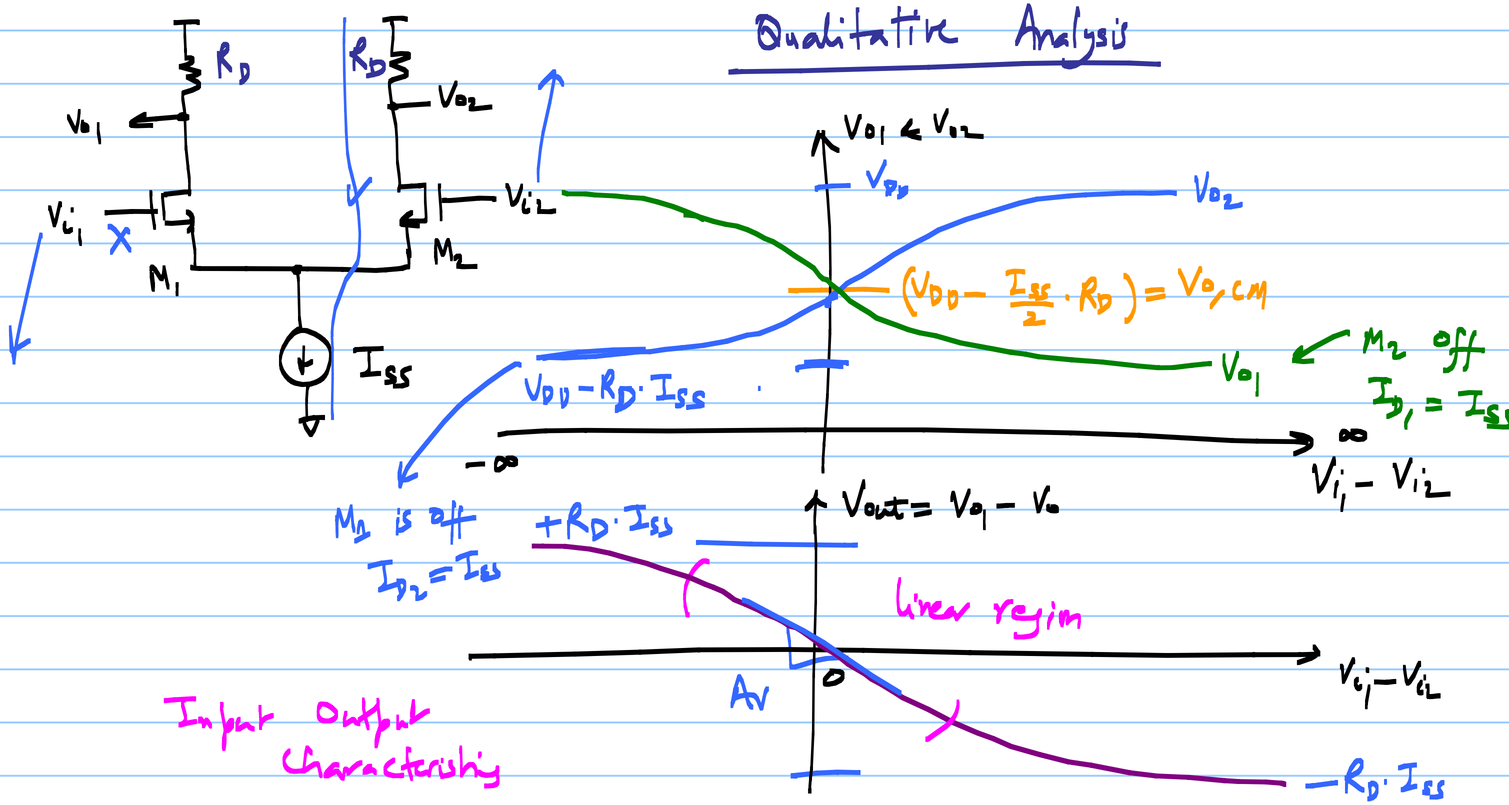
$$\boxed{I_{SS} = I_{D_1} + I_{D_2}}$$ independent of $V_{in,cm}$

× If $V_{i_1} = V_{i_2} = V_{in,cm} \Rightarrow$ bias current in each device $= \left(\frac{I_{SS}}{2}\right)$

$$V_{out,cm} = V_{DD} - \frac{I_{SS}}{2} R_D$$

* DC biasing is simplified

Qualitative Analysis



* small signal gain $A_v = \dfrac{d(V_{o_1} - V_{o_2})}{d(V_{i_1} - V_{i_2})}$

Common-mode behavior of the circuit