Project 1

ECE 5/411 – CMOS Analog IC Design (Spring 2013)

Due on Wednesday, May 7, 2013.

1 Problem Statement

Design of a single-ended Opamp: Signal processing applications like Filters and ADCs require opamps with high performance and linearity. Typically analog signal processing employs fully-differential opamps. However, in this project a single-ended opamp has to be designed which satisfies the given specifications using TSMC 180-nm mixed-mode CMOS technology with a VDD=1.8 V supply voltage.

The target specifications for the singly-ended opamp are as follows:

Table 1: Opamp design specifications.

Parameter	**Specified Value**
Technology	TSMC 180n CMOS
Supply voltage, V_{DD}	1.8 V
Typical load	$100k\Omega \| \| 1pF$
Unit gain frequency (f_{un})	$> 100\,MHz$ *for ECE 411*
	$> 200\,MHz$ *for ECE 511*
Open-loop gain (A_{OL})	$> 70\,dB$
Slew-rate (SR)	$> 500\frac{V}{\mu s}$
Phase margin (ϕ_M)	$\gtrsim 63^\circ$
Power consumption	Minimum possible

2 Opamp Design

In your opamp design consider the following criterion:

1. Explore the opamp design space in the given technology. Select an appropriate topology which will meet the given specifications. *If you are not able to meet any of the specifications, explain giving justification.* You would want to have a class-AB output buffer to drive the given load with rail-to-rail output swing.

2. Characterize the process and explain the transistor size selection in your design. Show the biasing circuits with appropriate simulations.

3. Explain your opamp design choices and the various architectural trade-offs, e.g. Telescopic *vs* Folded-cascode, etc.

4. Pay special attention to the compensation scheme which will provide high-speed compensation with best possible slew-rate performance, e.g. Miller with zero-nulling R *vs* Indirect Cascode compensation *vs* Feed-forward compensation. Show necessary analysis, derivations and plots (pole-zero, root-locus, Bode, Nyquist etc.). I would like to see some MATLAB modeling.

5. Perform stability (***stb***) analysis in Spectre using the ***iprobe*** and plot the open-loop AC response [4]. Label the PM and GM values and comment on closed-loop stability. This is important!

6. Simulate the opamp in unity-gain feedback with step input and comment on the transient stability. Characterize the design for small as well as large step inputs. Label your settling times. Do you see any slewing? Argue why this method of determining stability will work for any feedback factor ($\beta \leq 1$).

7. Characterize your design for all metrics including *Slew-rate, CMRR, PSRR*, power consumption using appropriate test bench schematics [5].

8. Comment on the temperature behavior of the design for $0^\circ < T < 100^\circ C$.

3 Final Report

Submit your neatly typed report in a two-column IEEE transactions format [6]. Show crisply drawn schematics and block diagrams. You can download the Visio schematic symbols from the course website [7]. Provide relevant references in your report. Show the overall opamp performance in a neatly tabulated manner along with the conclusion.

4 Academic Honesty

You are expected to come up with your original designs. No circuits can be shared or copied from other student(s). Any instance of plagiarism will lead to an automatic zero grade on the project.

References

[1] N. Krishnapura, “Opamp analysis and performance summary” [Online]

[2] V. Saxena, and R.J. Baker, "Compensation of CMOS Op-Amps using Split-Length Transistors,", proceedings of the 51st Midwest Symposium on Circuits and Systems, pp. 109-112, August 10-13, 2008.

[3] B.K. Thandri, J. Silva-Martinez, "A robust feed-forward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," IEEE J. Solid-State Circuits, vol.38, no.2, pp. 237- 243, Feb 2003.

[4] Loop Stability Analysis [Online].

[5] “Functional Verification of a Differential Operational Amplifier,” Cadence Whitepaper [Online].

[6] IEEE Transactions Templates. Available [Online].

[7] Visio Schematic Symbols. Available [Online].