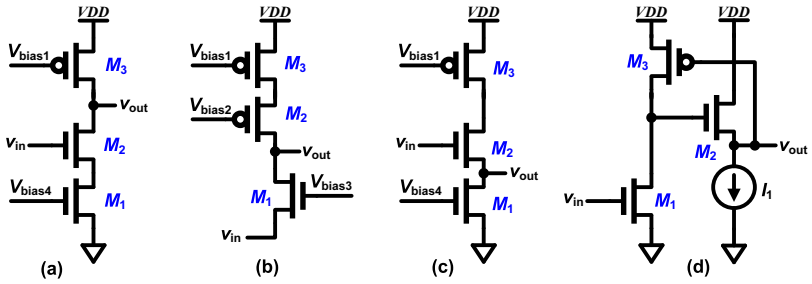
Homework 7

ECE 5411 – CMOS Analog IC Design (Spring 2013)

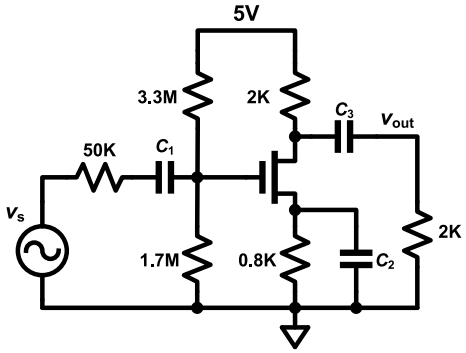
Due on Tuesday, April 2, 2013.

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

Problem 1: Assuming all transistors are in saturation, find small-signal voltage gain for each of the circuits shown below. Use variables g_{m1}, r_{o1}, g_{m2}, r_{o2}, etc.



Problem 2: The NMOS in the figure below has $V_{THN} = 0.7V$, and $KP_n = 500\mu A/V^2$. The drain current in the device is 1mA.



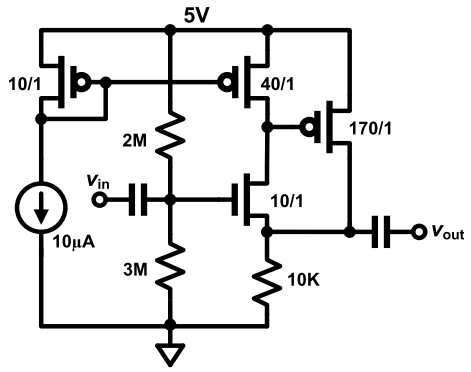
a) Determine the small signal gain from v_s to v_{out}.

b) Determine the W/L for the device and the DC operating points V_{GS} and V_{DS}.

c) The lowest frequency in v_s is ω_{in} =100rad/s. Determine the minimum values of C_1, C_2 and C_3required so that the frequencies associated with their charging/discharging is at least 10 times smaller than ω_{in}.

d) The supply voltage is changed to 5.5. Determine the small signal gain of the amplifier.

Problem 3: For the amplifier shown in the figure below:



$V_{THN} = 0.7V,$ and $KP_n = 200\frac{\mu A}{V^2}$

$V_{THP} = 0.8V,$ and $KP_p = 50\frac{\mu A}{V^2}$

$\gamma = 0$

a) Determine the operating points of all the devices in the circuit. For this part, neglect channel length modulation ($\lambda = 0$).

b) All transistors in the circuit have finite r_o, such that for any transistor $g_m r_o = 100$. Draw the small signal equivalent circuit of the amplifier, and determine the small signal gain ($\frac{v_{out}}{v_{in}}$). Also determine the input and output resistances of the amplifier (Perform low-frequency analysis only).