

# Homework 6

ECE 5411 – CMOS Analog IC Design (Spring 2013)

Due on Tuesday, Mar 19, 2013.

**Note:** Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

**Problems A:** Do problems A21.3, A21.6, A21.14 and A21.16 from the extra problem set available on the textbook website. Simulate **only** A21.6 and A21.16, others are optional.

**Problem B:** Assuming all transistors are in saturation, find small-signal voltage gain for each of the circuits shown below. Use variables  $g_{m1}$ ,  $r_{o1}$ ,  $g_{m2}$ ,  $r_{o2}$ , etc.

