Homework 5

ECE 5411 – CMOS Analog IC Design (Spring 2013)

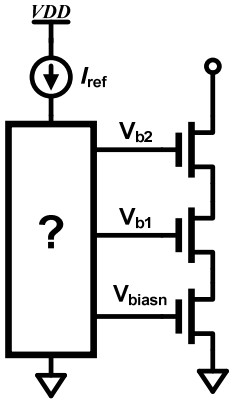
Due on Monday, March 5, 2013.

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

Problems A: Do problems A20.8, A20.16, A20.21, A20.22, A20.24, A20.25 and A20.28 from the extra problem set available on the textbook website. Simulations are **not required** for the problems A20.8 and A20.21.

Problem B2: The concept of cascoding can be further extended to realize a *triple-cascode* current mirror as shown below.

a) Assuming all devices to be identical, find an expression for the output resistance of this double-cascode current mirror? What are the trade-offs involved if double-cascoding is used in designs?



b) Given an ideal reference (I_{ref}) and using long-channel equations, design a wide-swing double-cascode current mirror such that the minimum allowed output voltage is $3V_{DS,sat}$. Neatly show the schematics and the steps for calculating the sizes of the long-length devices used in the design.