

Homework 4

ECE 5411 – CMOS Analog IC Design (Spring 2013)

Due on Tuesday, Feb 26, 2011.

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

Problems 1-3: Do problems A20.1, A20.2, A20.6 from the extra problem set available on the textbook website.

Problem 4: The beta-multiplier references (BMR) are used for constant- g_m biasing, where the goal is to stabilize the transconductance of a transistor. For example, in Fig. 1 (a), the g_m of M1 will be 'copied' to a current mirror device (not shown here).

- Derive expressions for I_{ref} , V_{GS1} and g_{m1} in Fig. 1 (a). Note that M3 is K times wider than M4 and M1 and M2 are the same size. Draw the schematic for a start-up circuit for this BMR.
- Will the circuit shown in Fig. 1 (b) work as a constant- g_m reference? Explain.
- Fig. 1 (c) shows a fix for the body effect problem in the bottom NMOS in the BMR. Derive an equation for I_{ref} in this circuit. Run a temperature sweep on I_{ref} and compare it with the results from the BMR seen in class. Explain your observations.

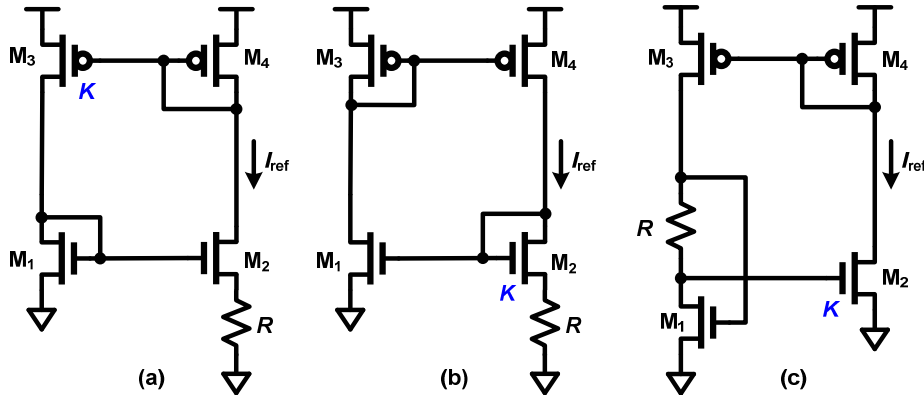


Figure 1: Problem 4

Problem 5: Using the TSMC 180n process and the characterization data from HW3, design and simulate:

- A beta-multiplier current reference (BMR) as seen in Fig. 20.18 in the textbook. Plot the currents in the BMR when V_{DD} is swept. Comment on the supply sensitivity of the circuit.
- Repeat part (a), by using an ideal amplifier to regulate the drain voltages of the bottom NMOS devices in the BMR.
- Replace the ideal amplifier model by a transistor-level self-biased amplifier as in textbook Fig. 20.22. Simulate and comment on the supply sensitivity of this circuit. Apply a step input to V_{DD} and plot the response to verify the stability of the circuit.