Homework 3

ECE 5411 – CMOS Analog IC Design (Spring 2013)

Due on Tuesday, Feb 19, 2011.

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

Problems 1-3: Do problems A9.20, A9.27-A9.28 from the extra problem set available on the textbook website .

Problem 4 - Process Characterization: Using the TSMC 180n CMOS models ($V_{DD} = 1.8V$, $L_{min} = 0.18\mu$):

a) Regenerate the Table 9.2 in the textbook for an overdrive ($V_{OV} = V_{GS} - V_{THN}$) equal to 5% of V_{DD}. Use $L = L_{min}$ and state your assumptions. Show all the relevant simulation plots. *Save all your neatly created simulation test-benches for upcoming homeworks and project.*

b) For the NMOS and PMOS devices in your table, plot f_T, $g_m r_o$ and $g_m r_o \cdot f_T$ as a function of overdrive (V_{OV}). Interpret each of these graphs. (*You can plot these results in any tool like Excel or Matlab.*)

c) For the NMOS and PMOS above, plot $\frac{g_m}{I_D}$ as a function of overdrive (V_{OV}). Explain these plots.