Homework 1

ECE 5411 – CMOS Analog IC Design (Spring 2013)

Due on Tuesday, Feb 5, 2013.

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

Problem 1-4: Do problems A9.1, A9.3-A9.5 from the extra problem set available on the textbook website.

Problem 5: Using the TSMC 180nm Spectre models, generate all the I-V curves for a 10/1 NMOS and a 10/1 PMOS. Do you expect long-channel or short-channel behavior from these devices?