

Project Help Session

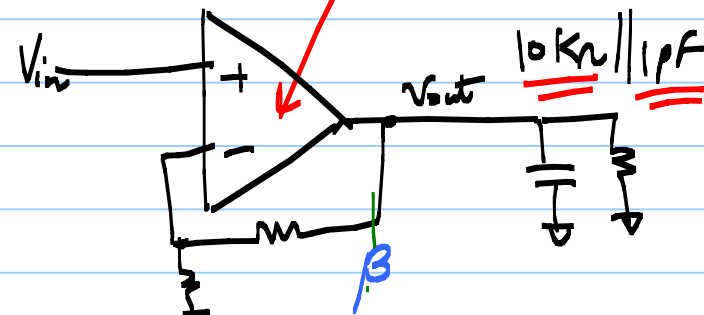
Note Title

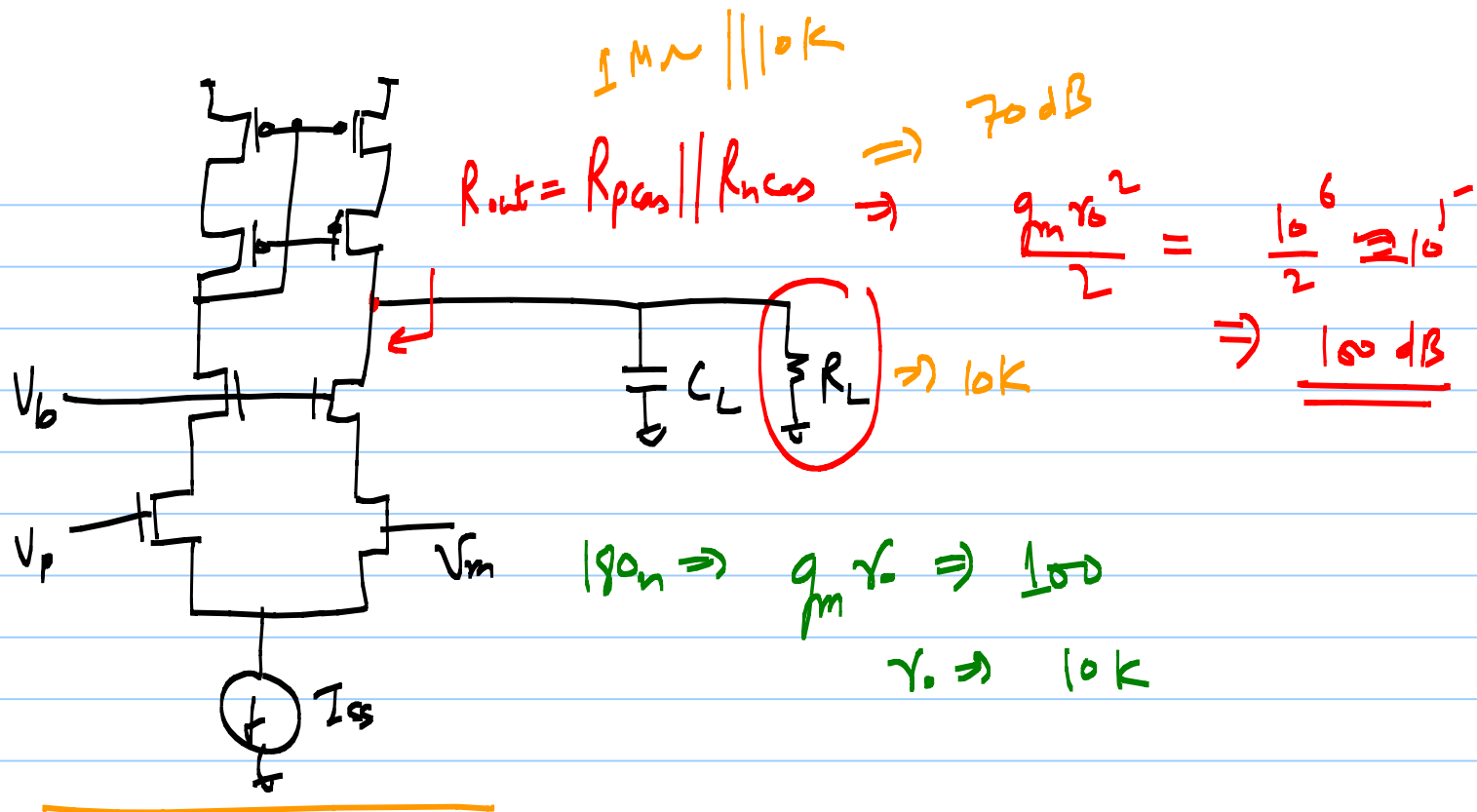
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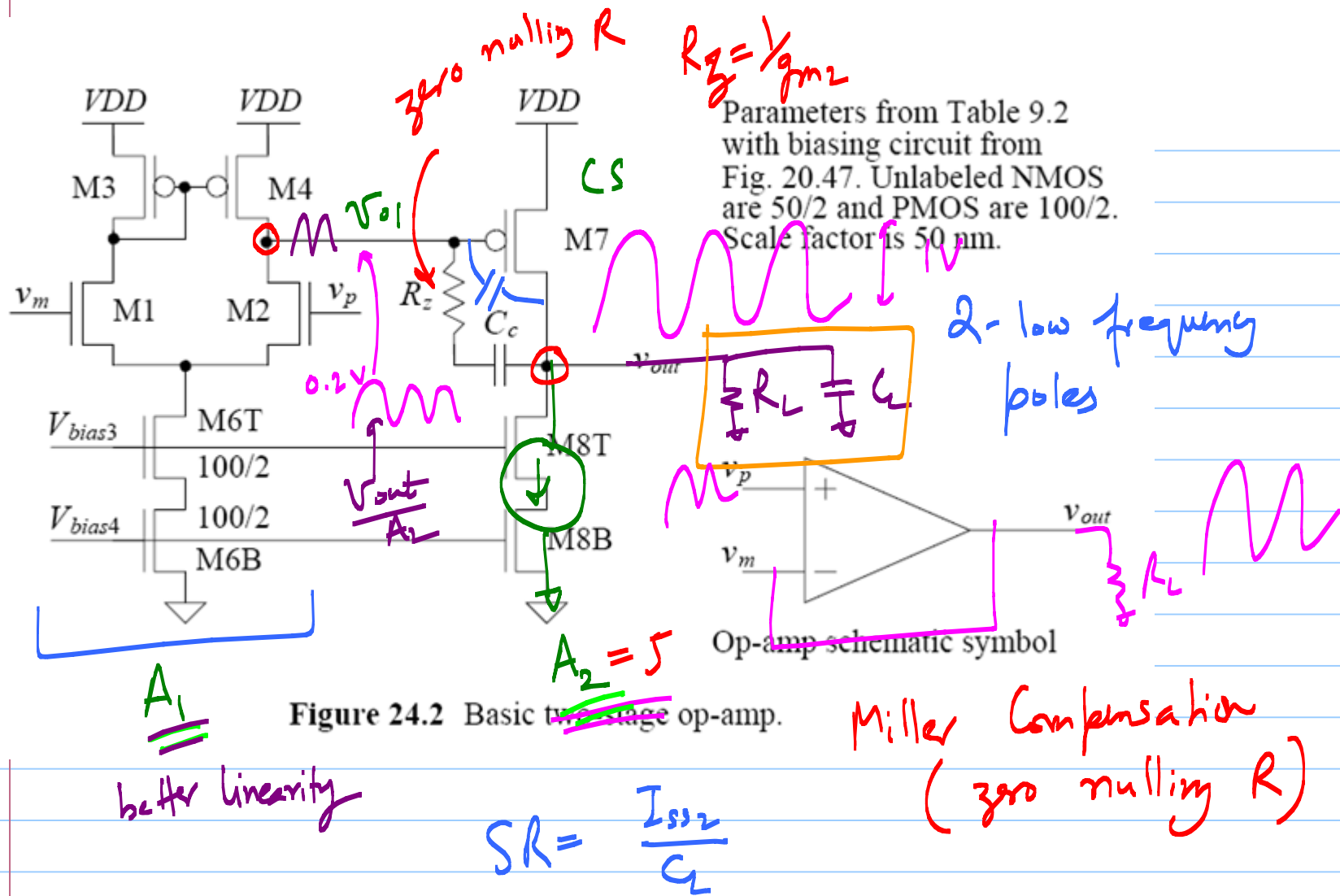
Table 1: Opamp design specifications.

Parameter	Specified Value
Technology	TSMC 180n CMOS
Supply voltage, V_{DD}	1.8 V
Typical load	$10k\Omega 1pF$
Unit gain frequency (f_{un})	$> 100 MHz$
Open-loop gain (A_{OL})	$> 70 dB$
Slew-rate (SR)	$> 500 \frac{V}{\mu s}$
Phase margin (ϕ_M)	$\geq 63^\circ$
Power consumption	Minimum possible

$$SR = 500 \frac{V}{\mu s} = \frac{0.5V}{ns}$$





Miller Compensation

$$SR = \frac{I_{SS2}}{C_L} = \frac{I_{SS2}}{1\text{pF}} \quad 500 \frac{\text{V}}{\mu\text{s}}$$

$$I_{SS2} = 500 \times 10^6 \times 10^{-12} \\ = \boxed{500 \mu\text{A}}$$

x Need Class AB 2nd-stage

output buffer to drive "heavy" loads

Telescopic

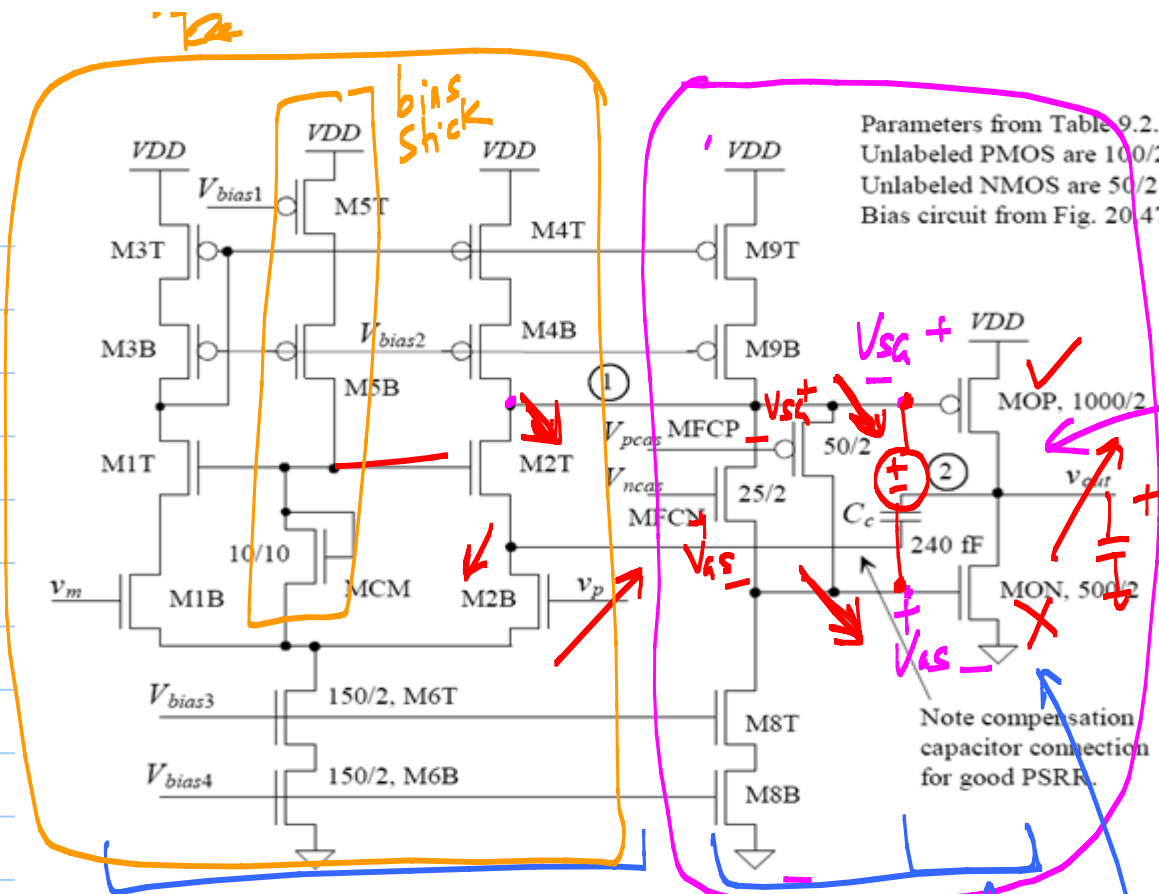


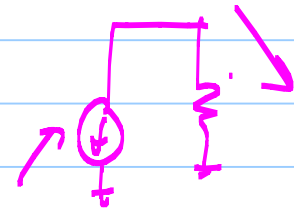
Figure 24.29 A CMOS op-amp with output buffer.

A₁

A₂

$$A_{v2} = -(g_{mp} + g_{mn}) (r_{op} || r_{on})$$

class AB
(push-pull)
stage



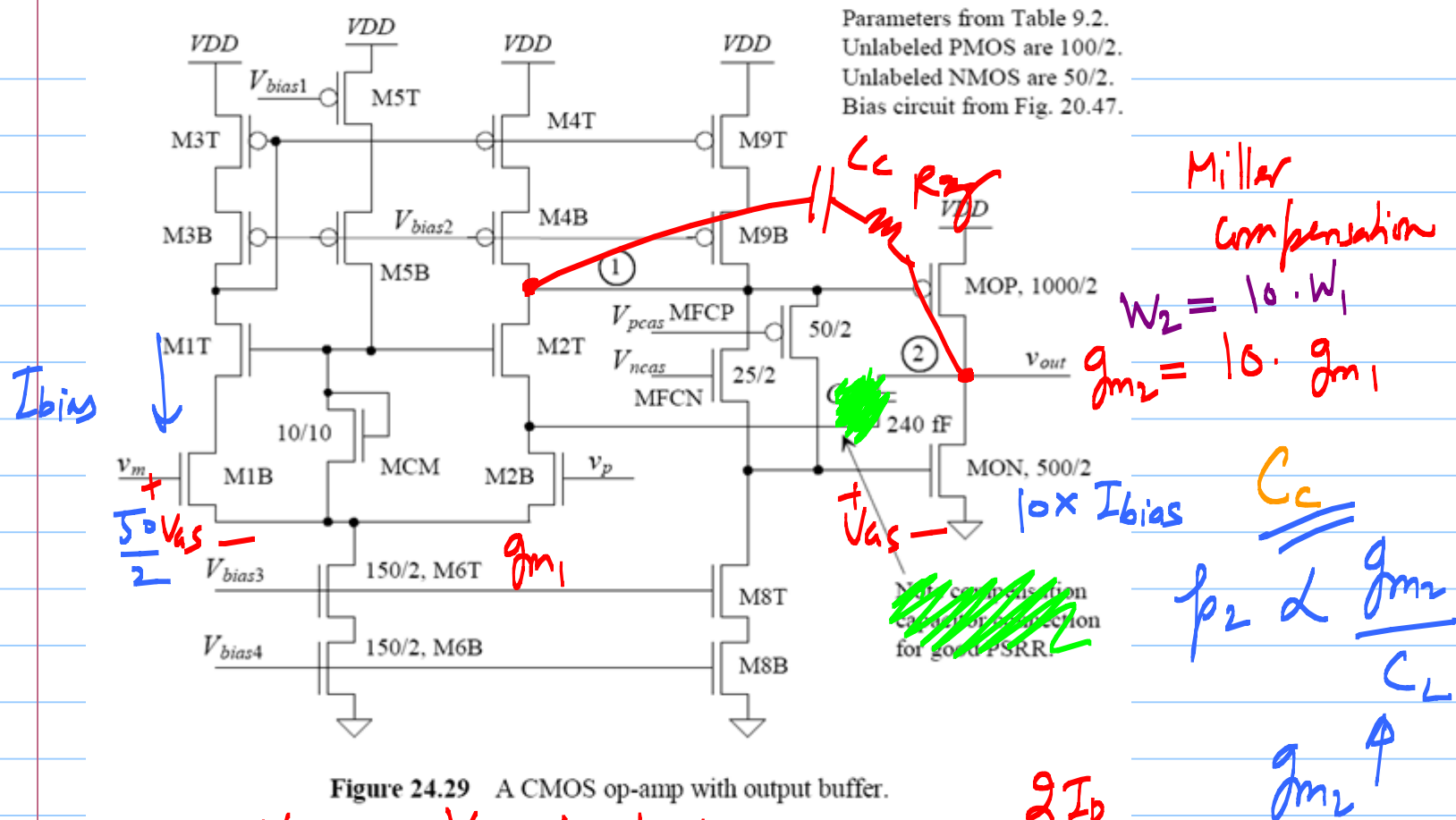


Figure 24.29 A CMOS op-amp with output buffer.

Same $V_{as} \Rightarrow V_{ov}$ is fixed

$$g_m = \frac{2I_D}{V_{ov}}$$

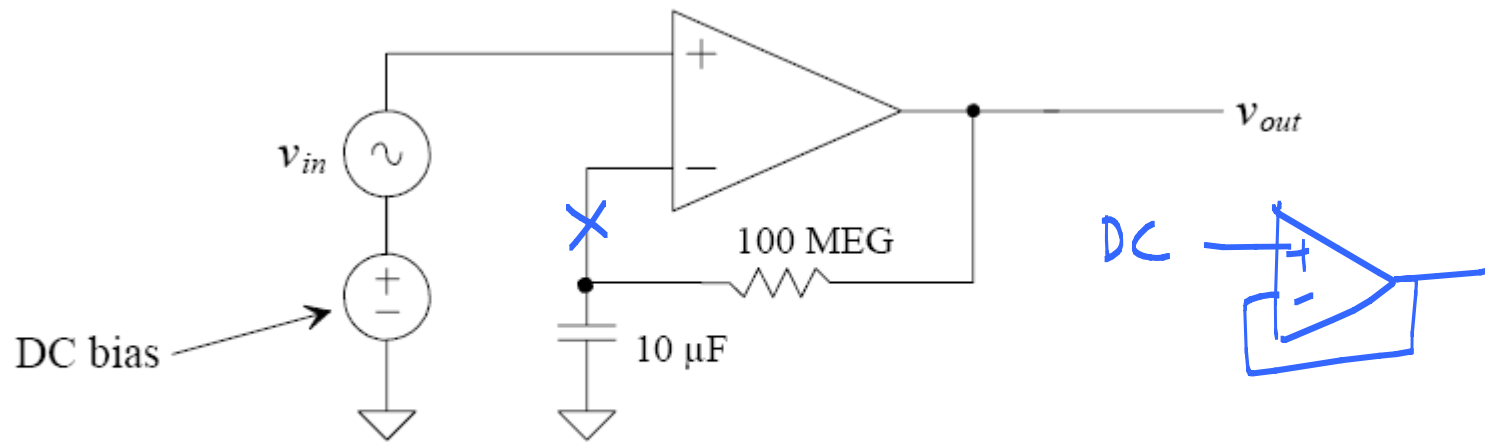
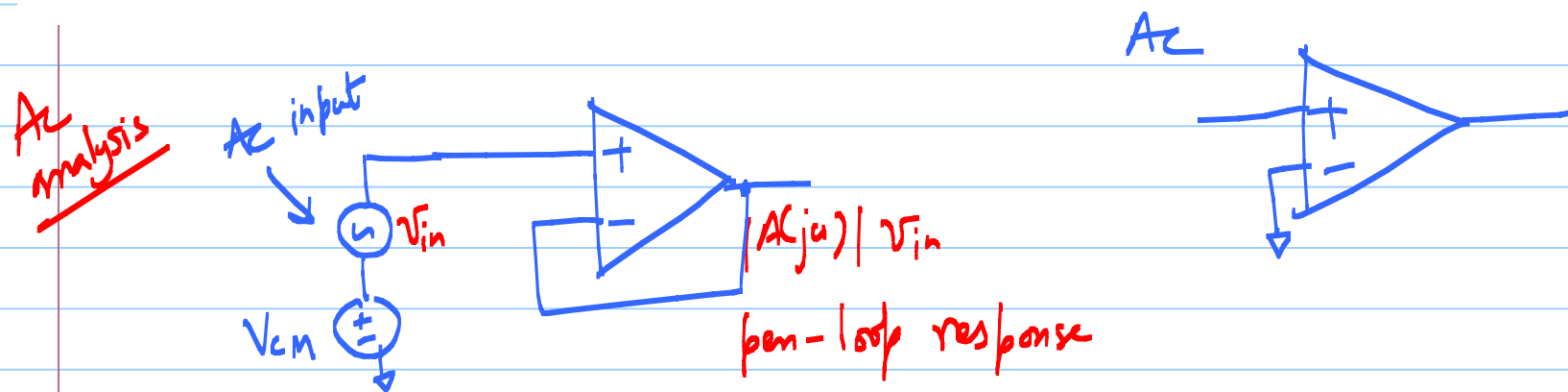
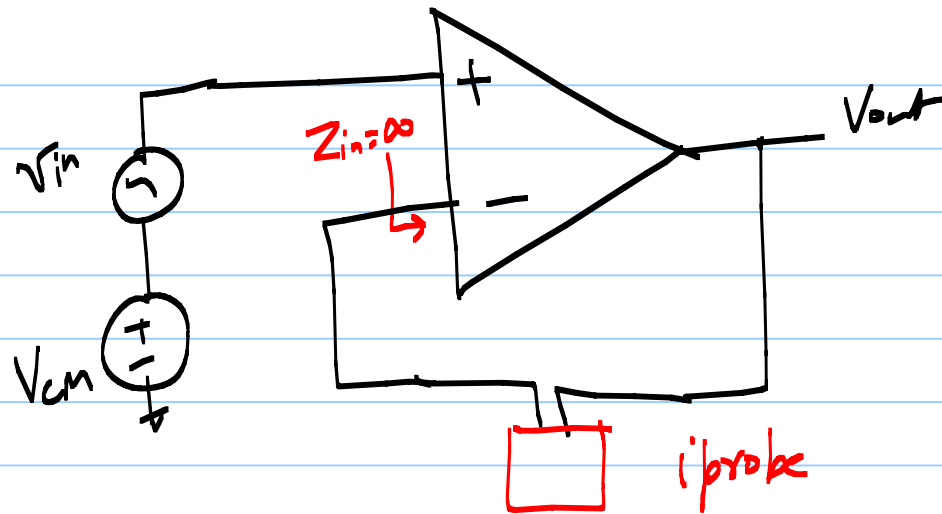


Figure 24.9 Circuit configuration used to simulate open-loop frequency response.



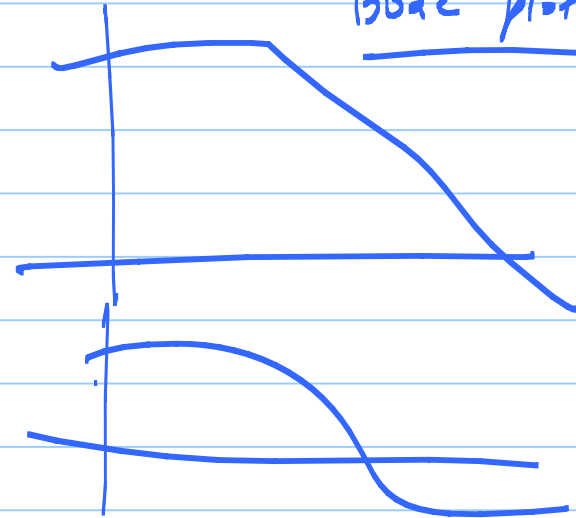
In Spectre



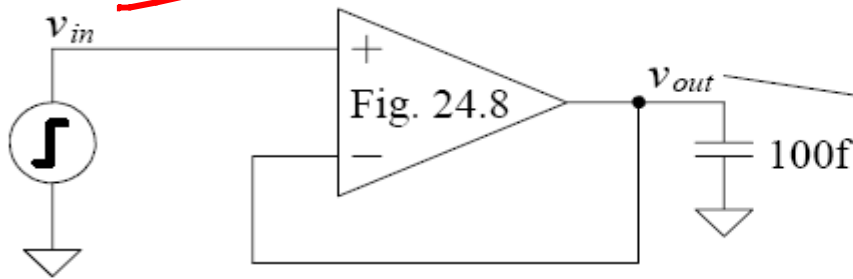
"Stb Analysis"

"Stability"

"Bode plots"



step response



$$C_c = 2.4 \text{ pF}$$

$$R_z = 6.5 \text{ k}$$

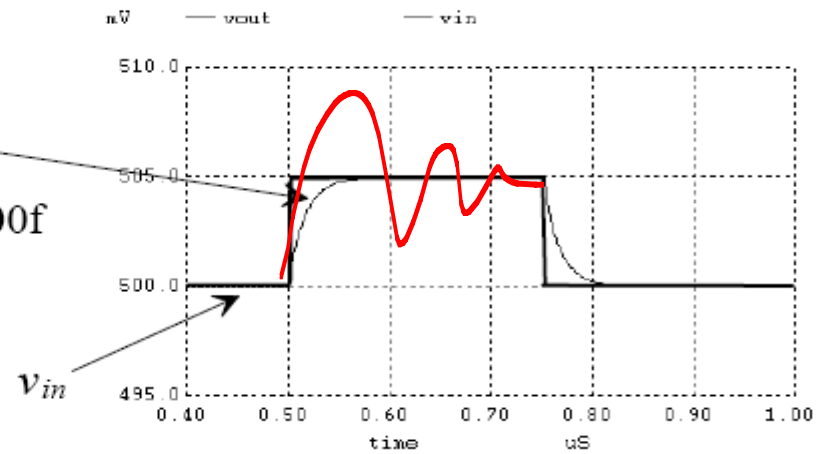


Figure 24.14 Good step response of the op-amp with the zero absent.

Small - steps
large - step



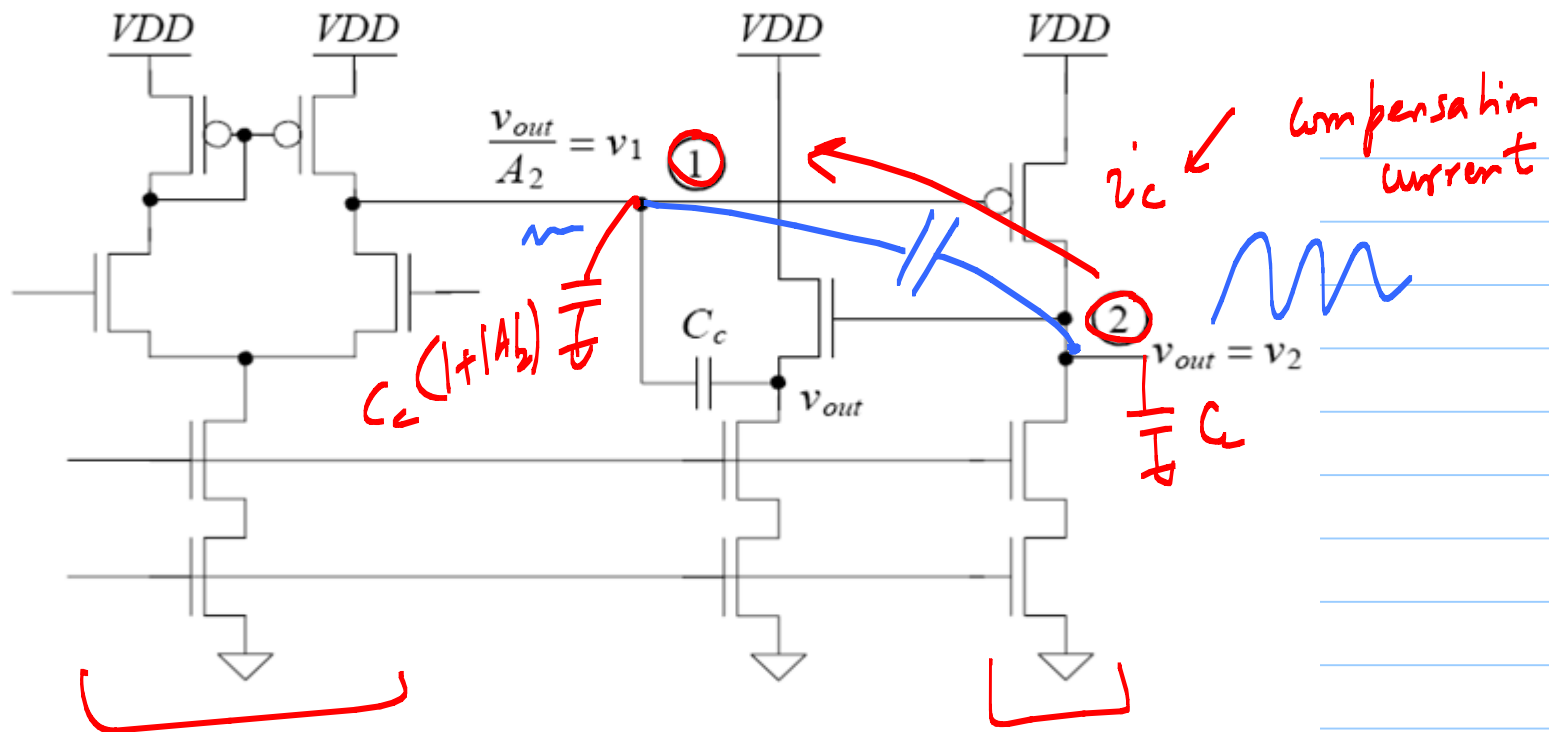


Figure 24.16 Using an amplifier to eliminate forward signal feedthrough via the compensation capacitor.

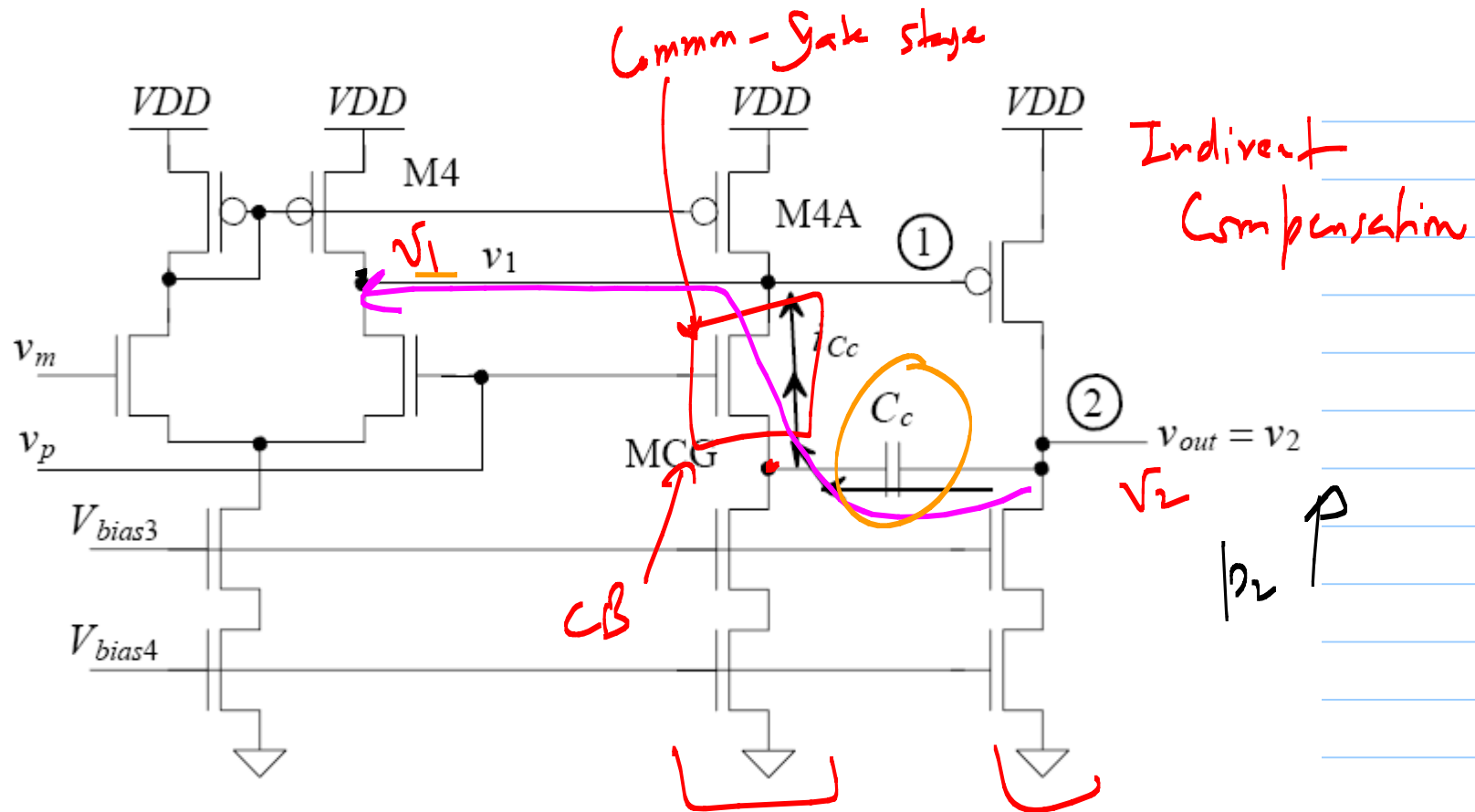


Figure 24.17 Feeding back a current indirectly to avoid the RHP zero.

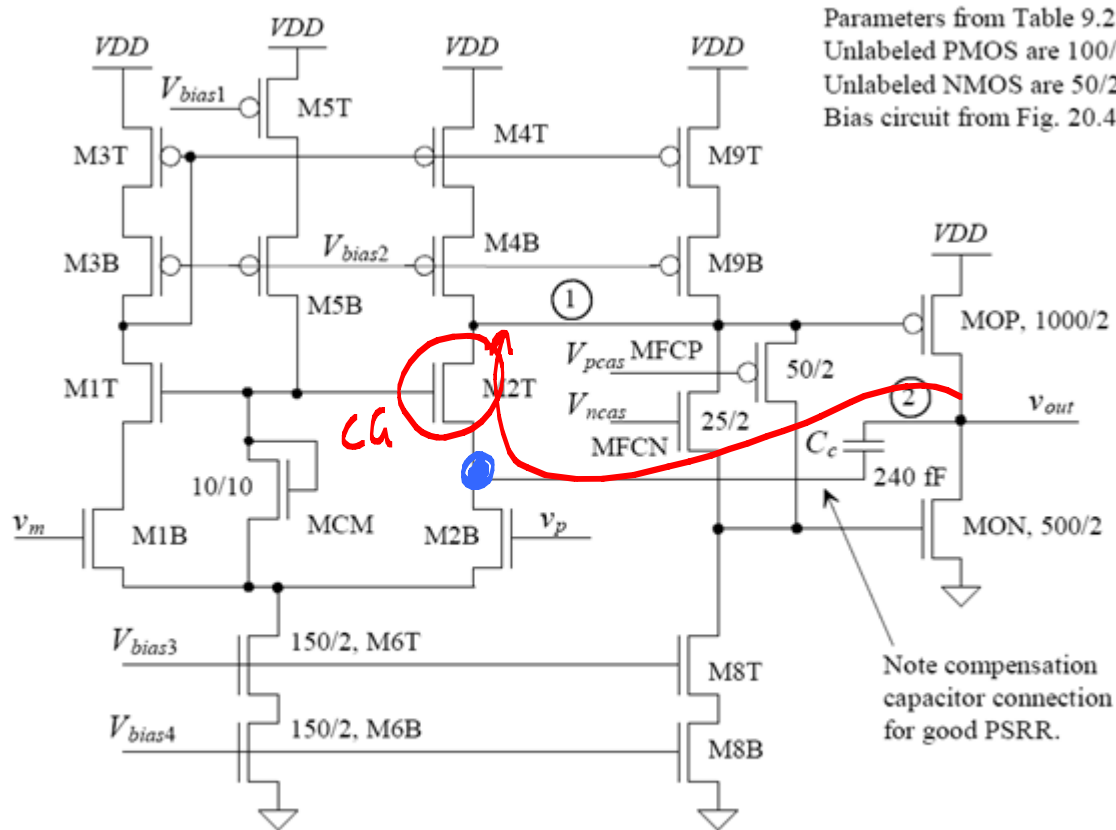


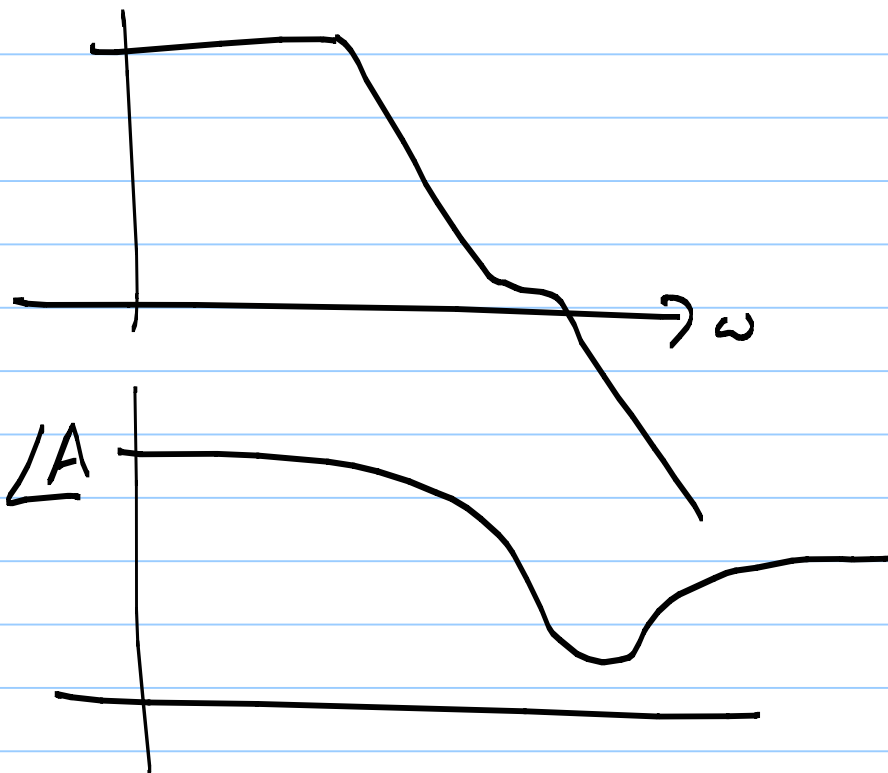
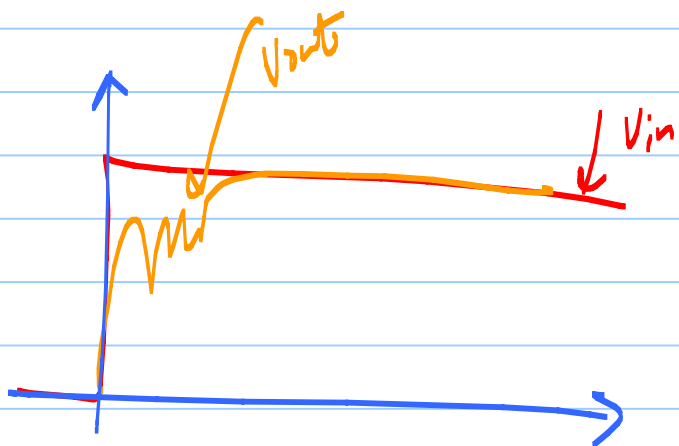
Figure 24.29 A CMOS op-amp with output buffer.

LHP
zero

$C_c \downarrow$
 $g_{m2} \downarrow$

p_3

$$f_2 \approx f_{un} |A|$$



Folded cascode

Biasing from Fig. 20.47.
 Sizes given in Table 9.2.

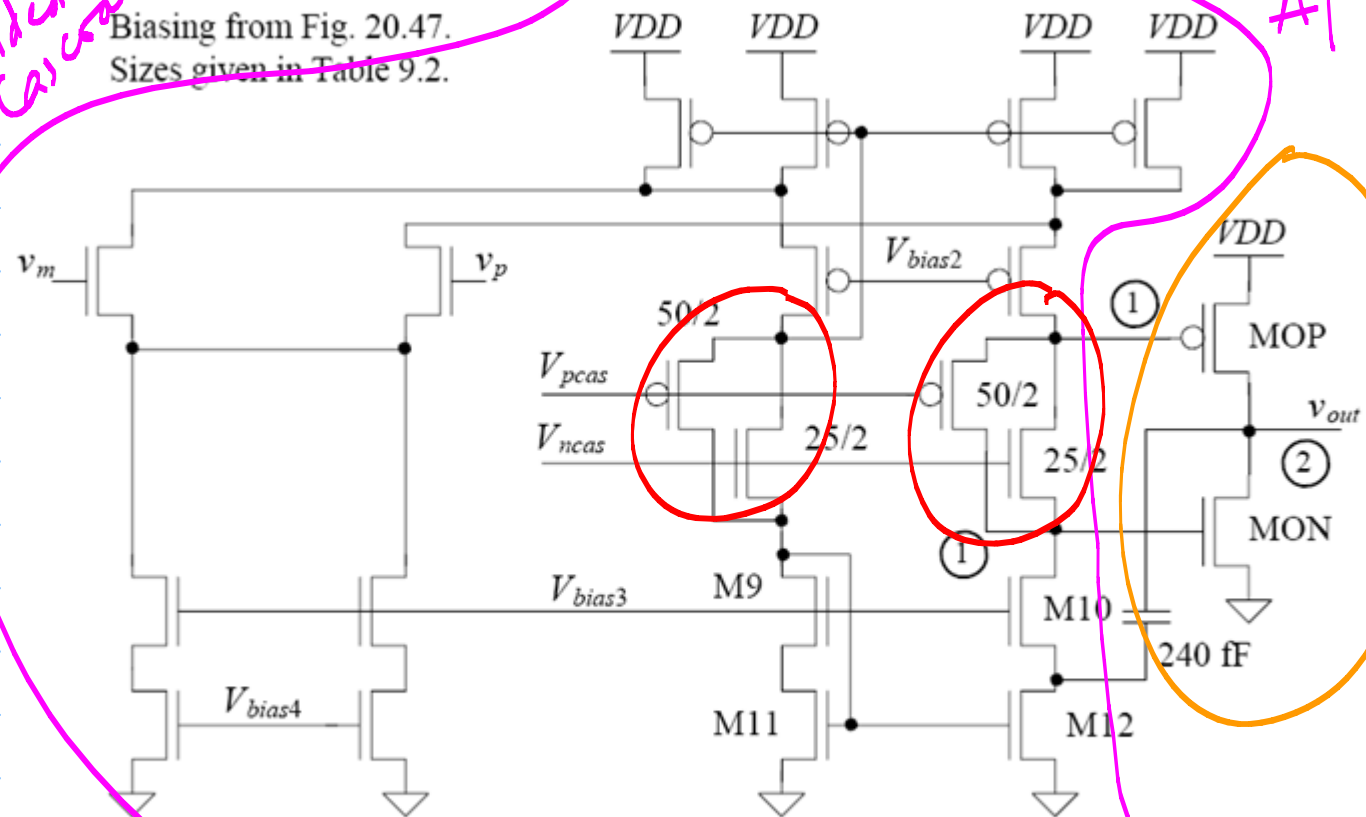


Figure 24.44 Folded-cascode op-amp with class AB output buffer.