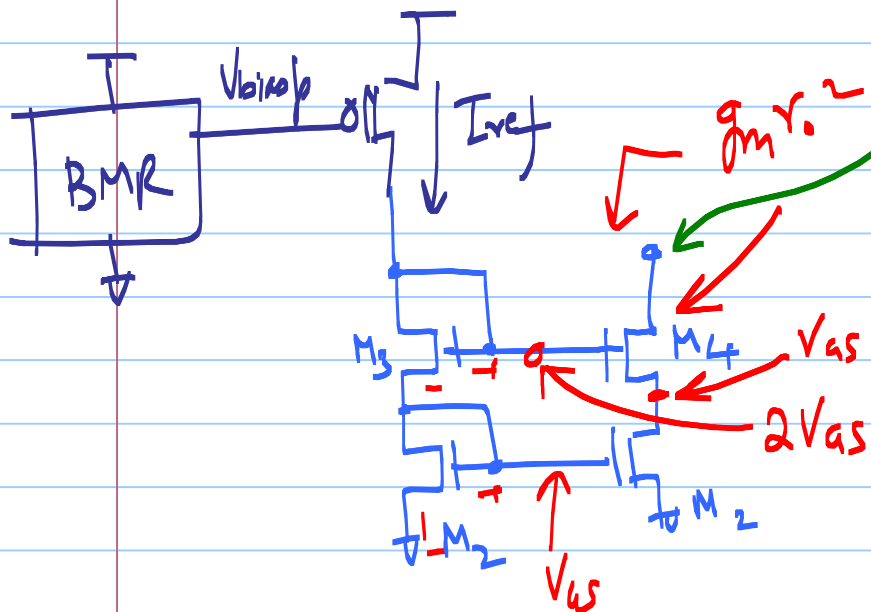
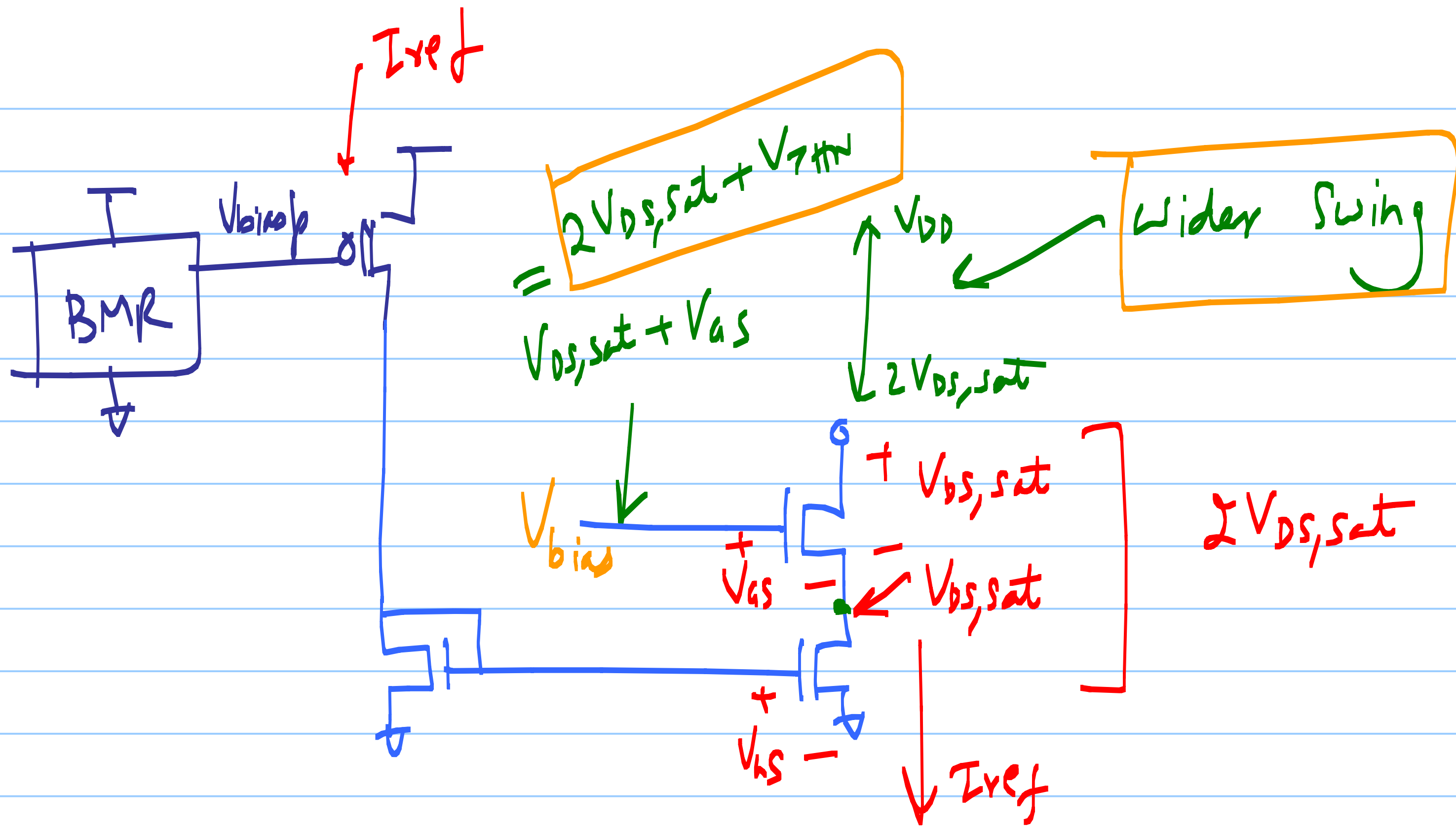
ECE 511 – Lecture 9

Note Title

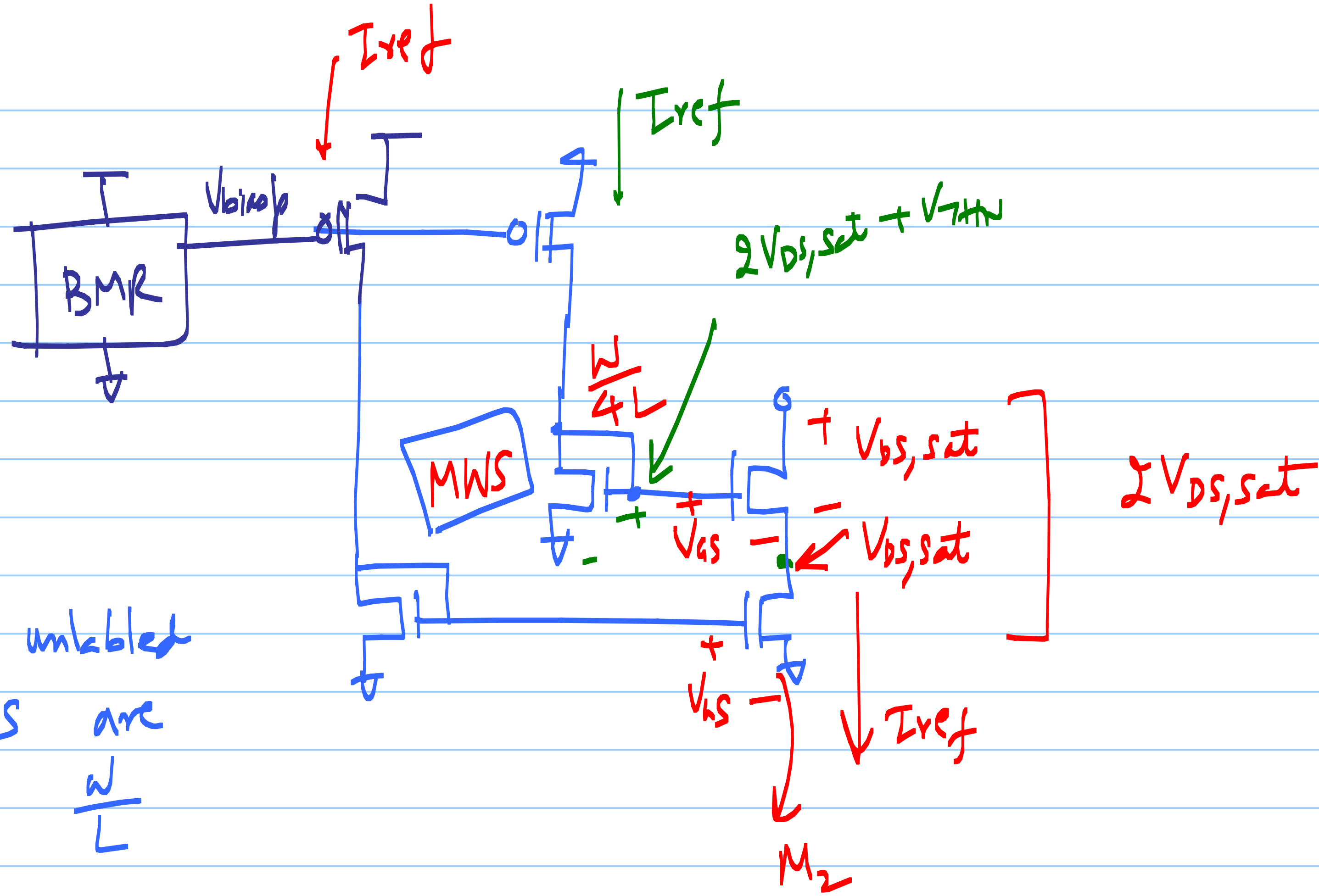
2/22/2012



$V_{GS} + V_{DS,sat} = 2V_{DS,sat} + V_{Tn}$



BMR
Vbiasp
Iref
$= 2V_{DS,sat} + V_{THN}$
$V_{DS,sat} + V_{GS}$
VDD
$2V_{DS,sat}$
wider swing
V_{bias}
$+ V_{GS} -$
$+ V_{DS,sat} -$
$V_{DS,sat}$
$2V_{DS,sat}$
$+ V_{GS} -$
Iref



All unlabled NMOS are $\frac{W}{L}$

for MOS device (β')

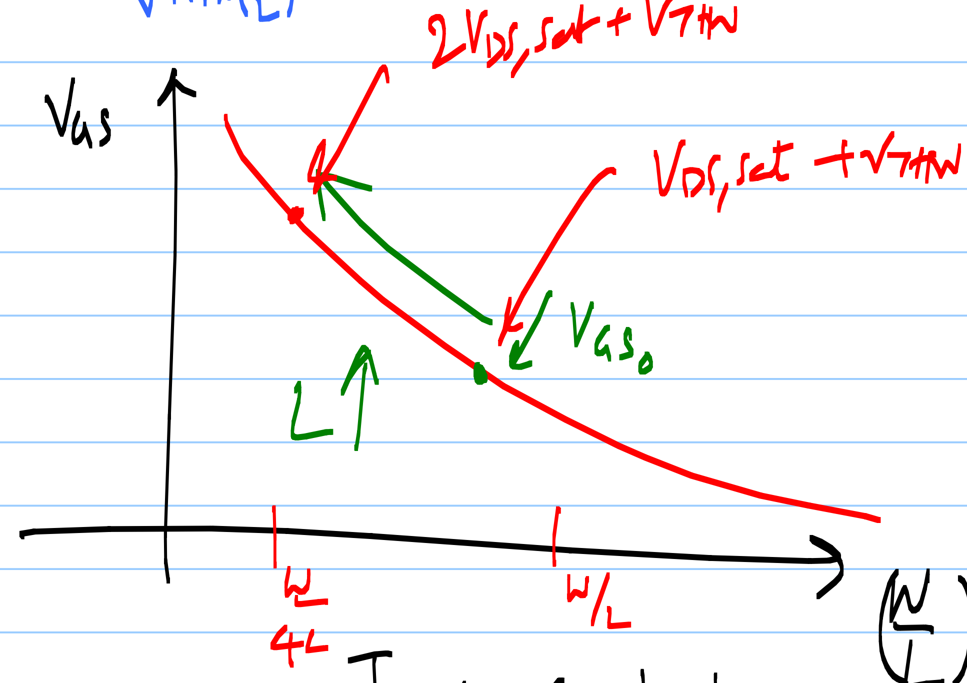
$$V_{GS}' = 2V_{DS,sat} + V_{THN} = \sqrt{\frac{2I_{ref}}{\beta'}} + V_{THN}$$

$$\Rightarrow 2\sqrt{\frac{2I_{ref}}{\beta}} = \sqrt{\frac{2I_{ref}}{\beta'}}$$

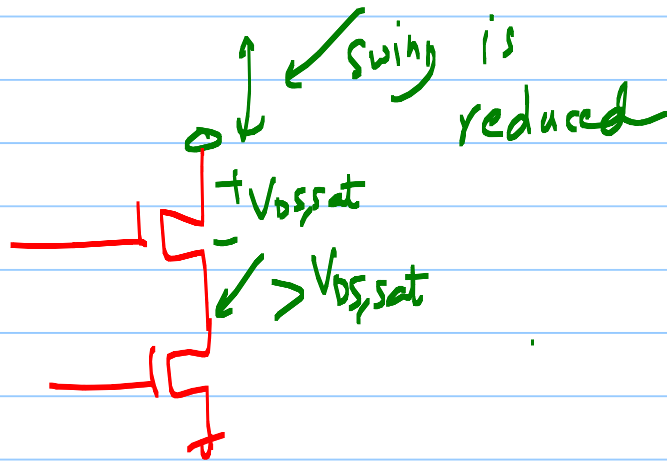
$$\Rightarrow 2\sqrt{\beta'} = \sqrt{\beta}$$

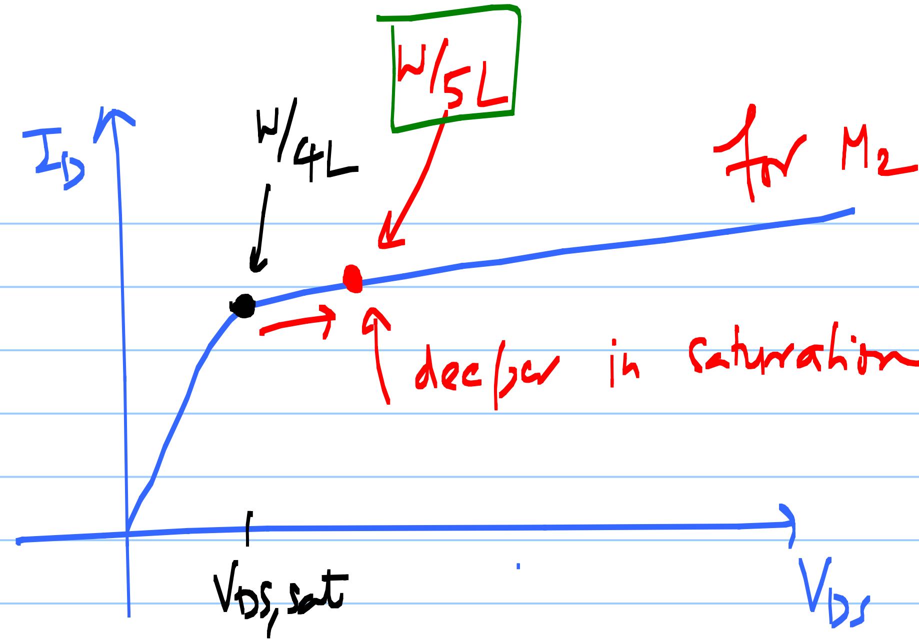
$$\Rightarrow \boxed{\beta' = \frac{\beta}{4}} \Rightarrow \frac{W}{4L}$$

$$V_{GS} = \sqrt{\frac{2I_D}{KP_n\left(\frac{W}{L}\right)}} + V_{THN}$$



I_D is constant

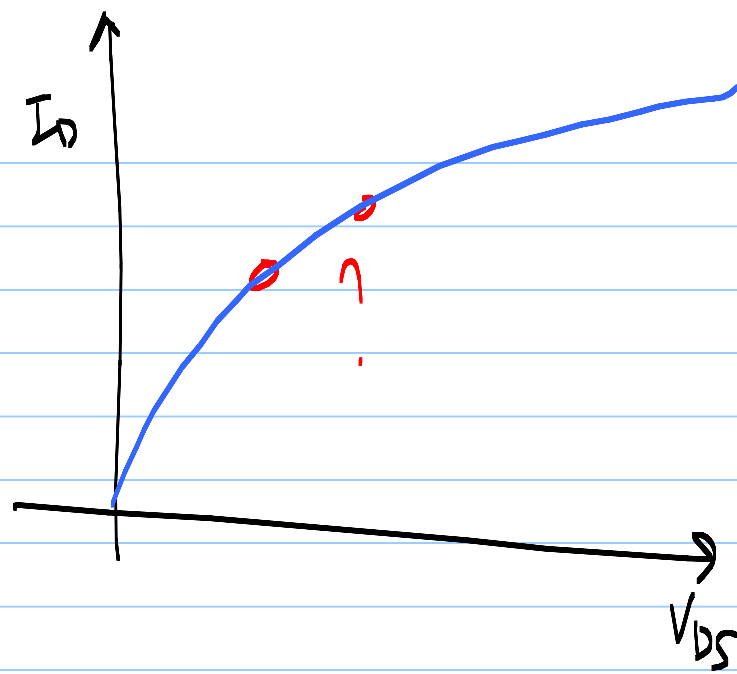


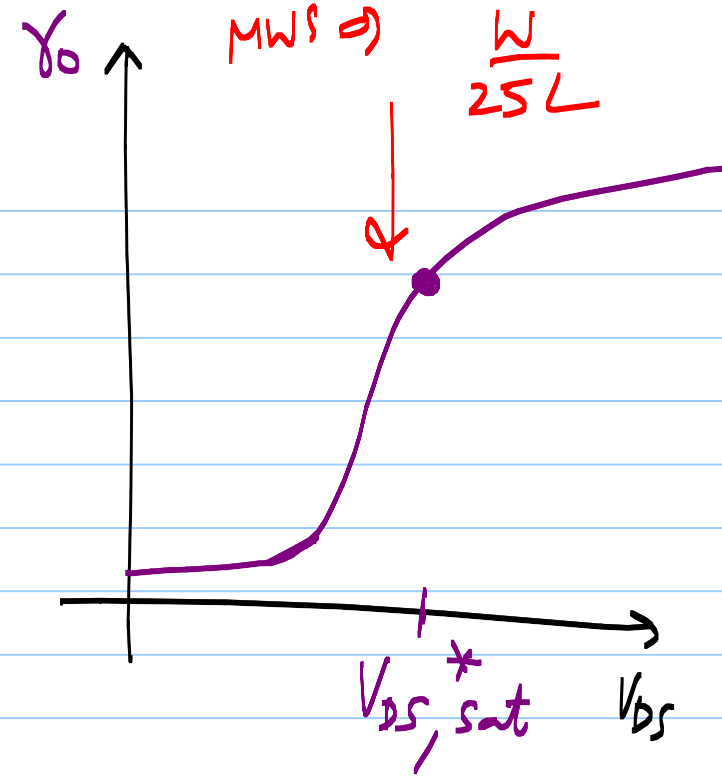


if for MWS ← $\frac{W}{4L}$

50n short channel

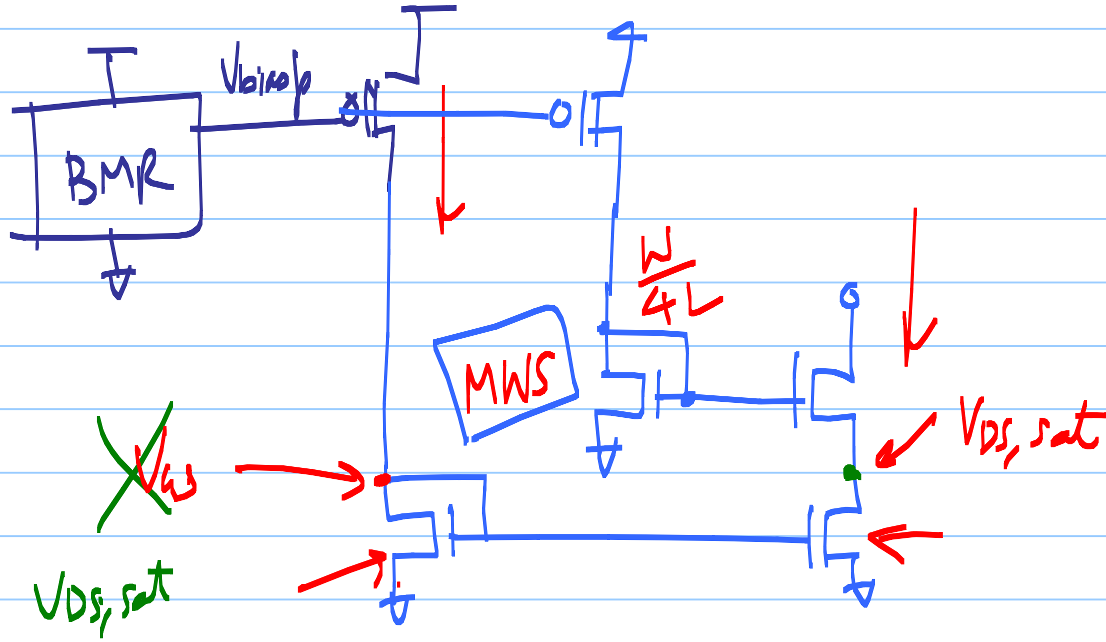
for M4



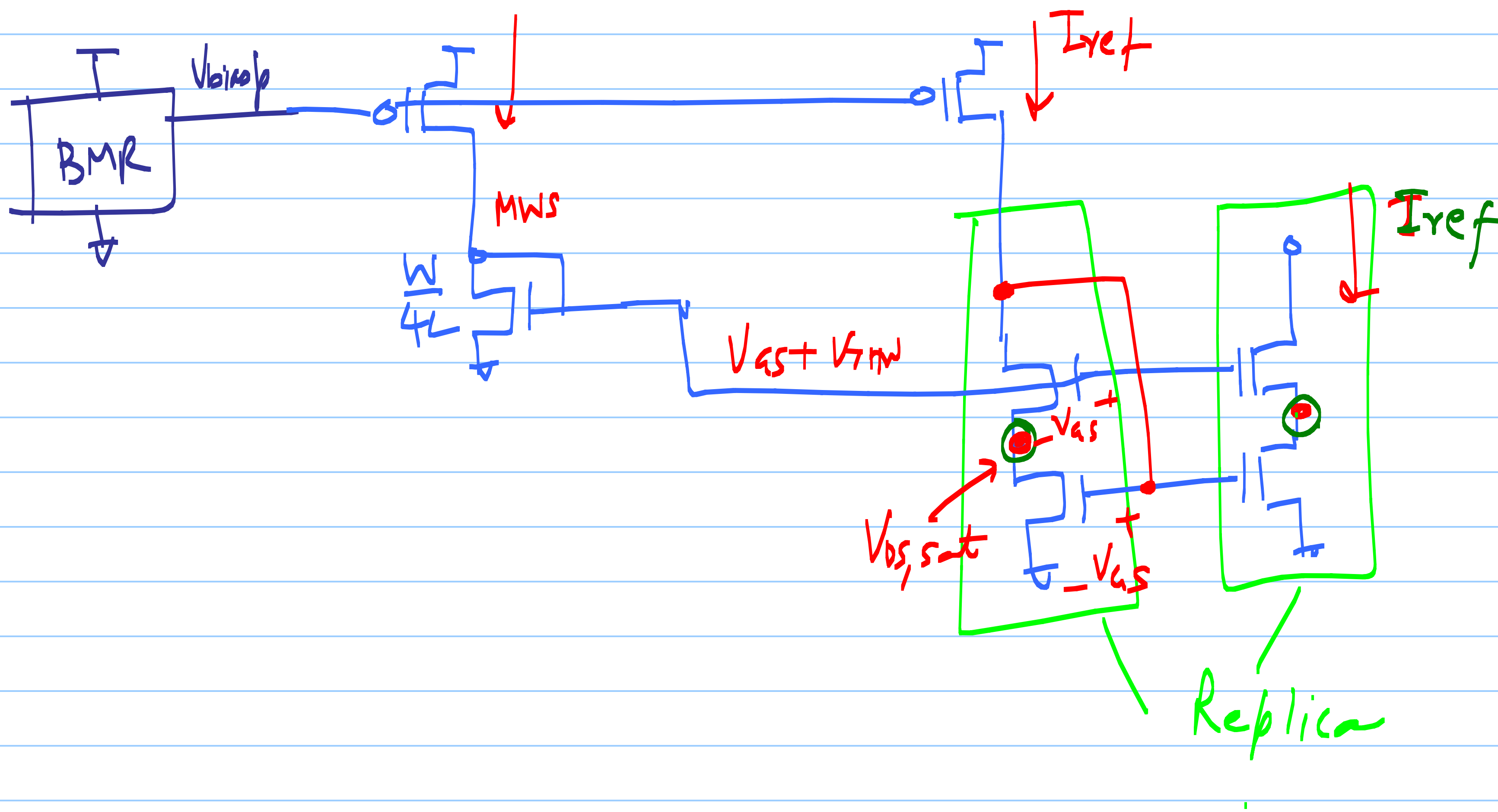


for 180n ⇒ $\frac{W}{10L} \leftrightarrow \frac{W}{15L}$

Sizing MWS ⇒ M_2 is in high-r_o regime


BMR
Vbiasp
MWS
W/4L
VGS
VDS,sat
VDS,sat

"Replica Circuit"



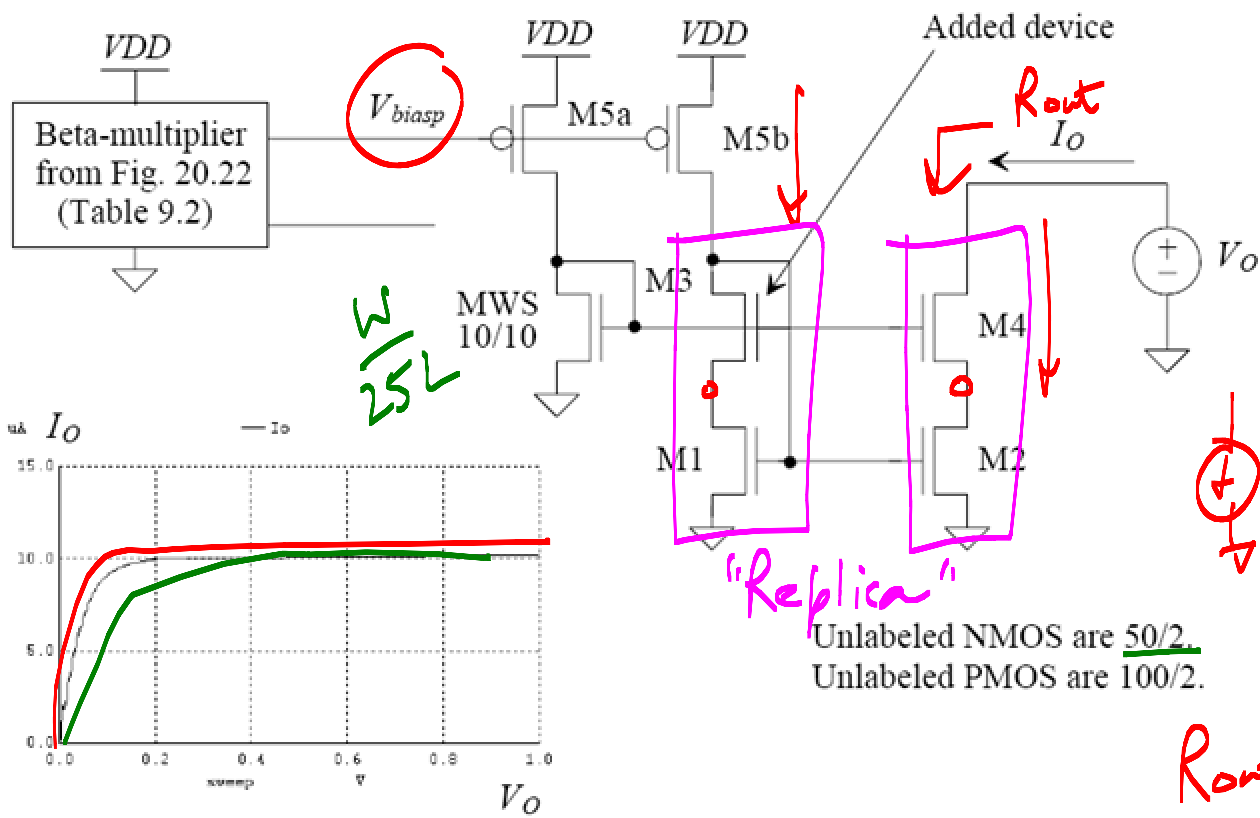


Figure 20.38 Wide-swing cascode current source in the short-channel process (good). Notice the drain-to-source voltages of M1 and M2 are the same.

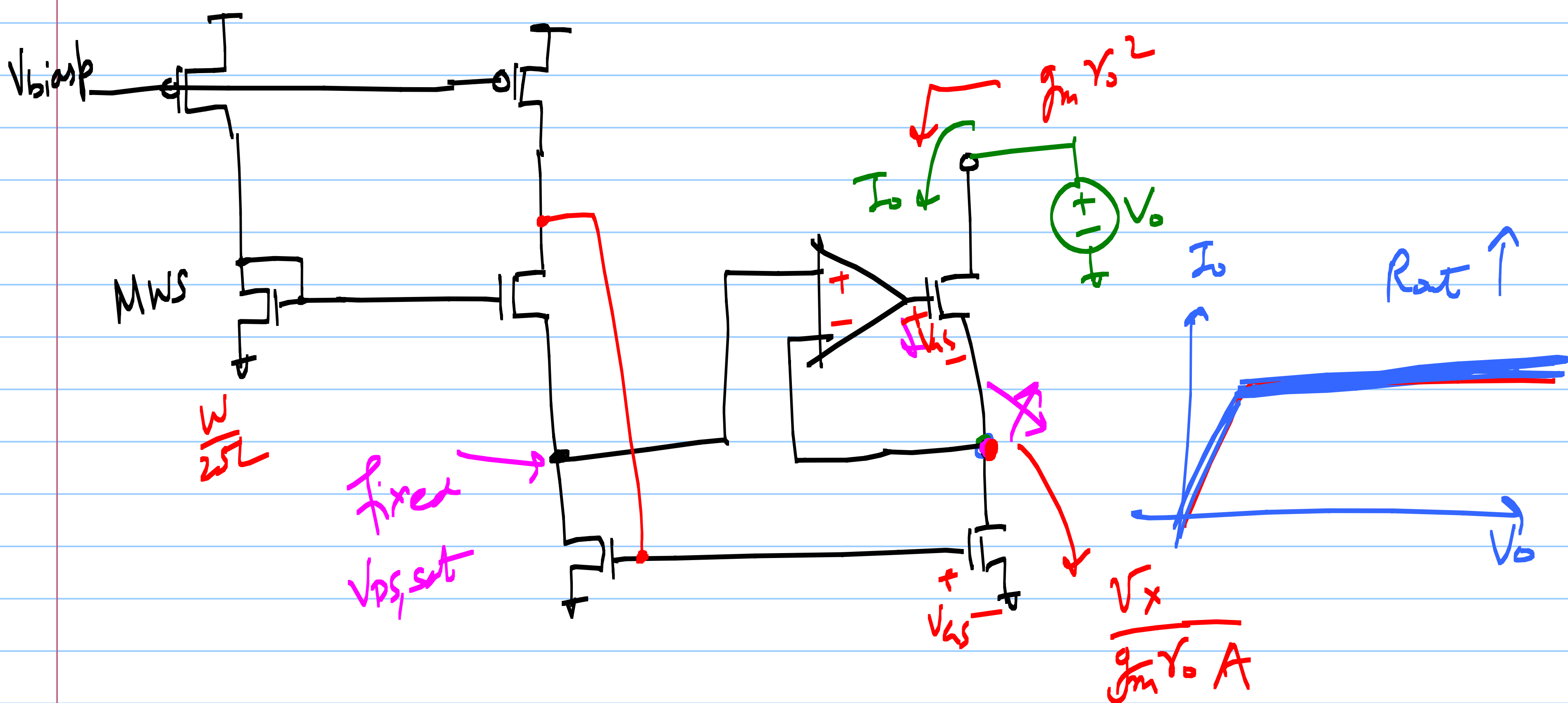
PMOS version

$\frac{W}{25L} \rightarrow \frac{50}{50}$

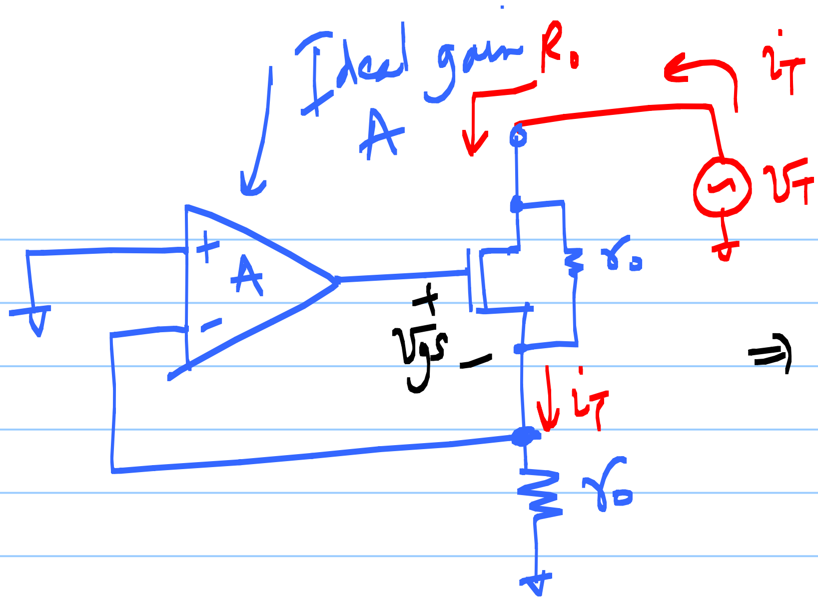
$\frac{10}{10}$

$R_{out} = g_m r_o^2$

Regulated Drain Current Mirror



Small-signal analysis.



$$\Rightarrow v_{gs} = A(0 - i_T r_o) - i_T r_o$$

$$v_{gs} = -(A+1)\, i_T r_o \longrightarrow (1)$$

KCL @ The output $\Rightarrow$

$$i_T - g_m v_{gs} - \frac{(v_T - i_T r_o)}{r_o} = 0$$

$$i_T + g_m r_o (A+1) i_T - \frac{v_T}{r_o} + i_T = 0$$

$$\Rightarrow \frac{v_T}{r_o} = i_T \left(2 + g_m r_o (A+1)\right)$$

$$\Rightarrow R_o = \frac{v_T}{i_T} = \left(2 + g_m r_o (A+1)\right) r_o = 2 r_o + g_m r_o^2 (A+1)$$

$$\simeq g_m r_o^2 \cdot A$$

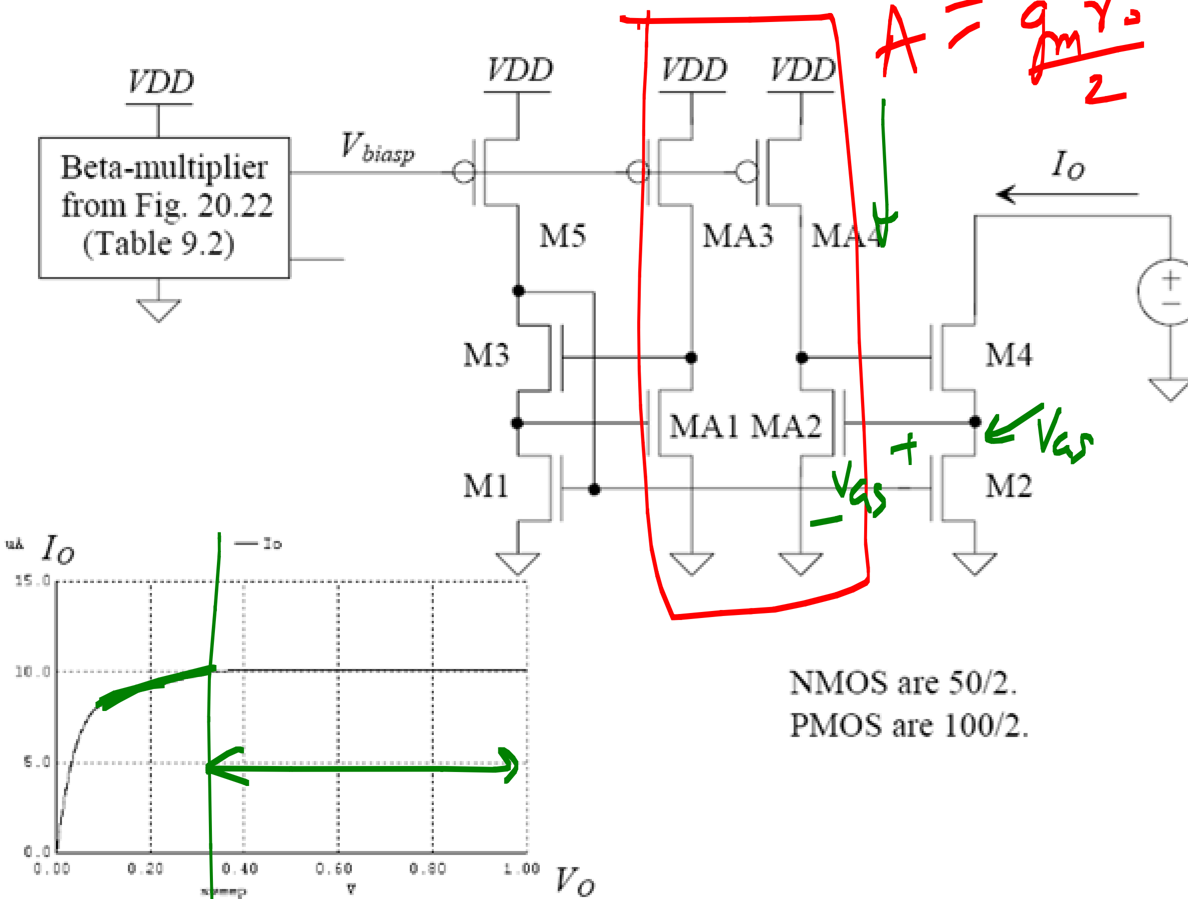


Figure 20.42 Using amplifiers to regulate the drain potentials in a current mirror.

$$A = \frac{g_m r_o}{2}$$

$$R_o = g_m r_o^2 \times \frac{g_m r_o}{2} = \frac{g_m^2 r_o^3}{2}$$

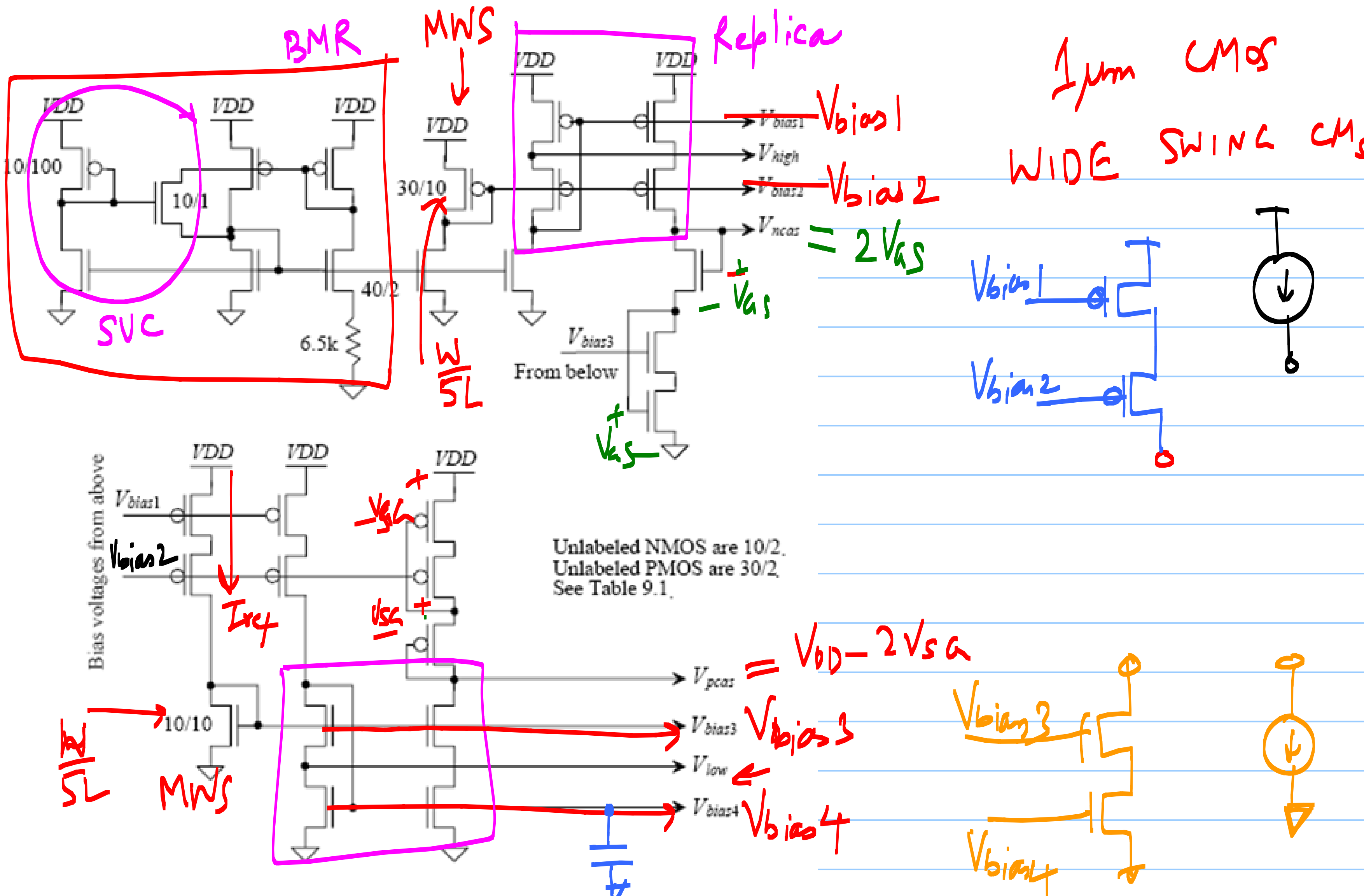
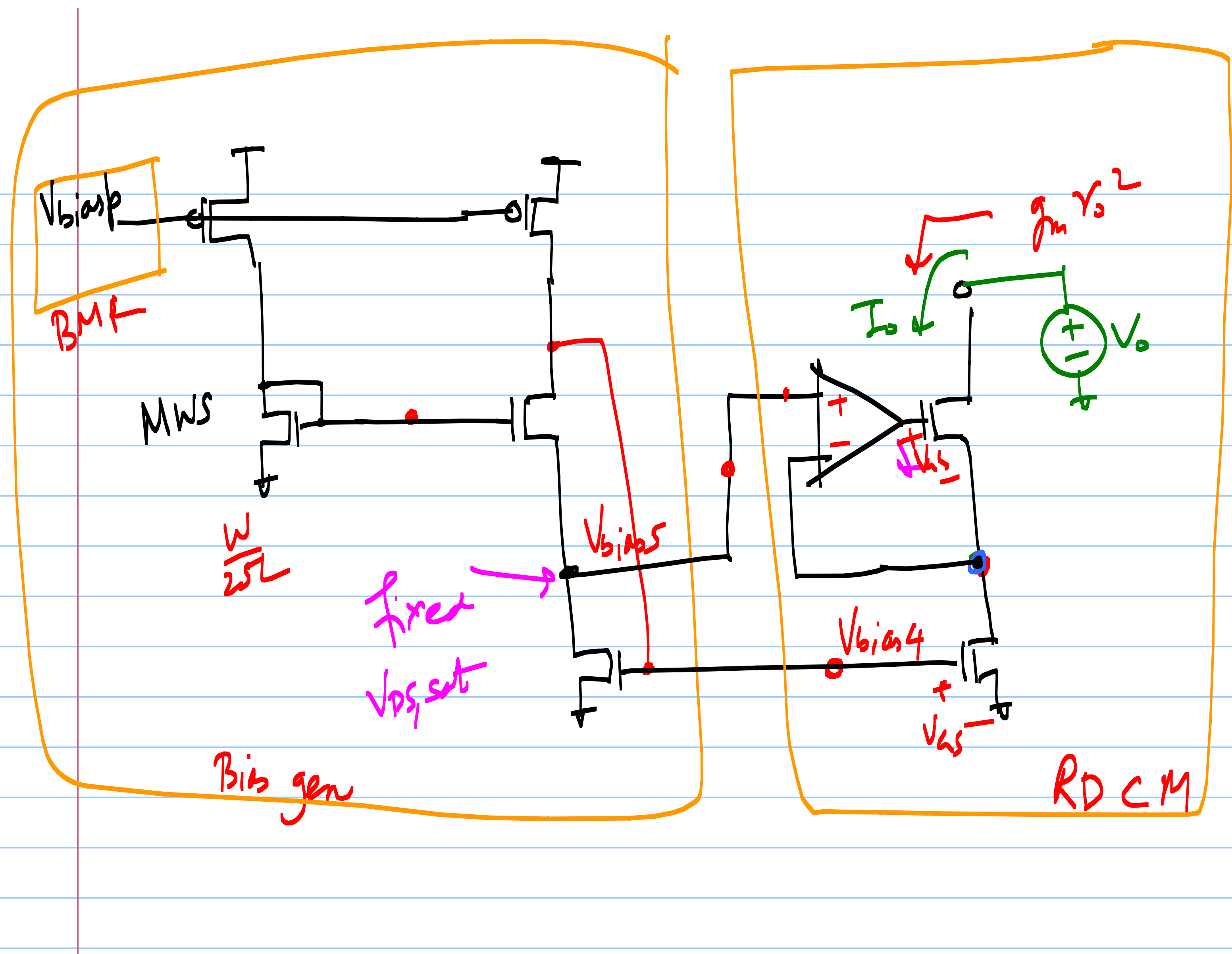
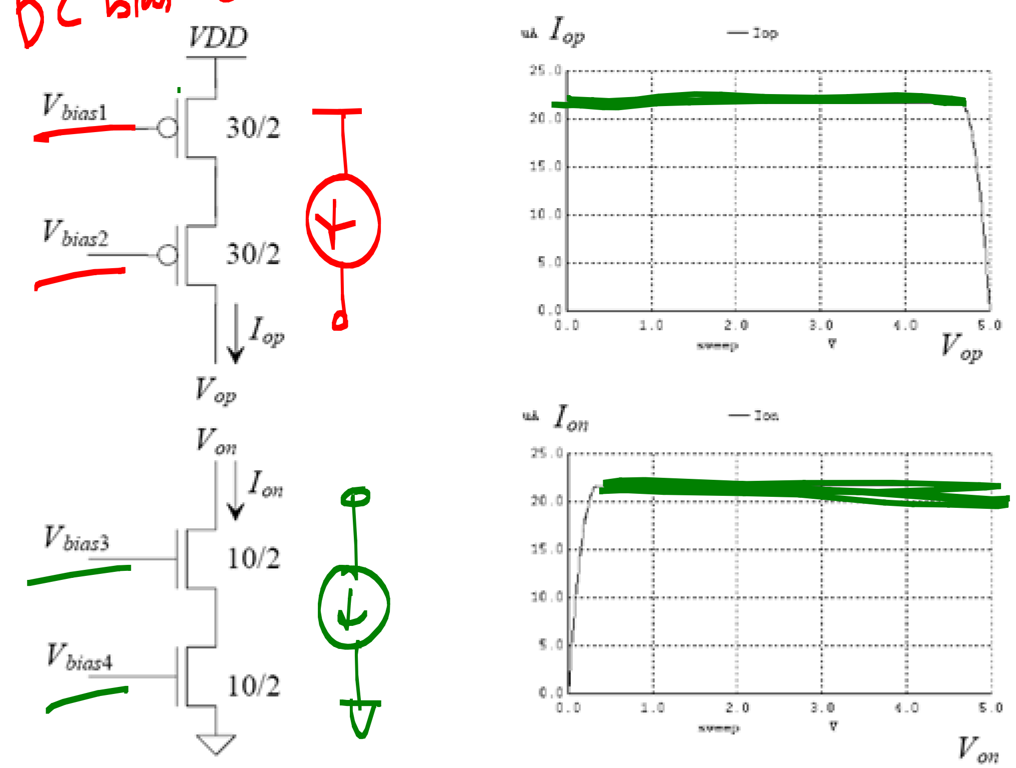


Figure 20.43 General biasing circuit for long-channel CMOS design using the data in Table 9.1



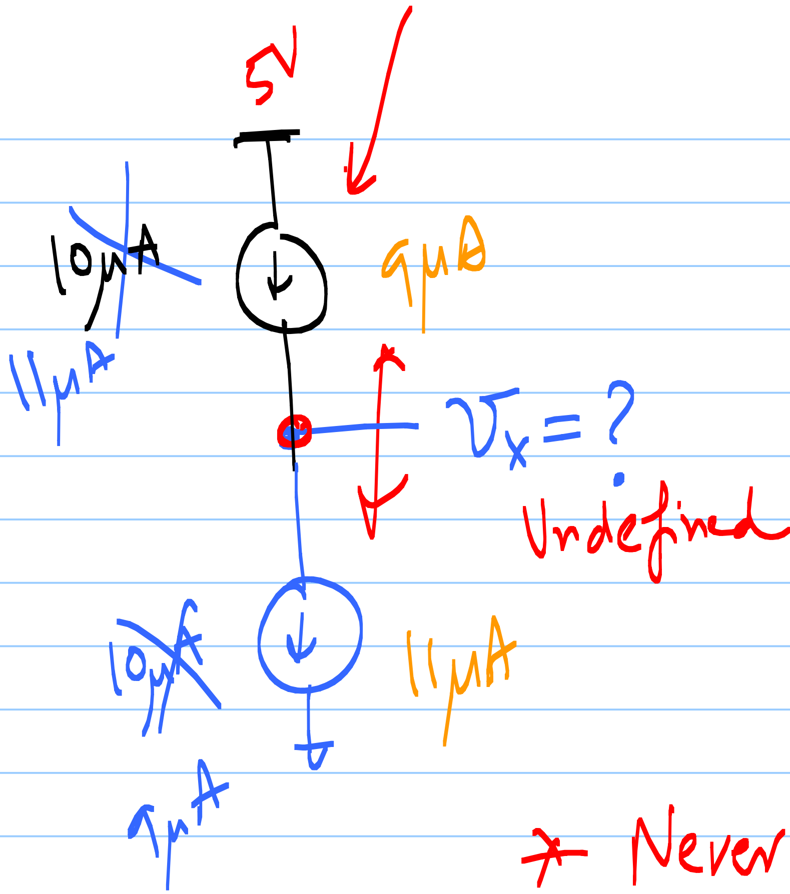
Vbiasp
BMF
MWS
W/25L
fixed
Vbias5
Vds,sat
Bias gen
gm ro^2
Io
Vo
Vgs
Vbias4
Vgs
RDCM

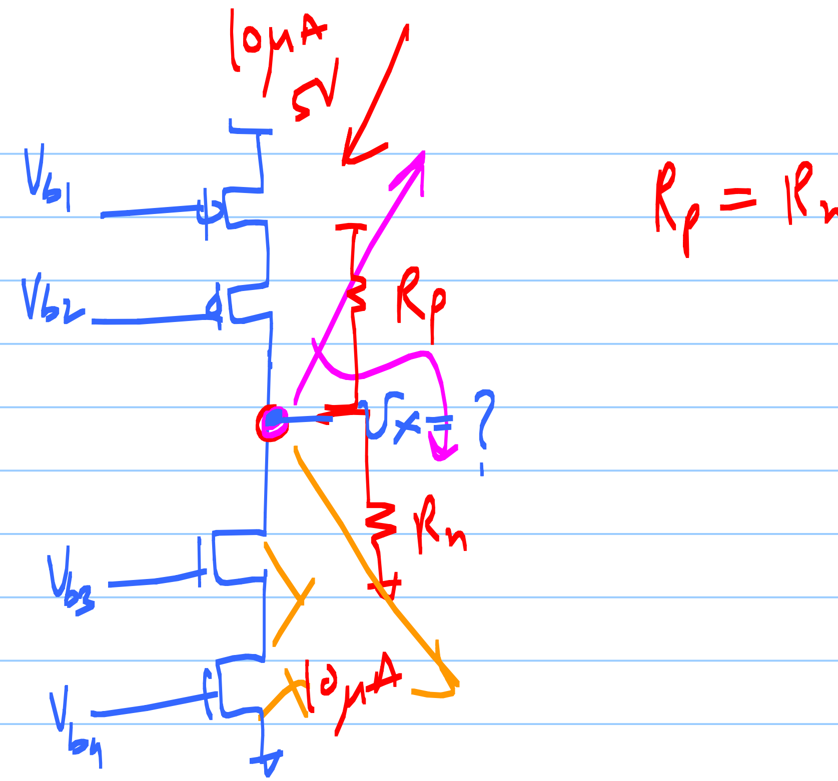
DC bias levels



Bias voltages come from Fig. 20.43 (long-channel parameters in Table 9.1).

Figure 20.44 How cascode currents are biased and how they operate.





* Never have two independent current source fight each other