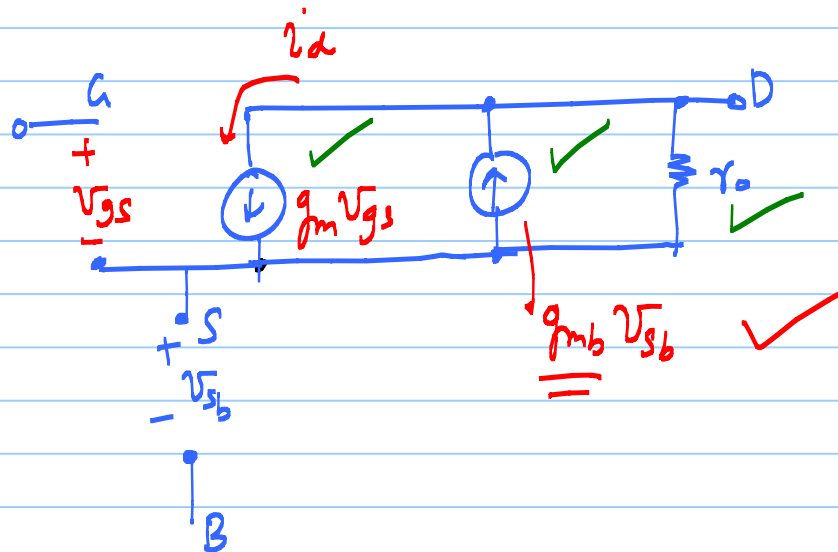
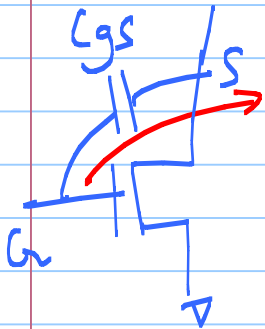


ECE 511 - Lecture 5

Note Title

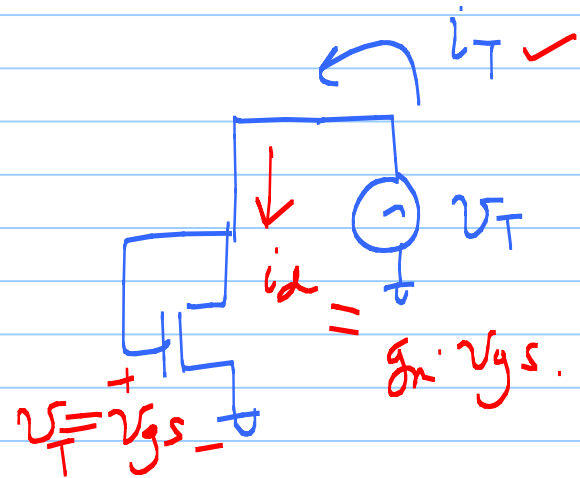
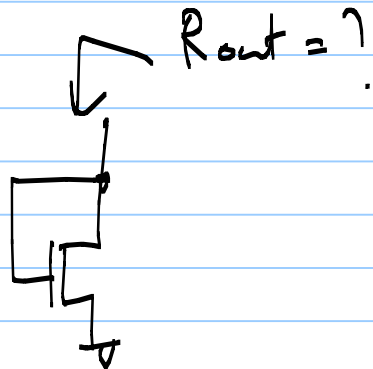
2/1/2012



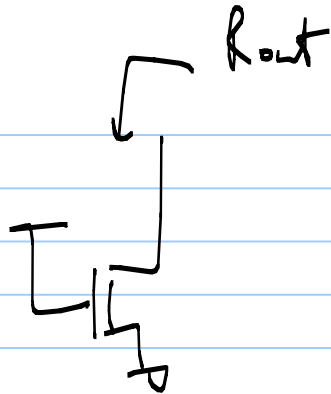
Small-signal
equivalent circuit for
NMOS

(low frequency) ✓

Diode Connected load :



$$R_{out} = \frac{v_T}{i_T} = \frac{v_{gs}}{i_d} = \frac{1}{g_m}$$



$$R_{out} = R_{ch} = \frac{1}{K P_n \frac{W}{L} (V_{GS} - V_{THN})}$$

$$\approx \frac{1}{g_m}$$

||
⋮

γ_0

$$\gamma_0 = \frac{1}{\lambda I_{Dsat}}$$

$$\lambda \propto \frac{1}{L}$$

$$I_{Dsat} = \frac{k_p}{2} \frac{W}{L} V_{DS,sat}^2$$

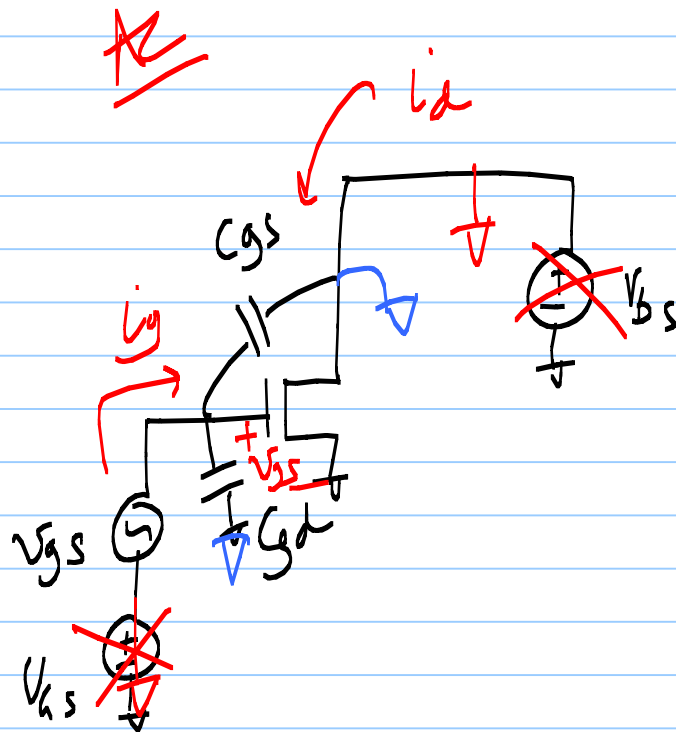
$$\gamma_0 \propto \frac{L^2}{V_{DS,sat}^2}$$

$$\propto \frac{V_{DS,sat}^2}{L}$$

$$L \uparrow \Rightarrow \gamma_0 \uparrow$$

$$V_{DS,sat} \uparrow \Rightarrow \gamma_0 \downarrow$$

MOSFET Transition frequency, f_T



$$@ f = \underline{\underline{f_T}} \quad \underline{\underline{\left| \frac{i_d}{i_g} \right| = 1}}$$

$$v_{gs} = i_g \cdot \frac{1}{s(C_{gd} + C_{gs})} \rightarrow \textcircled{1}$$

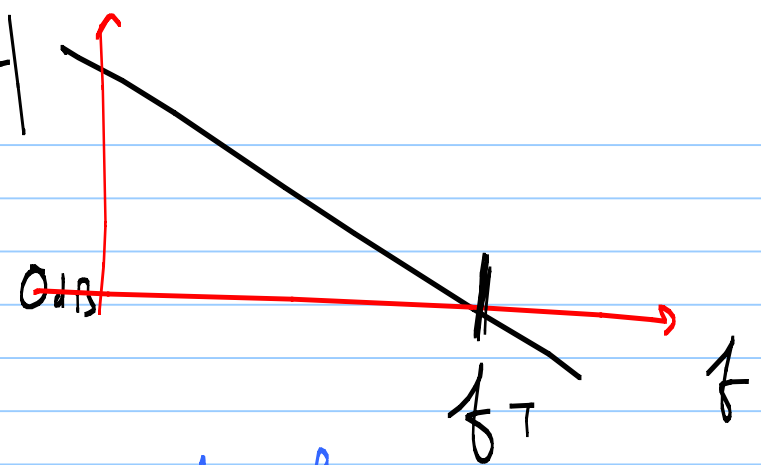
$$i_d = g_m v_{gs}$$

$$i_d = g_m \cdot \frac{i_g}{s(C_{gd} + C_{gs})}$$

$$\Rightarrow \left| \frac{i_d}{i_g} \right| = \left| \frac{g_m}{s(C_{gs} + C_{gd})} \right| = 1$$

$$\Rightarrow \frac{g_m}{2\pi f_T (C_{gs} + C_{gd})} = 1$$

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})}$$



$$@ f = f_T$$

$$\approx \frac{g_m}{2\pi C_{gs}}$$

$$\frac{C_{gs}}{\frac{2}{3} C_{ox}' WL} \gg \frac{\cancel{C_{gd}}}{C_{gd0} \cdot W}$$

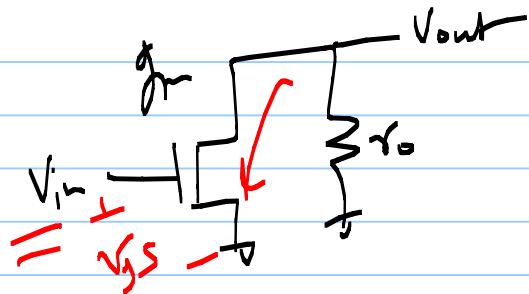
$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{3\mu_n}{4\pi} \frac{V_{DS,sat}}{L^2}$$

(Long-L MOSFET)

$L = L_{min}$ for maximum speed

$$f_T < \mu_n$$

$$\frac{f_{T_n}}{f_{T_p}} = \frac{\mu_n}{\mu_p} < 1$$



$$A_o =$$

$$A_o = g_m r_o \quad \uparrow \quad \downarrow$$

$$\begin{aligned} V_{out} &= -i_d r_o \\ &= -g_m V_{gs} r_o \\ &= -(g_m r_o) V_{in} \end{aligned}$$

$$\frac{V_{out}}{V_{in}} = -\boxed{g_m r_o} \leftarrow \text{open-loop gain of the MOSFET.}$$

$$(g_m r_o) f_T = \text{Constant}$$

$$GFT = \text{Constant.}$$

$$\Rightarrow L = 2 \text{ to } 5 \text{ times } L_{\min}$$

$$V_{ov} = V_{os, \text{sat}} = \begin{cases} \checkmark 5\% \text{ of } V_{DD} \Rightarrow \text{fast design} \\ \checkmark 1\% \text{ of } V_{DD} \Rightarrow \text{low-power} \end{cases}$$

Temperature Effects

$$I_{Dsat} = \frac{\mu_n}{2} C_{ox} \frac{W}{L} (V_{as} - V_{THN})^2$$

$\frac{\mu_n}{2}$ (green circle) $\swarrow$ $\frac{\epsilon_{ox}}{t_{ox}}$ (red) $\checkmark$ $\checkmark$

$$V_{THN} = -V_{ms} - 2V_{fp} + \frac{Q_b' - Q_{ss}'}{C_{ox}'}$$

$-V_{ms}$ (red circle) $\quad C_{ox}'$ (blue arrow) 10^{20}

$$\frac{\partial V_{THN}}{\partial T} = -\frac{k}{q} \ln \left(\frac{N_{D, poly}}{N_A} \right)$$

$N_{D, poly}$ (blue arrow) 10^{20} N_A (blue arrow) 10^{15}

$$\approx -1 \text{ mV}/^\circ\text{C}$$

$$\mu(T) = \mu(T_0) \left(\frac{T}{T_0} \right)^{-3/2}$$

$$T \uparrow \Rightarrow \mu_n \downarrow$$

$$\Rightarrow V_{THN} \downarrow$$

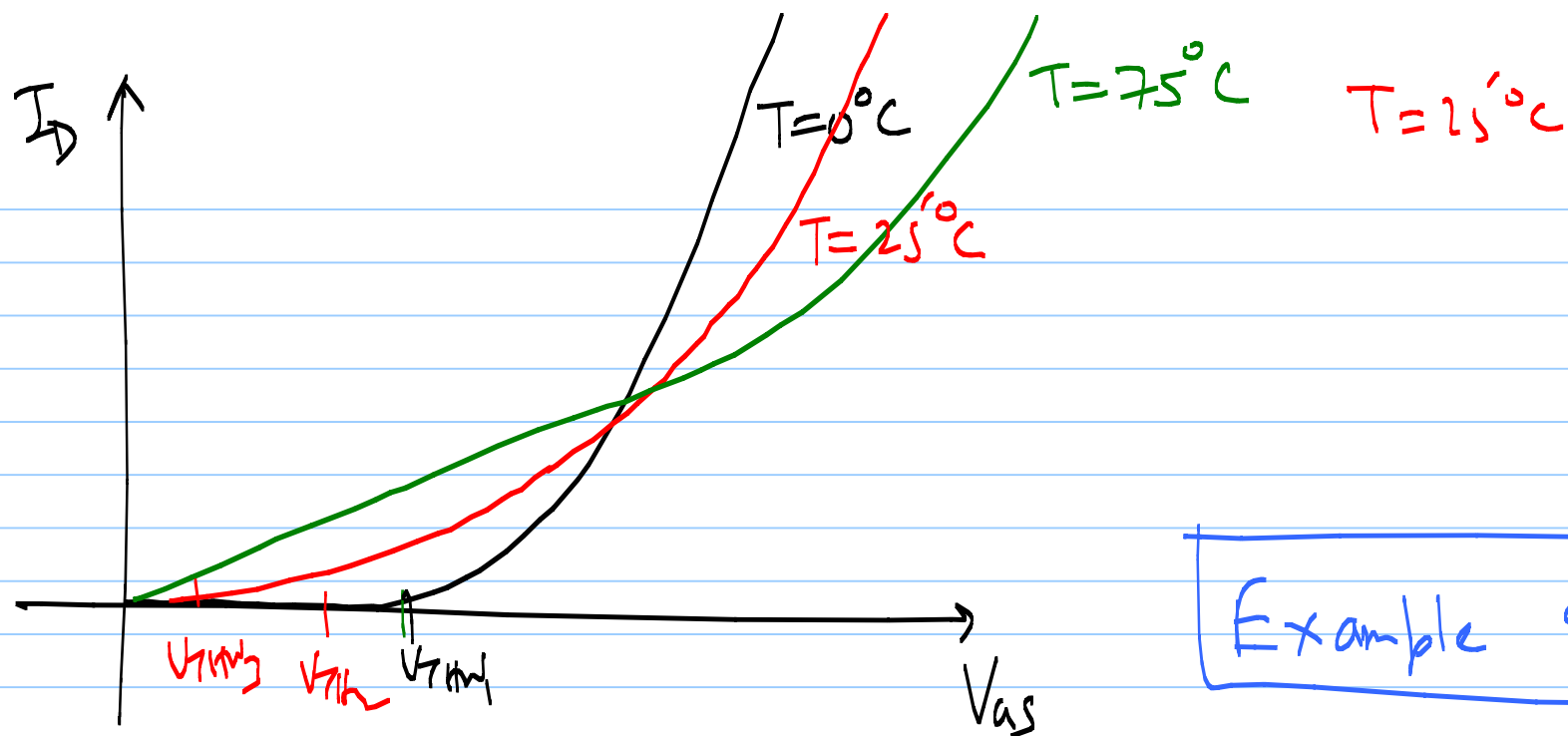
$$I_D = \frac{\overbrace{\mu_n C_{ox}}^{K_{Pn}}}{2} \frac{W}{L} (\underline{V_{as}} - V_{THN})^2$$

$$\frac{\partial I_D}{\partial T} = \frac{\partial K_{Pn}}{\partial T} \left[\frac{1}{2} \frac{W}{L} (V_{as} - V_{THN})^2 \right] - \left[\frac{K_{Pn}}{2} \cdot \frac{W}{L} \cdot 2 (V_{as} - V_{THN}) \right] \cdot \frac{\partial V_{THN}}{\partial T}$$

$$\frac{\partial I_D}{\partial T} = \frac{W}{L} (V_{GS} - V_{THW}) \left[\underbrace{\frac{1}{2} (V_{GS} - V_{THW})}_{\text{pink underline}} \cdot \left(\frac{\partial K P_n}{\partial T} \right) - K P_n \cdot \underbrace{\left(\frac{\partial V_{THW}}{\partial T} \right)}_{\text{red bracket}} \right]$$

@ low $V_{GS} \Rightarrow \frac{\partial V_{THW}}{\partial T}$ dominates

@ large $V_{GS} \Rightarrow \frac{\partial K P_n}{\partial T}$ dominates



Example 9.30

GFT:

Section 9.2.2

$$GFT = g_m r_o \cdot f_T$$

Long-L process

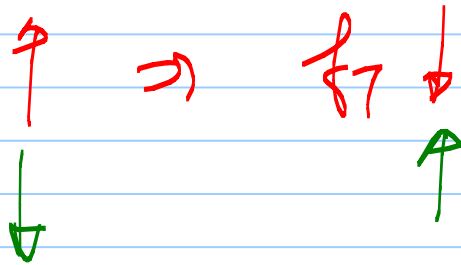
$$GFT = g_m r_o f_T = \cancel{g_m} \cdot \frac{g_m^2}{2\pi G_s} \cdot \frac{1}{\lambda I_D} = \frac{3\mu_n}{2\pi L^2 \lambda} \propto \frac{\mu_n}{L}$$

$GFT \propto \frac{\mu_n}{L}$

← Long-L CMOS

for a device with fixed $L \Rightarrow g_{FT} = \text{constant}$

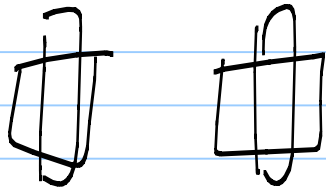
$$g_m r_o \uparrow \Rightarrow f_T \downarrow$$



for short channel CMOS $\Rightarrow$

$$V_{ov} \Rightarrow f_T \uparrow \quad g_{m,r} \downarrow$$

$$G_{FT} \uparrow \quad V_{ov} \uparrow$$



Short-channel CMOS

- * Lower $g_{m,r}$ $L = L_{min}$
- * higher mismatch
- * Voltage headroom shrinks

$\frac{g_m}{I_D}$ methodology

$$g_m = \frac{2I_D}{V_{OV}}$$

$$\left(\frac{g_m}{I_D}\right) = \left(\frac{2}{V_{OV}}\right)$$