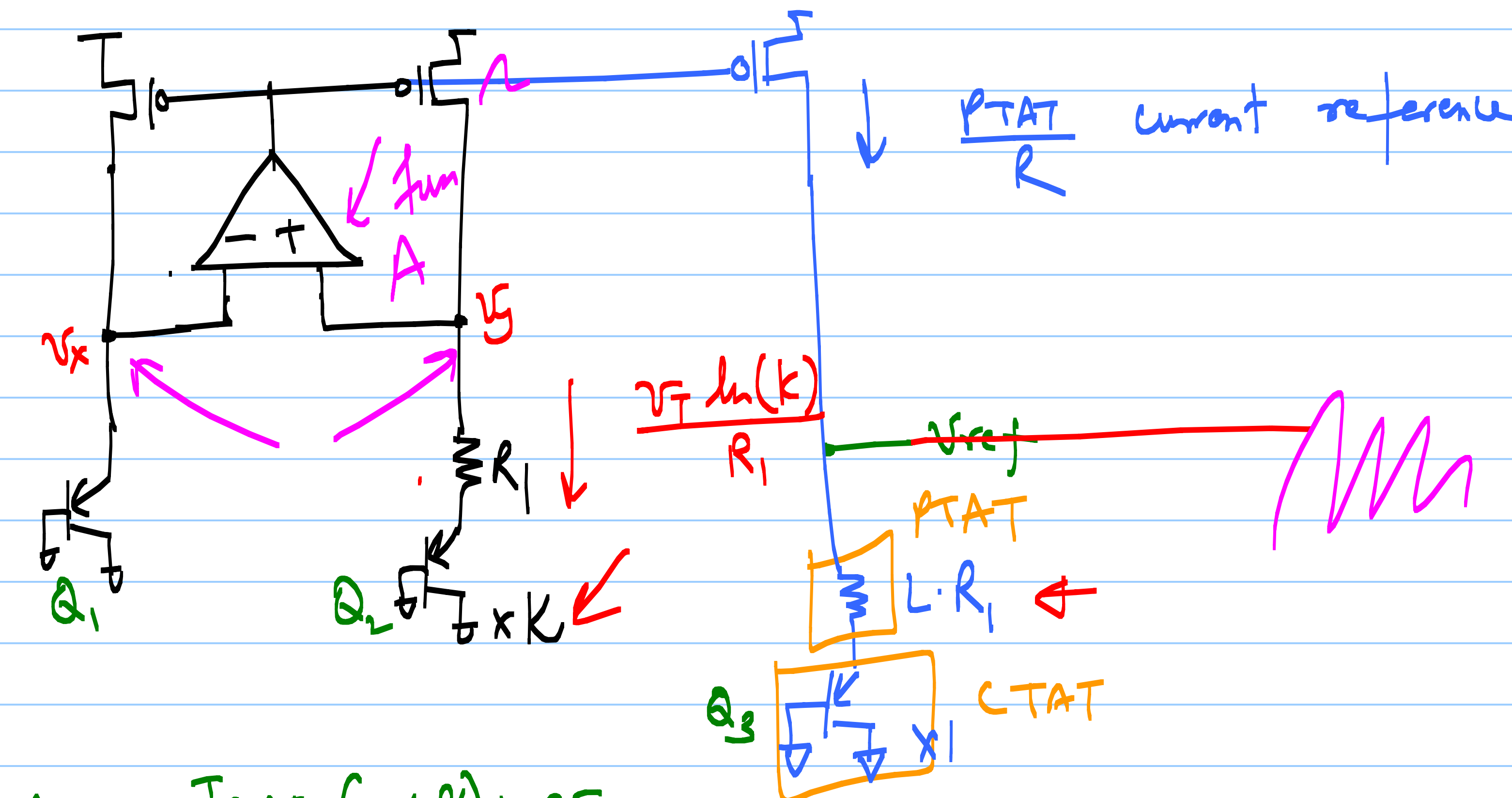
ECE 511 – Lecture 25 (Final Lecture)

Note Title 5/2/2012



$$V_{ref} = \frac{I_{PTAT}}{R_1}\left(L R_1\right) + V_{BE_3} = V_T \ln(K) \cdot L + V_{BE_3}$$

$$V_{ref} = \underbrace{V_T}_{PTAT}\,\underbrace{\ln(K)\cdot L}_{\alpha_2} + \underbrace{V_{BE_3}}_{CTAT}$$

for $\frac{\partial V_{ref}}{\partial T} = 0 \Rightarrow$ $\underbrace{\left(\frac{k}{q}\right)}_{0.085\ mV/°K} \cdot \ln(K)\,L + \underbrace{\frac{\partial V_{BE_3}}{\partial T}}_{-1.5\ mV/°K} = 0$

$\Rightarrow \quad \ln(K)\cdot L = 17.2$

for $L = 5$, $\quad K = e^{17.2/5} = e^{3.5} = 33$

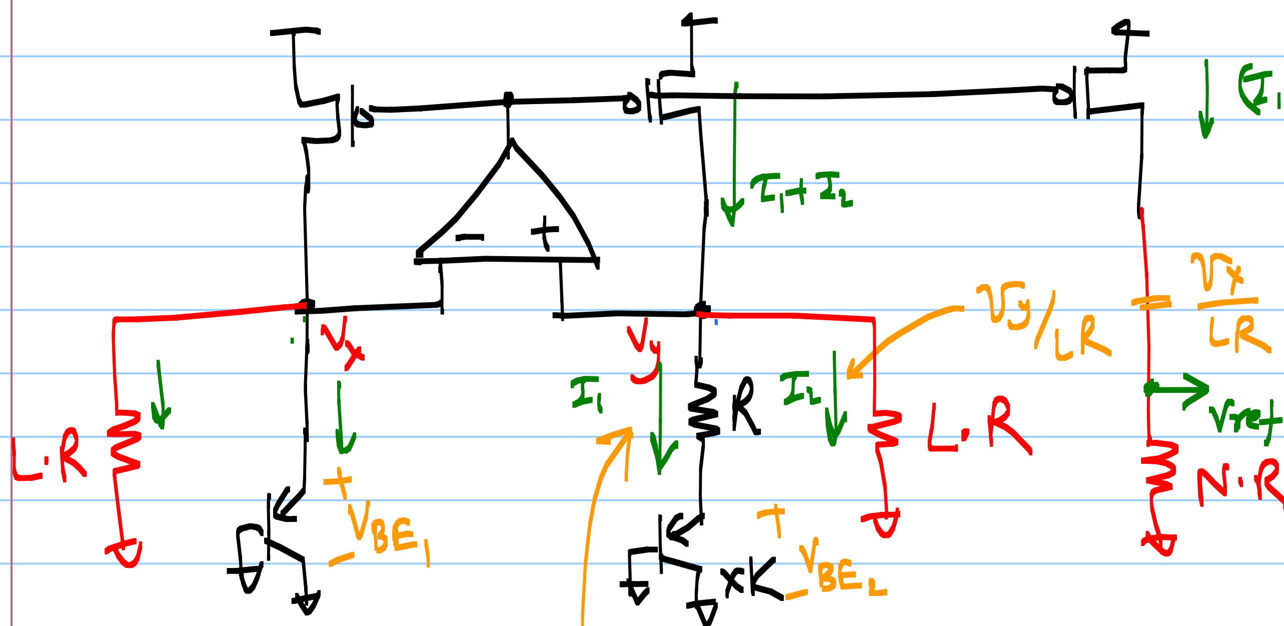
$K = 33$, $\quad L = 5$

$V_{ref} = V_{BE_3} + V_T \times 17.2$ (V_T = 26 mV)

$= 0.7 + 0.026 \times 17.2 = \boxed{1.25\ V}$

Short channel BGR ($V_{DD} \le 1V$)

$V_x = V_y$



$V_y / LR = \frac{V_x}{LR} = \frac{V_{BE_1}}{LR} = I_2$

$\frac{CTAT}{R}$ current

$V_x = V_y \Rightarrow \frac{V_T \ln K}{R}$ ← $I_1 = \frac{PTAT}{R}$ current

$V_{ref} = (I_1 + I_2)\, N \cdot R$

$$V_{ref} = \left(\frac{V_T \ln K}{R} + \frac{V_{BE_1}}{L \cdot R} \right) N \cdot R$$

$$V_{ref} = V_T \cdot \underbrace{N \ln(K)}_{\alpha_2} + \underbrace{\frac{N}{L}}_{\alpha_1} \cdot V_{BE_1}$$

$N, K, L = ???$

for $\frac{\partial V_{ref}}{\partial T} = 0 \Rightarrow \left(\frac{k}{q}\right) N \cdot \ln(K) + \frac{N}{L} \cdot \left(\frac{\partial V_{BE_1}}{\partial T}\right) = 0$

$$\Rightarrow L = \frac{1.5\ \text{mV}/°\text{K}}{\ln(K) \cdot 0.085\ \frac{\text{mV}}{°\text{K}}}$$

$$\Rightarrow \underline{L \cdot \ln(K) = 17.2}$$

Let's choose $\boxed{K=8}$ ✓ $\Rightarrow$ $\boxed{L = 9.41}$ (K, L) ☆

$V_{ref} = V_T \ln(K) \cdot N + \left(\frac{N}{L}\right) V_{BE_1}$

$\alpha_1 < 1$

By design 550 mV

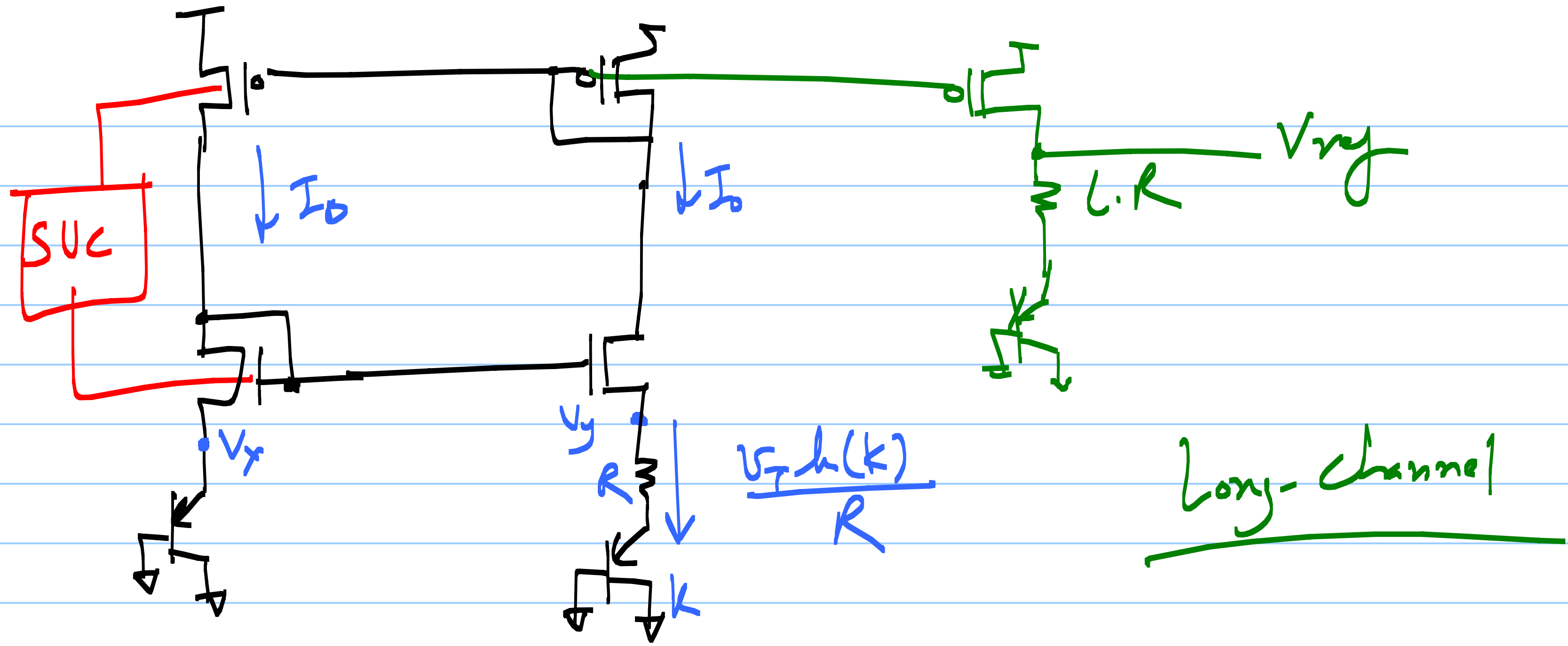
$\Rightarrow N = \dfrac{V_{ref}}{V_T \ln K + \frac{V_{BE}}{L}} = 3.91$ (V_{BE} ← 0.7V)

$\boxed{N = 3.91}$

$\boxed{V_{ref} = 500 \text{ mV}}$

* No unique solution

BMR-type design:



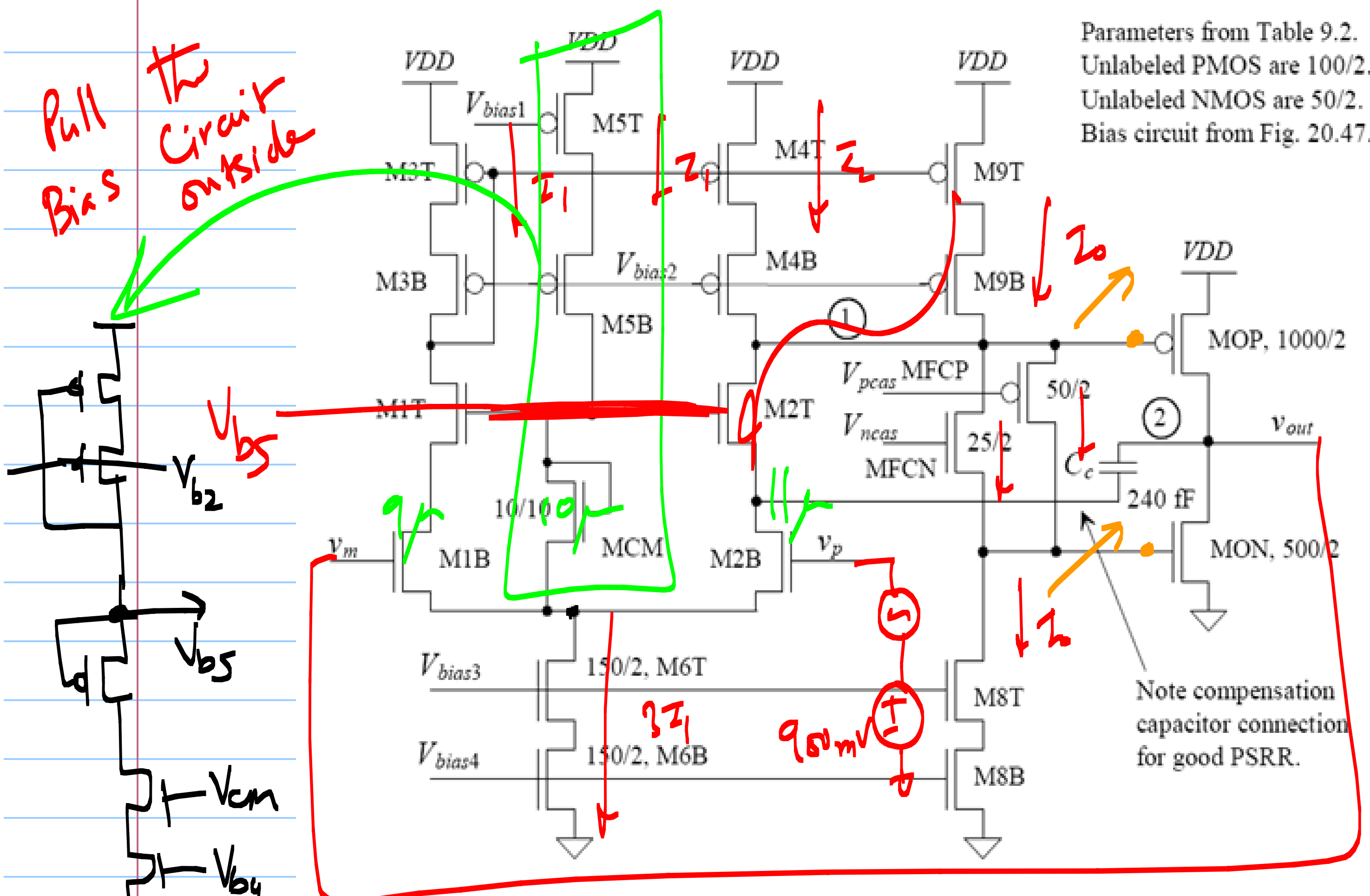


Figure 24.29 A CMOS op-amp with output buffer.

fixed V_{ov}

↳ 5% V_{DD}

↳ 90 mV

↓ + V_{THN}, V_{THP}

V_{as} = 350 mV

V_{sat} = 400 mV

I = 10 μA

$\left(\frac{W}{L}\right)_n$ $\left(\frac{W}{L}\right)_p$

ADE L ⇒ Results → Show Op points

↳ Print

g_m

g_{ds} is high ⇒ Triode

g_{ds} ← r_o^{-1}

g_{ds} is low ⇐

Caps

Deep Saturation

Fix

V_{ov}

50n

70% V_{DD}

Table 9.2 Typical parameters for analog design using the *short-channel* CMOS process discussed in this book. These parameters are valid only for the device sizes and currents listed.

Short-channel MOSFET parameters for general analog design VDD = 1 V and a scale factor of **50 nm** (*scale* = 50e–9)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias current, I_D	10 µA	10 µA	Approximate, see Fig. 9.31
W/L	50/2	100/2	Selected based on I_D and V_{ov}
Actual W/L	2.5µm/100nm	5µm/100nm	L_{min} is 50 nm
$V_{DS,sat}$ and $V_{SD,sat}$ V_{ovn} and V_{ovp}	50 mV 70 mV	50 mV 70 mV	However, see Fig. 9.32 and the associated discussion
V_{GS} and V_{SG}	350 mV	350 mV	No body effect
V_{THN} and V_{THP}	280 mV	280 mV	Typical
$\partial V_{THN,P}/\partial T$	– 0.6 mV/C°	– 0.6 mV/C°	Change with temperature
v_{satn} and v_{satp}	110 x 10^3 m/s	90 x 10^3 m/s	From the BSIM4 model
t_{ox}	14 Å	14 Å	Tunnel gate current, 5 A/cm^2
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	25 fF/µm^2	25 fF/µm^2	$C_{ox} = C'_{ox} WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	6.25 fF	12.5 fF	PMOS is two times wider
C_{gsn} and C_{sgp}	4.17 fF	8.34 fF	$C_{gs} = \frac{2}{3} C_{ox}$
C_{gdn} and C_{dgp}	1.56 fF	3.7 fF	$C_{gd} = CGDO \cdot W \cdot scale$
g_{mn} and g_{mp}	150 µA/V	150 µA/V	At I_D = 10 µA
r_{on} and r_{op}	167 kΩ	333 kΩ	Approximate at I_D = 10 µA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	25 V/V	50 V/V	!!Open circuit gain!!
λ_n and λ_p	0.6 V^{-1}	0.3 V^{-1}	L = 2
f_{Tn} and f_{Tp}	6000 MHz	3000 MHz	Approximate at L = 2

$f_T \propto \frac{V_{OV}}{L}$ $\quad L_{min} = 180n$ $\qquad g_m r_o \propto \frac{L}{V_{OV}}$

$f_{in} \simeq \frac{f_T}{10}$

fixed V_{ov}

$$g_m = \frac{2 I_D}{V_{ov}}$$

$$\Rightarrow \left(\frac{g_m}{I_D}\right) = \frac{2}{V_{ov}}$$

fixed $\left(\frac{g_m}{I_D}\right)$ ratio ← independent of W

↳ $\left(\frac{g_m}{I_D}\right)$ method for sizing.