Homework 7

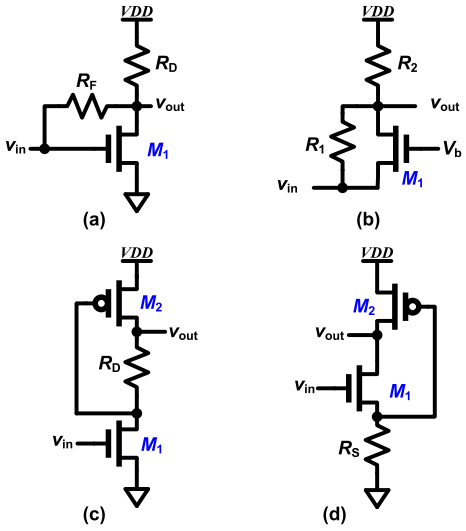
ECE 5411 – CMOS Analog IC Design (Spring 2012)

Due on Wednesday, Mar 21, 2012.

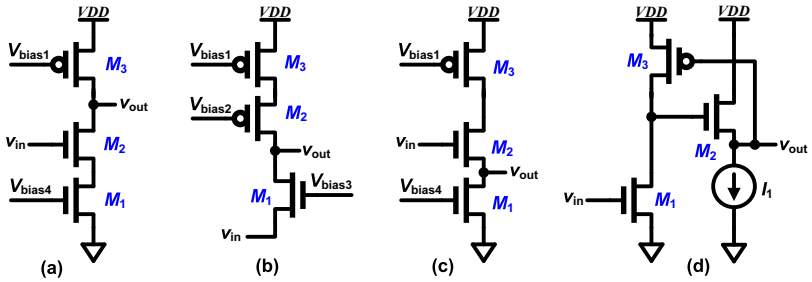
Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

Problems A: Do problems A21.14 and A21.16. Simulate **only one** of the problems.

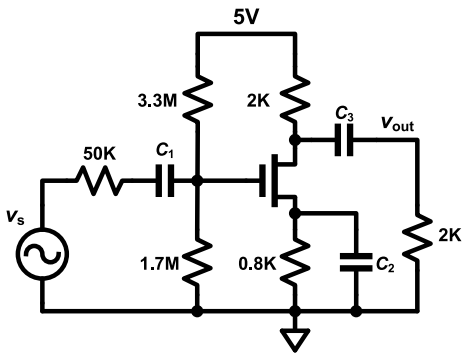
Problem B1: Assuming all transistors are in saturation, find small-signal voltage gain for each of the circuits shown below. Use variables g_{m1}, r_{o1}, g_{m2}, r_{o2}, etc.



Problem B2: Assuming all transistors are in saturation, find small-signal voltage gain for each of the circuits shown below. Use variables g_{m1}, r_{o1}, g_{m2}, r_{o2}, etc.



Problem B3: The NMOS in the figure below has $V_{THN} = 0.7V$, and $KP_n = 500\mu A/V^2$. The drain current in the device is 1mA.



a) Determine the small signal gain from v_s to v_{out}.

b) Determine the W/L for the device and the DC operating points V_{GS} and V_{DS}.

c) The lowest frequency in v_s is ω_{in} =100rad/s. Determine the minimum values of C_1, C_2 and C_3required so that the frequencies associated with their charging/discharging is at least 10 times smaller than ω_{in}.

d) The supply voltage is changed to 5.5. Determine the small signal gain of the amplifier.