Homework 6

ECE 5411 – CMOS Analog IC Design (Spring 2011)

Due on Monday, Mar 7, 2011.

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

Problems A: Do problems A20.27, A20.28, A21.1, A21.3, A21.5 and A21.7 from the extra problem set available on the textbook website. Simulate **only one** of the problems A21.1-A21.7, others are optional.