Homework 1

ECE 5411 – CMOS Analog IC Design (Spring 2011)

Due on Monday, Jan 24, 2011.

Note: Use Cadence schematic capture, layout and Spectre simulation tools, available on the AMS servers for the homework problems.

Problem 0: Mention your name, previous background in analog circuit design, and what do you expect to learn in this course?

Problems 1-2: Do problems A9.1-A9.2 from the extra problem set available on the textbook website.

Problem 3: Using the TSMC 180nm Spectre models, generate all the I-V curves for a 10/1 NMOS and a 10/1 PMOS. Do you expect long-channel or short-channel behavior from these devices? Give reasons.