ECE 5411 CMOS Analog Integrated Circuit Design
Sample Midterm 1
Mar 4, 2011 **Name:** _____

Closed Book, Closed Notes, Closed Computer. Show your steps clearly to get credit. State clearly any assumptions made. This exam has 6 questions, for a total of 100 points.

Use the following transistor parameters for problems in this exam. $V_{DD} = 5$V and scale factor of $1\mu m$.

Parameter	**NMOS**	**PMOS**
$V_{THN,P}$	0.8 V	0.9 V
$KP_{n,p}$	120 $\frac{\mu A}{V^2}$	40 $\frac{\mu A}{V^2}$
$\lambda_{n,p}$	0.01 V^{-1}	0.0125 V^{-1}

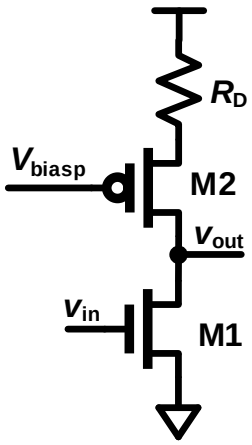
1. Answer the following parts:

   (a) (5 points) For an NMOS, sketch g_m vs V_{GS} plot. On this plot, label the g_m correspoding to a fixed gate overdrive voltage V_{ov}.

   (b) (5 points) Sketch g_m as a function of current (I_D) when the W/L ratio is constant.

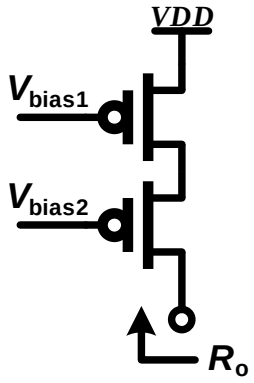
(c) (5 points) Explain the temperature behavior of a PMOS transistor using I_{DS} vs V_{GS} curves.

(d) (5 points) Find the small-signal gain of this amplifier in terms of g_m and r_o of the transistors.



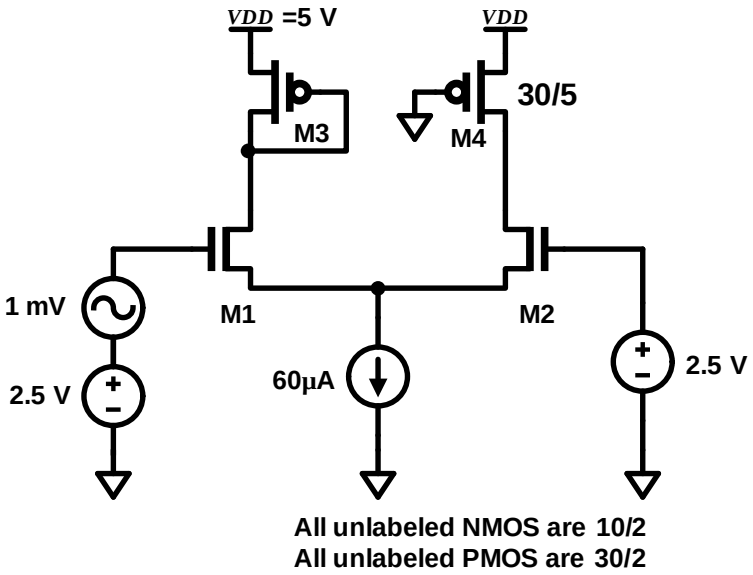
2. (10 points) Define the transition frequency (f_T) for an NMOS and derive an expression for f_T. How does f_T depends on the channel length (L) and the gate overdrive voltage (V_{ov})?

3. (a) (5 points) Sketch the circuit(s) used to generate references V_{bias1} and V_{bias2} from a beta-multiplier reference (BMR).

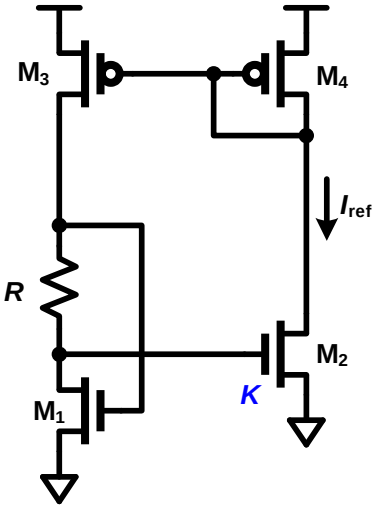


(b) (5 points) Derive an exact expression for the output resistance of the cascode current source seen above.

4. (20 points) Estimate all the DC and AC voltages in the circuit shown below. Ignore the device output resistances (r_o) in this problem.



5. Consider the beta multiplier reference (BMR) circuit shown in the figure below.

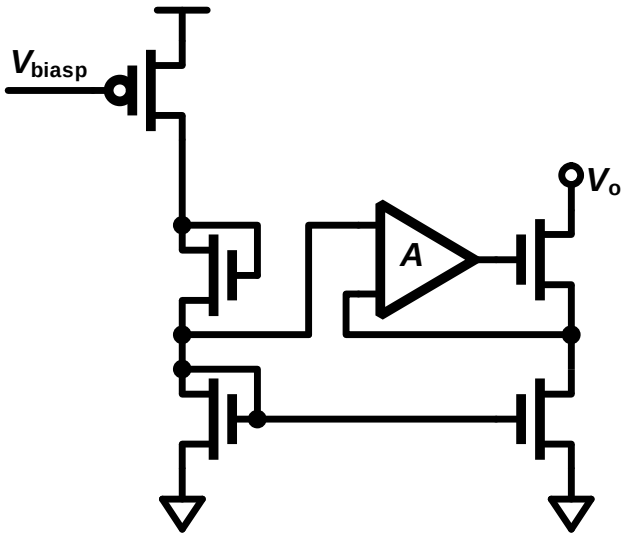


(a) (10 points) Derive expressions for I_{ref}, V_{GS_1} and g_{m1}. Note that M2 is K times wider than M1.

(b) (5 points) Draw the schematic for a start-up circuit for this BMR.

(c) (5 points) Modify this circuit to make it suitable for short-channel design.

6. Consider the regulated drain current mirror shown below.



(a) (3 points) Assign the positive and negative terminals on the amplifier to ensure overall negative feedback.

(b) (7 points) Label all the nodes in the circuits in terms of $V_{DS,sat}$ and V_{THN}. What is the allowable range for the voltage V_o?

(c) (10 points) Derive an expression for the output resistance of this current mirror.

(d) (0 points) **Bonus**: Sketch the PMOS and wide-swing version of this circuit.