# ECE 5411 CMOS Analog Integrated Circuit Design
## Sample Midterm 2
## Mar 7, 2011 Name: _____

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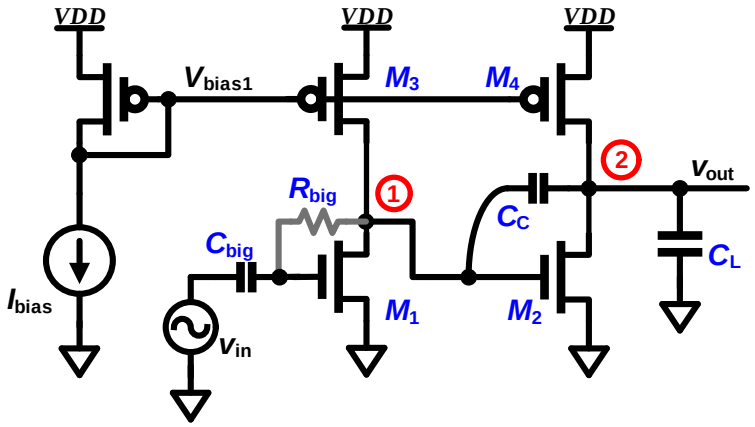
| Closed Book, Closed Notes, Closed Computer.<br>Show your steps clearly to get credit.<br>State clearly any assumptions made.<br>This exam has 5 questions, for a total of 100 points. |

1. Consider the Miller-compensated two-stage amplifier shown below,




The pole and zero expressions for the amplifier are given by

$\omega_z = +\frac{g_{m1}}{C_c}$

$\omega_{p_1} \approx \frac{1}{g_{m2}R_2R_1C_c}$

$\omega_{p_2} \approx \frac{g_{m2}C_c}{C_2(C_1+C_C)+C_CC_1} \propto \frac{g_{m2}}{C_2}$

(a) (5 points) Explain pole-splitting in this circuit, showing relevant pole-zero plot (s).

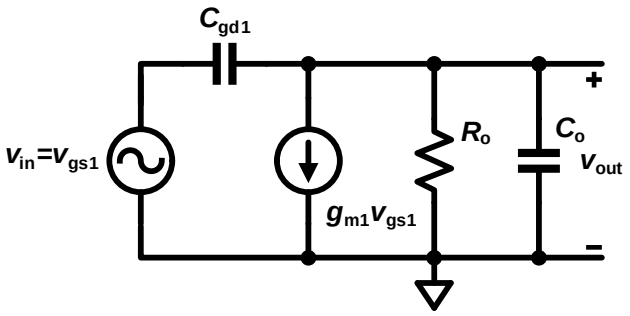
(b) (5 points) Looking at the circuit, qualitatively explain why does a feed-forward (Miller) cap lead to an RHP zero in a CS stage?

(c) (5 points) Qualitatively, why does the second pole ($\omega_{p_2}$) gets pushed to a frequency location roughly given by $\frac{g_{m2}}{C_2}$ ?

(d) (5 points) Assuming that the amplifier is dominant pole compensated, derive the expression for unity gain frequency ($f_{un}$).

(e) (0 points) Comment on the slew-rate limitation in this amplifier. How will you fix it?

2. (20 points) Solve for $\frac{v_{out}}{v_{in}}(s)$ in the following circuit. Find the locations of the pole ($\omega_p$) and zero ($\omega_z$). Assuming that $C_o \gg C_{gs1}$, sketch rough Bode magnitude and phase plots.

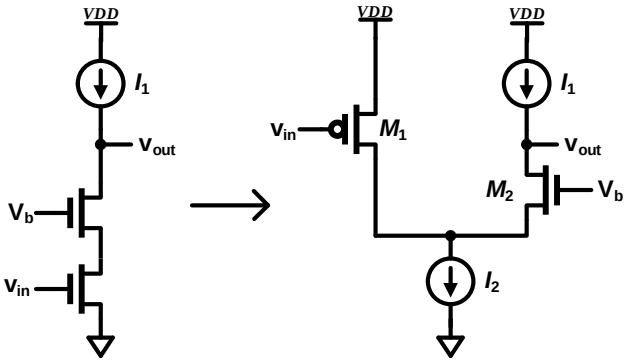


3. (a) (10 points) Derive and explain Miller capacitance multiplication effect in amplifiers with negative gain.

(b) (10 points) Why does a source follower (common-drain) amplifier have a low input capacitance? Use a circuit sketch to illustrate your answer.

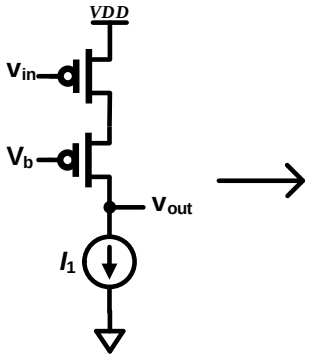
(c) (0 points) Why is Miller effect not a big contributor in a cascode common-source amplifier? Use a circuit sketch to illustrate your answer.

4. A cascode amplifier can be converted to its equivalent 'folded-cascode' topology for alleviating voltage swing limitations in the former. The figure below illustrates the translation of a single-ended NMOS cascode amplifier to its folded-cascode counterpart, where the input device is replaced by its PMOS equivalent.

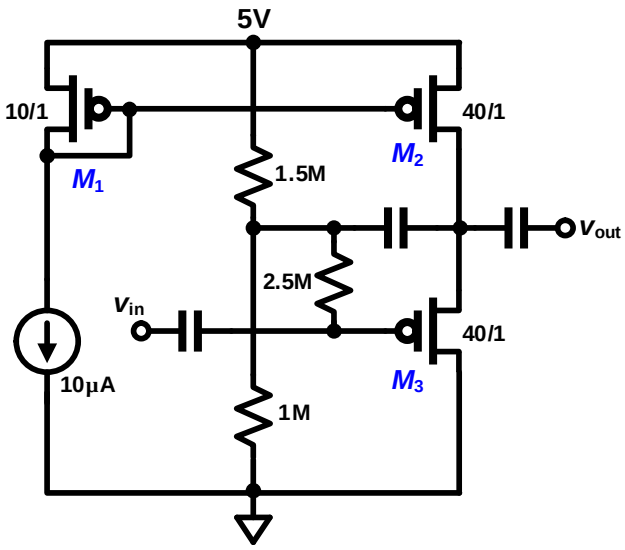



(a) (10 points) Find the small-signal gain of the folded-cascode amplifier (b) shown above, and compare it with the gain of the cascode amplifier (a). Assume that the current sources are ideal.

(b) (10 points) Draw the equivalent folded cascode amplifier for the PMOS cascode amplifier.



5. For the amplifier shown in the figure below:




$V_{THP} = 0.8V$, and $KP_p = 50\frac{\mu A}{V^2}$

Assume that the coupling capacitors are infinite.

(a) (5 points) Determine the operating points of all the devices in the circuit. For this part, neglect channel length modulation (i.e. $\lambda = 0$).

(b) (10 points) All transistors in the circuit have finite $r_o$, such that for any transistor $g_m r_o = 100$. Draw the small signal equivalent circuit of the amplifier and determine the small-signal gain ($A_v = \frac{v_{out}}{v_{in}}$).

(c) (5 points) Determine the input and output resistances of the amplifier.

(d) (0 points) Determine the amplitude of the largest sinusoid that can be applied at the input, so that the output is also a sinusoid, devoid of clipping effects.