Project 1

ECE 5/411 – CMOS Analog IC Design (Spring 2011)

Due on Wednesday, May 4, 2011.

1 Problem Statement

Design of a singly-ended Opamp: Signal processing applications like Continuous-time Delta-Sigma ADCs require opamps with high performance and linearity. Typically analog signal processing employs fully-differential opamps. However, in this project a singly-ended equivalent opamp has to be designed which satisfies the given specifications using TSMC 180-nm mixed-mode CMOS technology with a VDD=1.8 V supply voltage.

The target specifications for the singly-ended opamp are as follows:

Table 1: Opamp design specifications.

Parameter	**Specified Value**
Technology	TSMC 180n CMOS
Supply voltage, V_{DD}	1.8 V
Typical load	$5k\Omega \| \| 1pF$
Unit gain frequency (f_{un})	$> 100\,MHz$
Open-loop gain (A_{OL})	$> 60\,dB$
Slew-rate (SR)	$> 500\frac{V}{\mu s}$
Phase margin (ϕ_M)	$\gtrsim 63^\circ$
Power consumption	Minimum

2 Opamp Design

In your opamp design consider the following criterion:

1. Explore the opamp design space in the given technology. Select an appropriate topology which will meet the given specifications. If you are not able to meet any of the specifications, explain giving details. You may want to have a class-AB output buffer to drive the given load with rail-to-rail output swing.

2. Characterize the process and explain the transistor size selection in your design. Show the biasing circuits with appropriate simulations.

3. Explain your opamp design choices and the various architectural trade-offs, e.g. Telescopic vs Folded-cascode, etc.

4. Pay special attention to the compensation scheme which will provide you high-speed compensation with best possible slew-rate performance, e.g. Miller with zero-nilling R vs Indirect Cascode compensation vs Feed-forward compensation. Show necessary analysis, derivations and pole-zero, root locus, Bode, Nyquist plots etc.

5. Simulate the opamp in unity-gain feedback and comment on the frequency domain and transient stability. Argue why your method of determining stability will work for any feedback factor ($\beta \leq 1$). Characterize the design for small as well as large step inputs.

6. Characterize your design for metrics including Slew-rate, CMRR, PSRR, power consumption using an appropriate test benches [7].

7. Comment on the temperature behavior of the design for $0^\circ < T < 100^\circ C$).

3 Final Report

Submit your neatly typed report in a two-column IEEE transactions format [8]. Lyx has the IEEE transactions template (IEEEtran) built-in. Show crisply drawn schematics and block diagrams drafted using a professional tool like Visio, besides your Cadence schematics. You may download the Visio schematic symbols from the course website [9]. Provide relevant references in your report. Show the overall opamp performance in a neatly tabulated manner along with the conclusion.

4 Design Submission

Submit your design library zip by email on the due date (11:59 pm at the end of the day). The library should include all the neatly done schematics will the relevant test-benches. Include any Ocean scripts or MATLAB code developed to characterize the design.

References

[1] N. Krishnapura, S. Pavan, “Tutorial on Negative feedback system and circuit design,” at the 22nd International Conference on VLSI Design, Jan 2009, [Online]

[2] P. R. Gray and R. G. Meyer, "MOS operational amplifier design-A tutorial overview," IEEE Journal of Solid-State Circuits, vol. 17, pp. 969 - 982, December 1982.

[3] N. Krishnapura, “Opamp analysis and performance summary” [Online]

[4] V. Saxena, and R.J. Baker, "Compensation of CMOS Op-Amps using Split-Length Transistors,", proceedings of the 51st Midwest Symposium on Circuits and Systems, pp. 109-112, August 10-13, 2008.

[5] V. Saxena, "Indirect Compensation Techniques for Multi-Stage Operational Amplifiers," MS Thesis, Boise State University, 2007 [Online].

[6] B.K. Thandri, J. Silva-Martinez, "A robust feed-forward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," IEEE J. Solid-State Circuits, vol.38, no.2, pp. 237- 243, Feb 2003.

[7] “Functional Verification of a Differential Operational Amplifier,” Cadence Whitepaper [Online].

[8] IEEE Transactions Templates. Available [Online].

[9] Visio Schematic Symbols. Available [Online].