High Speed Op-amp Design: Compensation and Topologies for Two-Stage Designs

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Outline

- Introduction
- Two-stage Op-amp Compensation
- Conclusion

INTRODUCTION

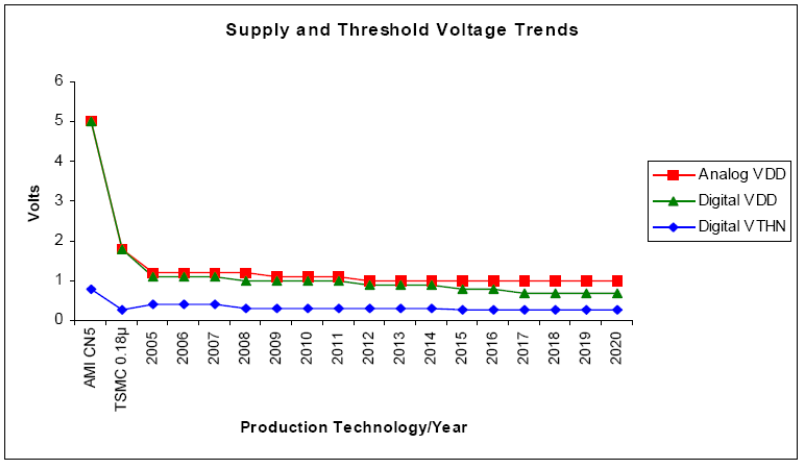
Op-amps and CMOS Scaling

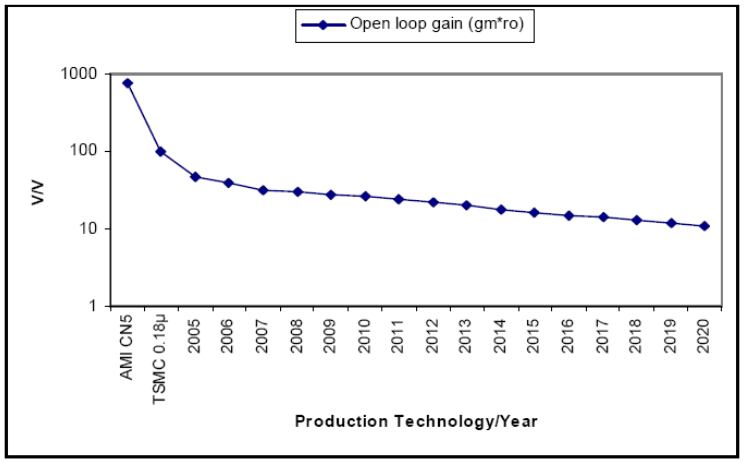
- The Operational Amplifier (op-amp) is a fundamental building block in Mixed Signal design.
  - ✓ Employed profusely in data converters, filters, sensors, drivers etc.
- Continued scaling in CMOS technology has been challenging the established paradigms for op-amp design.
- With downscaling in channel length (L)
  - ✓ Transition frequency increases (more speed).
  - ✓ Open-loop gain reduces (lower gains).
  - ✓ Supply voltage is scaled down (lower headroom) [1].

$$f_T \propto \frac{V_{ov}}{L}$$

$$g_m r_o \propto \frac{L}{V_{ov}}$$

CMOS Scaling Trends

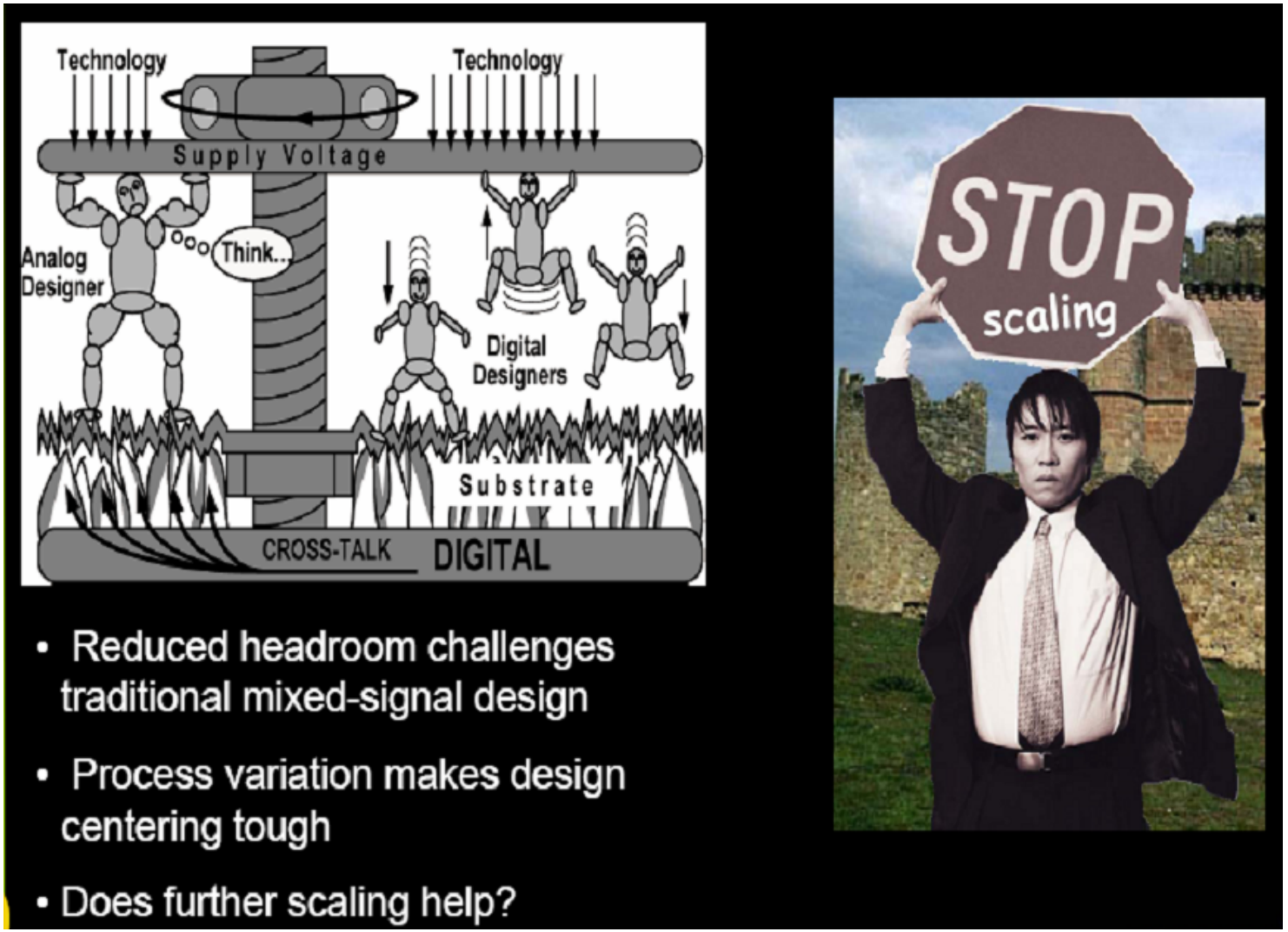




- VDD is scaling down but V_{THN} is almost constant.
  - ✓ Design headroom is shrinking faster.
- Transistor open-loop gain is dropping (~10's in nano-CMOS)
  - ✓ Results in lower op-amp open-loop gain. But we need gain!
- Random offsets due to device mismatches. $\sigma_{\Delta VTH} \propto \frac{1}{L \cdot W}$

[3], [4].

Analog Design Getting Squeezed With Scaling



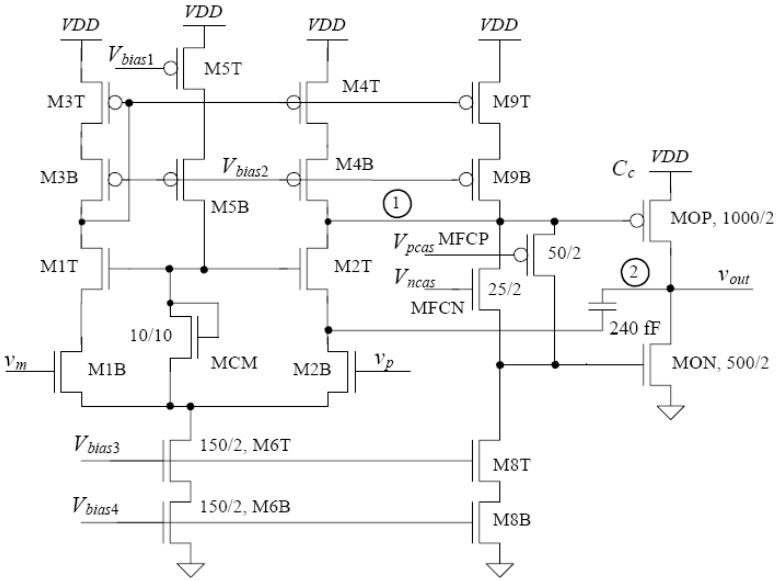
[5]

Integration of Analog into Nano-CMOS?

- Design low-VDD op-amps.
  - ✓ Replace vertical stacking (cascoding) by horizontal cascading of gain stages (see the next slide).
- Explore more effective op-amp compensation techniques.
- Offset tolerant designs.
- Also minimize power and layout area to keep up with the digital trend.
- Better power supply noise rejection (PSRR).

Cascoding vs Cascading in Op-amps

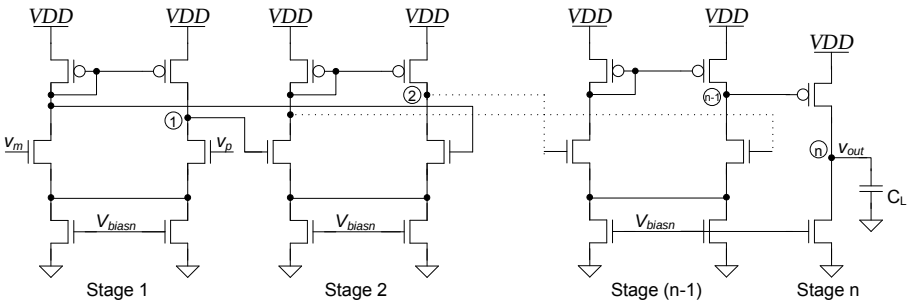
A Telescopic Two-stage Op-amp



$VDD_{min}>4V_{ovn}+V_{ovp}+V_{THP}$ with wide-swing biasing. [1]

A Cascade of low-VDD Amplifier Blocks.

(Compensation not shown here)

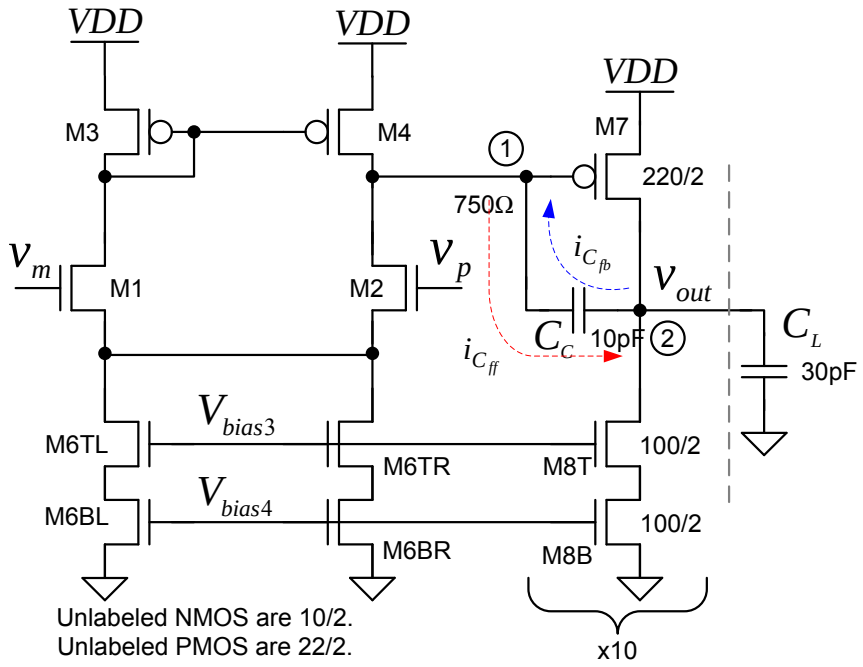


$VDD_{min}=2V_{ovn}+V_{ovp}+V_{THP}$.

- Even if we employ wide-swing biasing for low-voltage designs, three- or higher stage op-amps will be indispensable in realizing large open-loop DC gain.

TWO-STAGE OP-AMP COMPENSATION

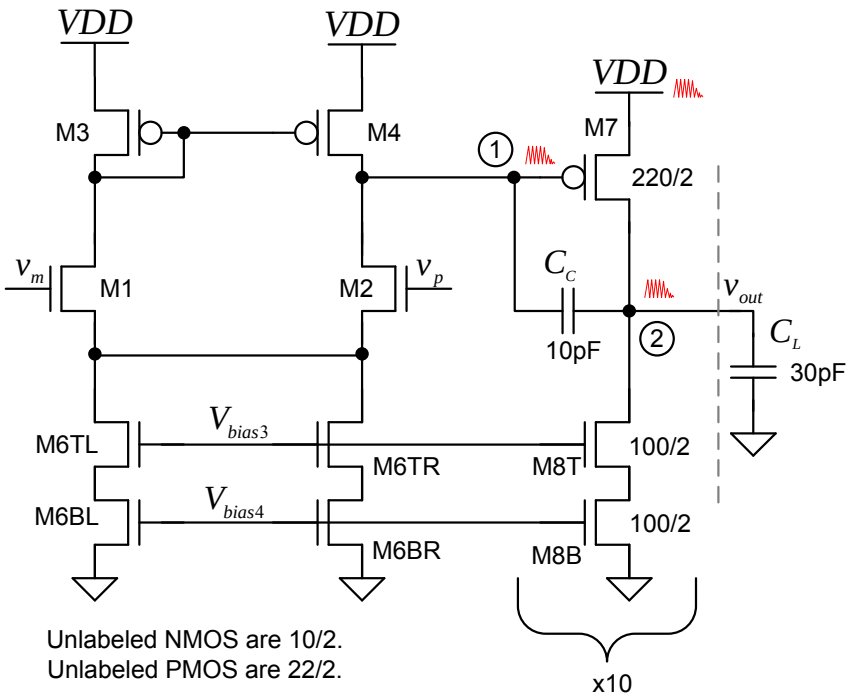
Direct (or Miller) Compensation



- Compensation capacitor (C_c) between the output of the gain stages causes pole-splitting and achieves dominant pole compensation.
- An RHP zero exists at $z_1 = \frac{g_{m2}}{C_c}$
  - ✓ Due to feed-forward component of the compensation current (i_C).
- The second pole is located at $-\frac{g_{m2}}{C_1 + C_c}$
- The unity-gain frequency is $f_{un} = \frac{g_{m1}}{2\pi C_c}$
- A benign undershoot in step-response due to the RHP zero

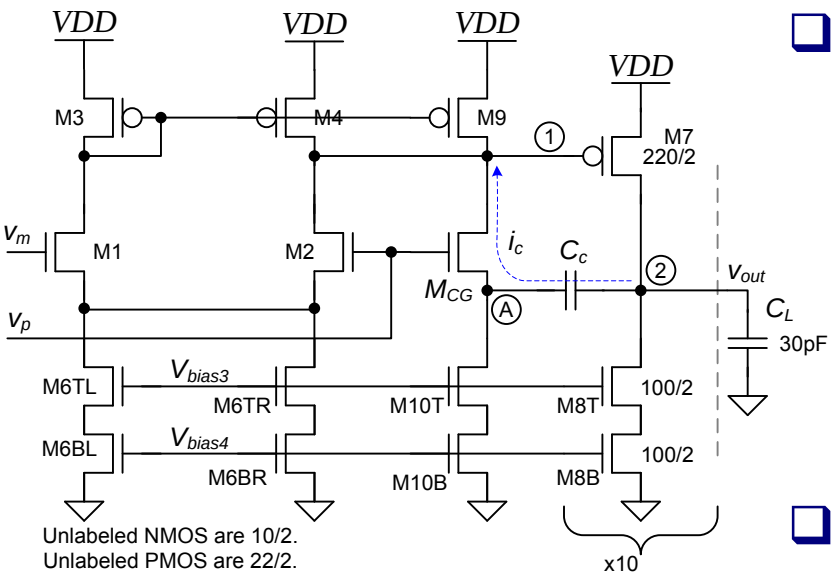
❖All the op-amps presented have been designed in AMI C5N 0.5μm CMOS process with scale=0.3 μm and L_{min}=2. The op-amps drive a 30pF off-chip load offered by the test-setup.

Drawbacks of Direct (Miller) Compensation



- The RHP zero decreases phase margin
  - ✓ Requires large C_C for compensation (10pF here for a 30pF load!).
- Slow-speed for a given load, C_L.
- Poor PSRR
  - ✓ Supply noise feeds to the output through C_C.
- Large layout size.

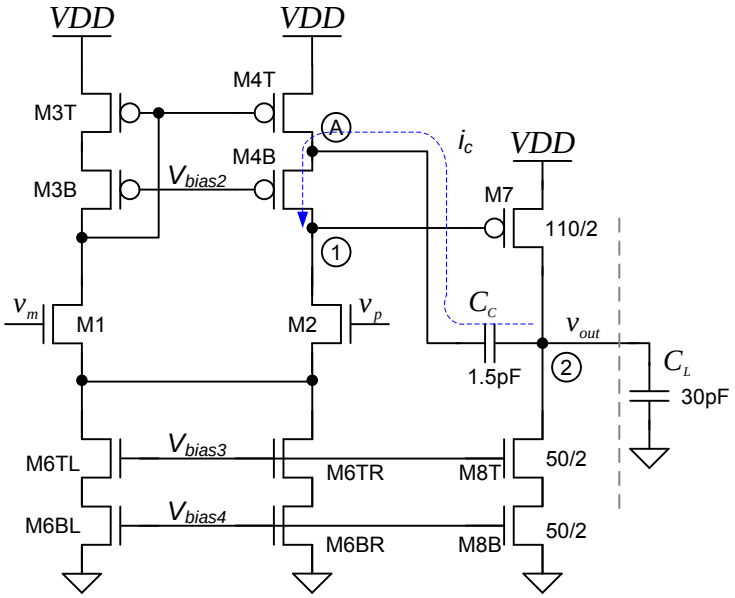
Indirect Compensation



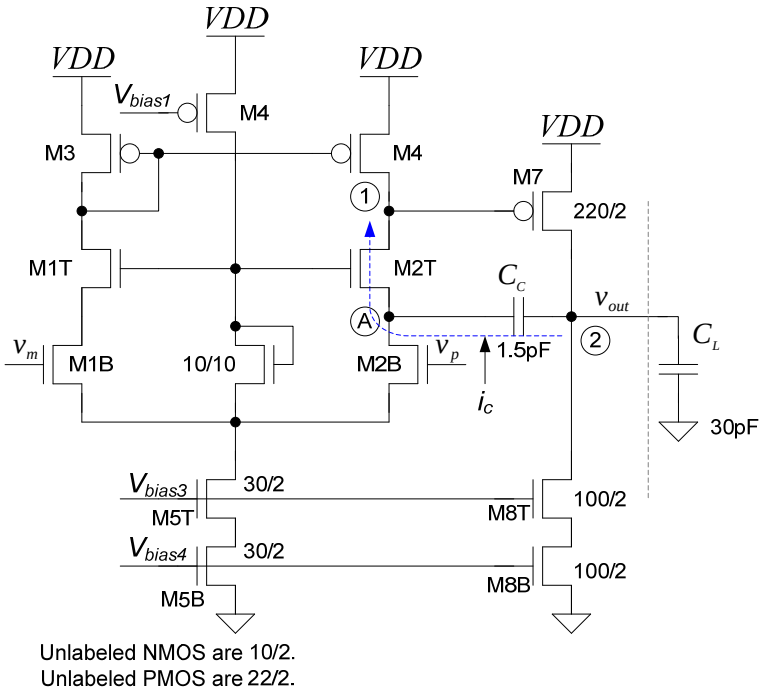
An indirect-compensated op-amp using a common-gate stage.

- The RHP zero can be eliminated by blocking the feed-forward compensation current component by using
  - ✓ A common gate stage,
  - ✓ A voltage buffer,
  - ✓ Common gate "embedded" in the cascode diff-amp, or
  - ✓ A current mirror buffer.
- Now, the compensation current is fed-back from the output to node-1 indirectly through a low-Z node-A.
- Since node-1 is not loaded by C_C, this results in higher unity-gain frequency (f_{un}).

Indirect Compensation in a Cascoded Op-amp



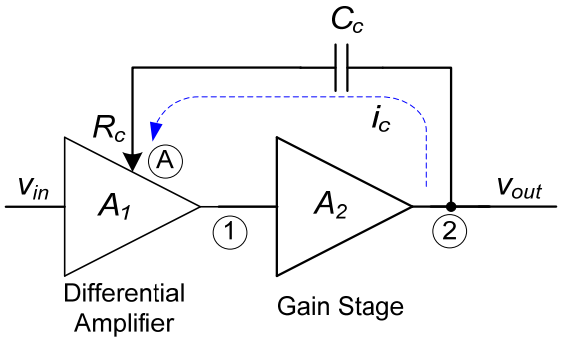
Indirect-compensation using cascoded current mirror load.



Indirect-compensation using cascoded diff-pair.

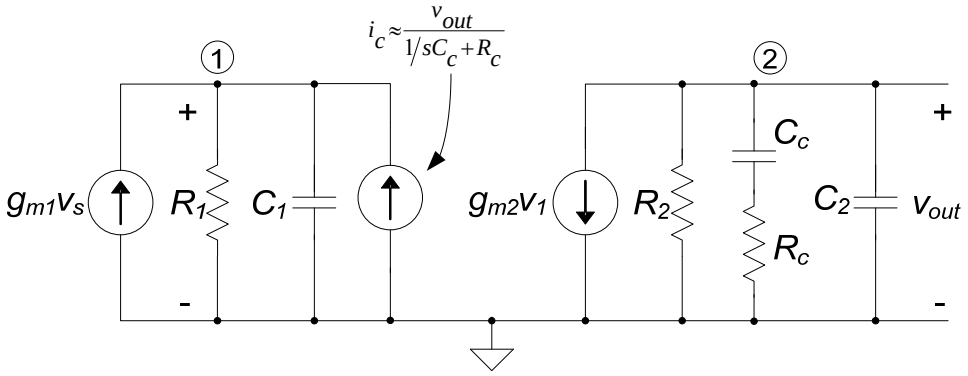
- Employing the common gate device "embedded" in the cascode structure for indirect compensation avoids a separate buffer stage.
  - ✓ Lower power consumption.
  - ✓ Also voltage buffer reduces the swing which is avoided here.

Analytical Modeling of Indirect Compensation



Block Diagram

The compensation current (i_C) is indirectly fed-back to node-1.

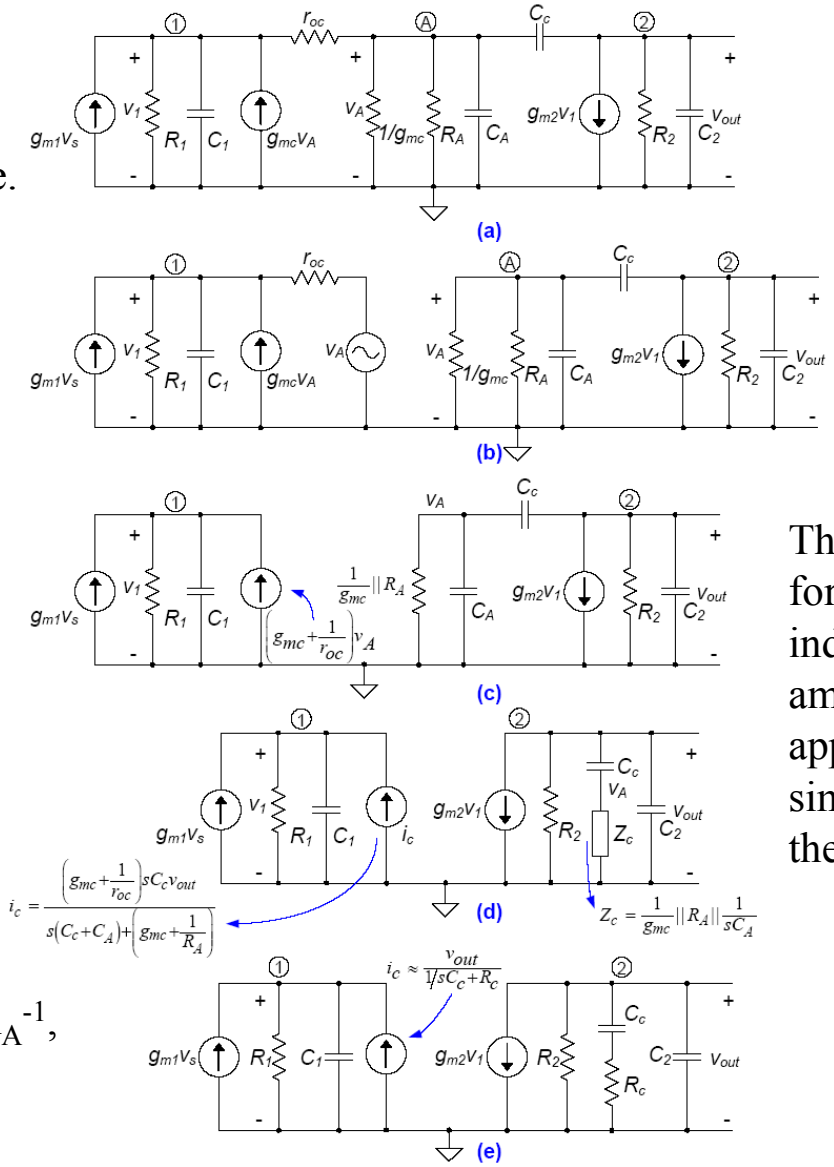


Small signal analytical model

R_C is the resistance attached to node-A.

Derivation of the Small-Signal Model

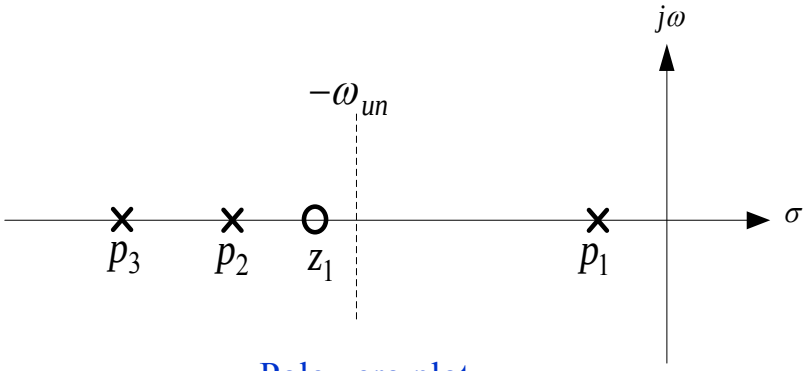
Resistance r_{oc} is assumed to be large.



The small-signal model for a common gate indirect compensated op-amp topology is approximated to the simplified model seen in the last slide.

$g_{mc} >> r_{oc}^{-1}$, R_A^{-1}, $C_C >> C_A$

Analytical Results for Indirect Compensation



Pole-zero plot

- Pole p_2 is much farther away from f_{un}.
  - ✓ Can use smaller g_{m2}=>less power!
- LHP zero improves phase margin.
- Much faster op-amp with lower power and smaller C_C.
- Better slew rate as C_C is smaller.

$$\frac{v_{out}}{v_s} = -A_v\left(\frac{1+b_1 s}{1+a_1 s+a_2 s^2+a_3 s^3}\right)$$

$$z_1 \approx -\frac{1}{R_c C_c}$$ LHP zero

$$p_1 \approx -\frac{1}{a_1} = -\frac{1}{g_{m2}R_2R_1C_c}$$

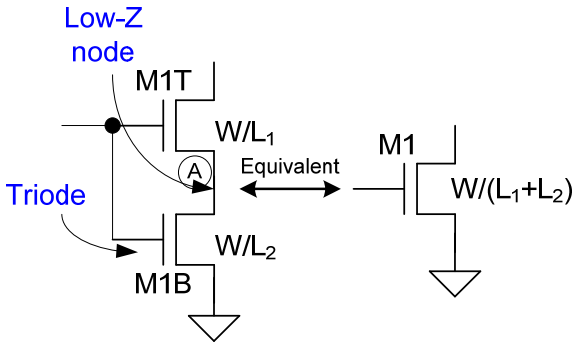
$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2}R_1C_c}{C_2(R_cC_c+R_1C_1)} \approx -\frac{g_{m2}C_c}{C_LC_1}$$

$$p_3 \approx -\frac{a_2}{a_3} = -\left[\frac{1}{R_cC_c}+\frac{1}{R_1C_1}\right]$$

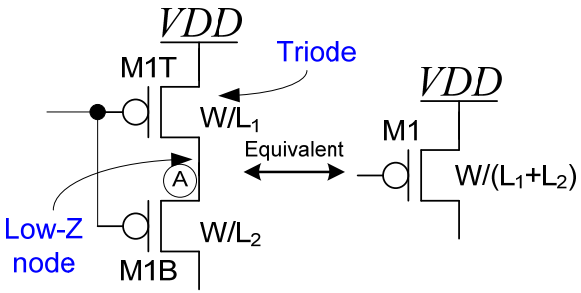
$$f_{un} = \frac{|p_1|A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_c}$$

Indirect Compensation Using Split-Length Devices

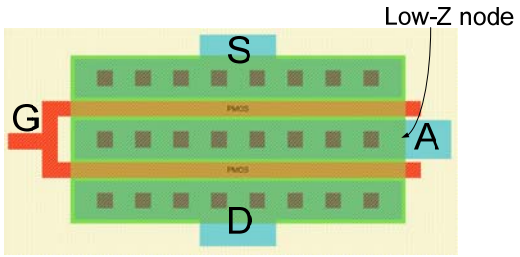
- As VDD scales down, cascoding is becoming tough. Then how to realize indirect compensation as we have no low-Z node available?
- Solution: Employ split-length devices to create a low-Z node.
  - ✓ Creates a pseudo-cascode stack but its really a single device.
- In the NMOS case, the lower device is always in triode hence node-A is a low-Z node. Similarly for the PMOS, node-A is low-Z.



NMOS

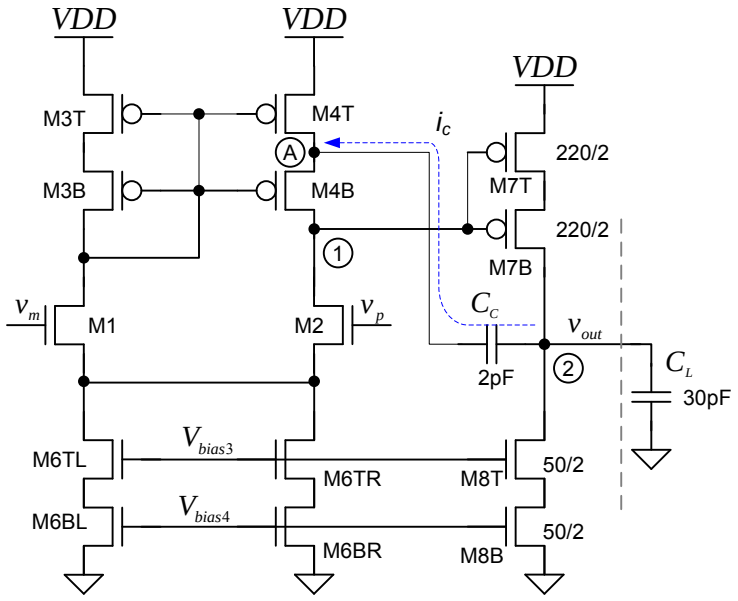


PMOS



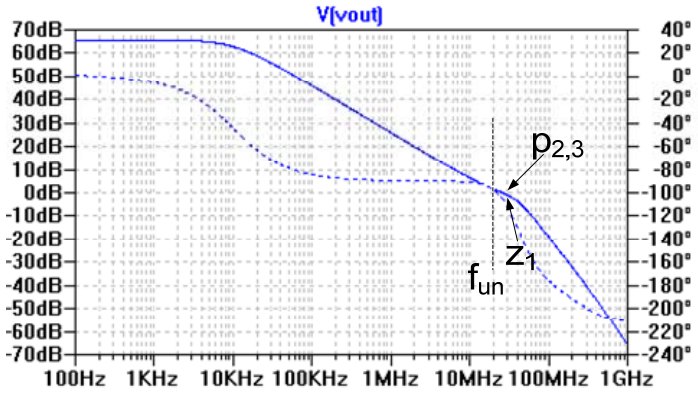
Split-length 44/4(=22/2)
PMOS layout

Split-Length Current Mirror Load (SLCL) Op-amp

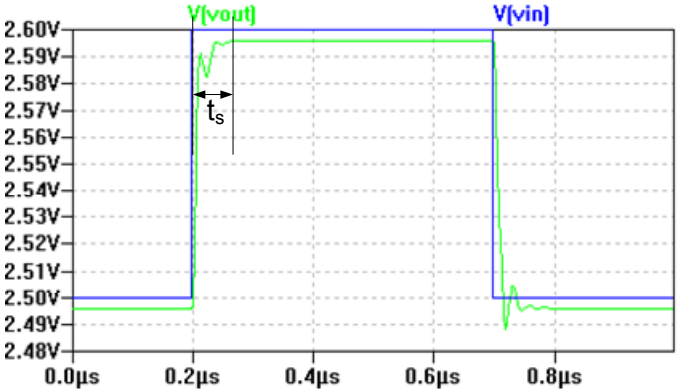


Unlabeled NMOS are 10/2.
Unlabeled PMOS are 22/2.

- The current mirror load devices are split-length to create low-Z node-A.
- Here, f_{un}=20MHz, PM=75° and t_s=60ns.

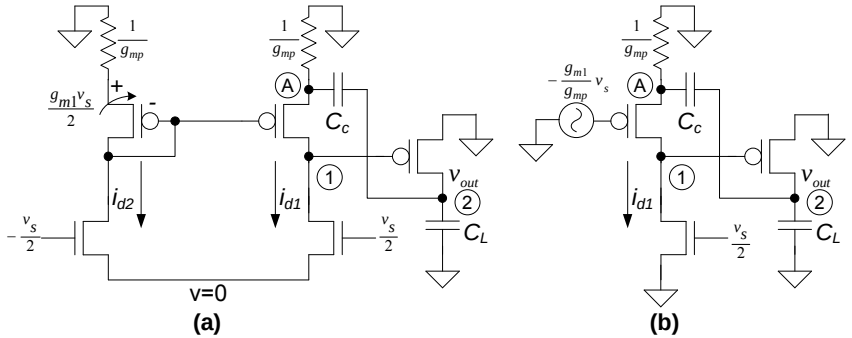


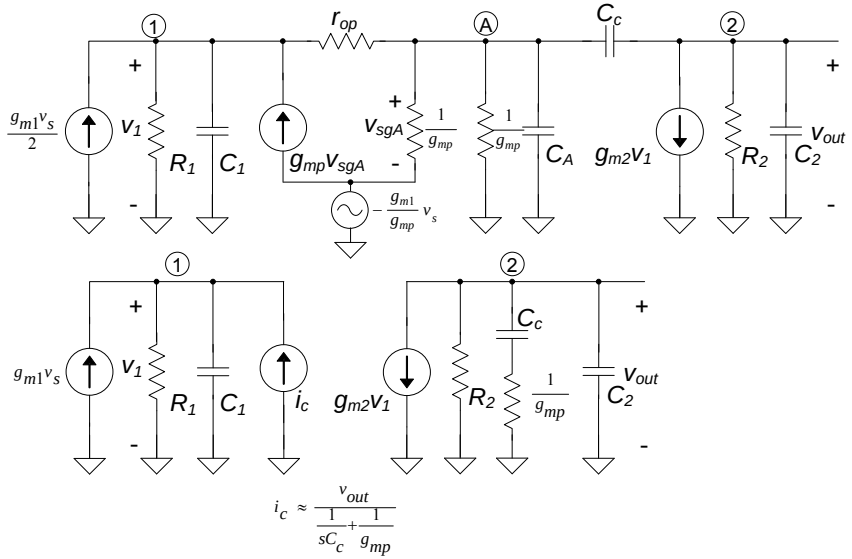
Frequency Response



Small step-input settling in follower configuration

SLCL Op-amp Analysis





$$i_c \approx \frac{v_{out}}{\frac{1}{sC_c}+\frac{1}{g_{mp}}}$$

$$f_{un} = \frac{g_{m1}}{2\pi(2C_c)}$$

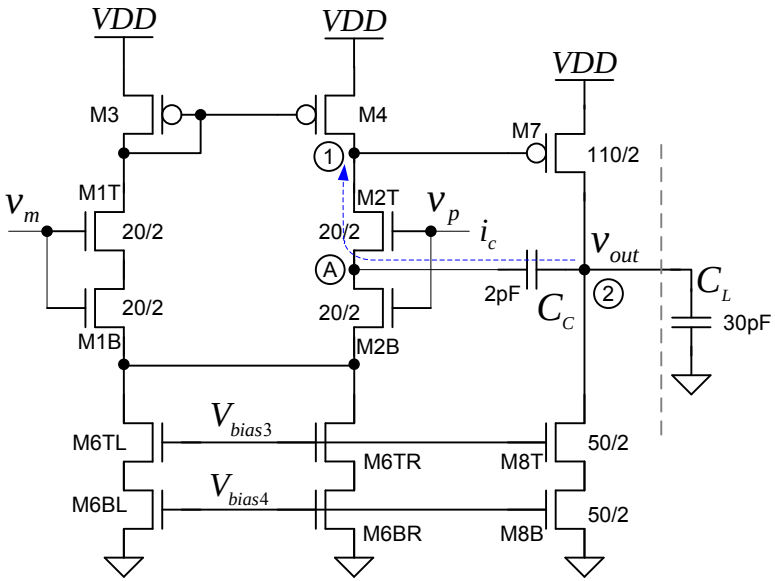
$$p_1 \approx -\frac{1}{2g_{m2}R_2R_1C_c}$$

$$\left|Re(p_{2,3})\right| = \frac{g_{m2}}{C_L}\sqrt{\frac{g_{mp}C_L}{g_{m2}C_1}}$$

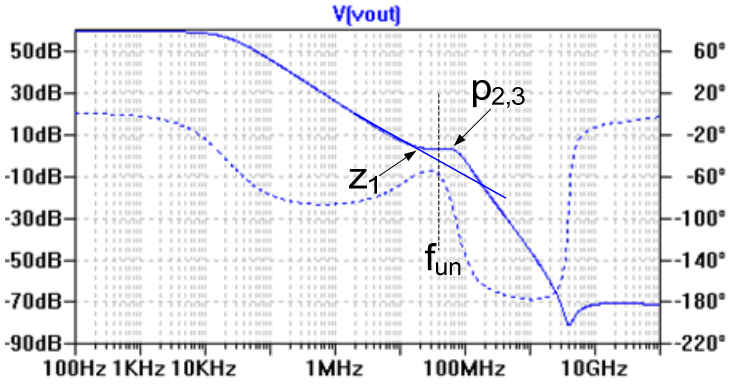
$$z_1 \approx -\frac{4g_{mp}}{3(C_c+C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_c+C_A)} \approx \frac{8\sqrt{2}}{3}\omega_{un}$$

- Here $f_{z1}=3.77f_{un}$
  - ✓ LHP zero appears at a higher frequency than f_{un}.

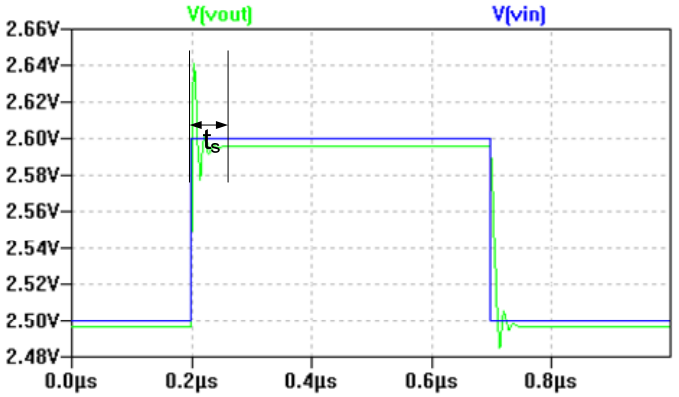
Split-Length Diff-Pair (SLDP) Op-amp



Unlabeled NMOS are 10/2.
Unlabeled PMOS are 22/2.



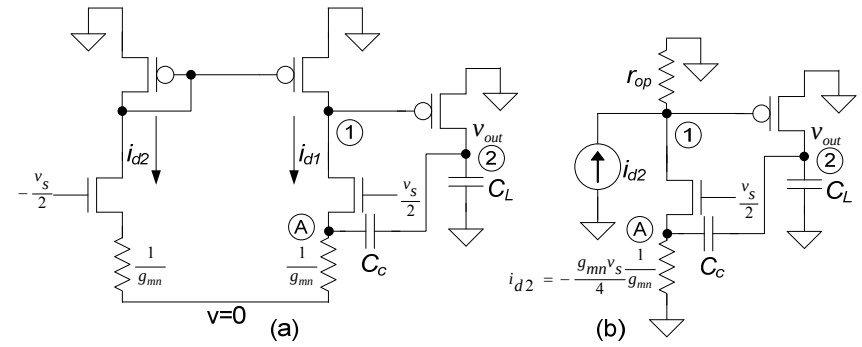
Frequency Response

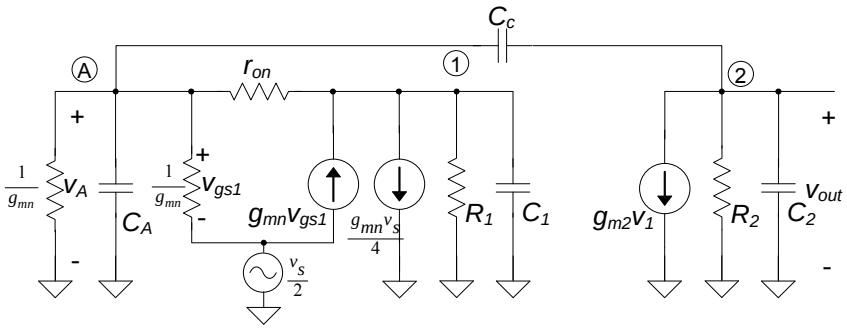


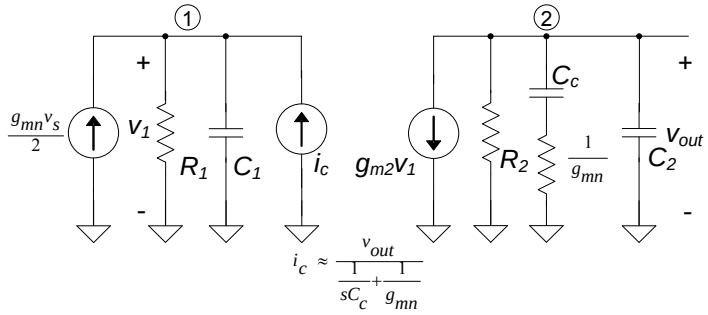
Small step-input settling in follower configuration

- The diff-pair devices are split-length to create low-Z node-A.
- Here, f_{un}=35MHz, PM=62°, t_s=75ns.
- Better PSRR due to isolation of node-A from the supply rails.

SLDP Op-amp Analysis







$$f_{un} = \frac{2g_{m1}}{2\pi C_c}$$

$$p_1 \approx -\frac{2}{g_{m2}R_2R_1C_c}$$

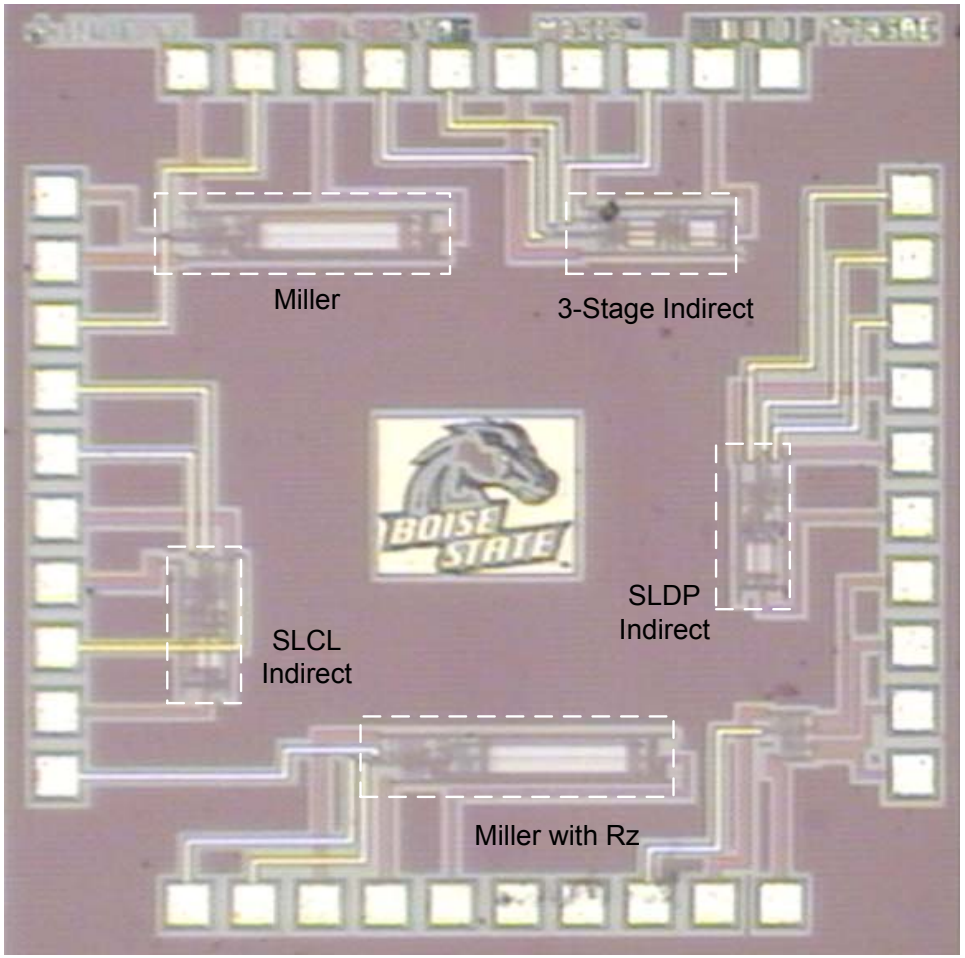
$$\left|Re(p_{2,3})\right| = \frac{g_{m2}}{C_L}\sqrt{\frac{g_{mp}C_L}{g_{m2}C_1}}$$

$$z_1 \approx -\frac{4g_{mn}}{3(C_c+C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_c+C_A)} \approx \frac{2\sqrt{2}}{3}\omega_{un}$$

- Here $f_{z1}=0.94f_{un}$,
  - ✓ LHP zero appears slightly before f_{un} and flattens the magnitude response.
  - ✓ This may degrade the phase margin.
- Not as good as SLCL, but is of great utility in multi-stage op-amp design due to higher PSRR.

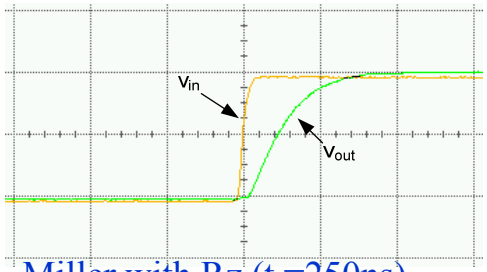
Saxena

Test Chip 1: Two-stage Op-amps

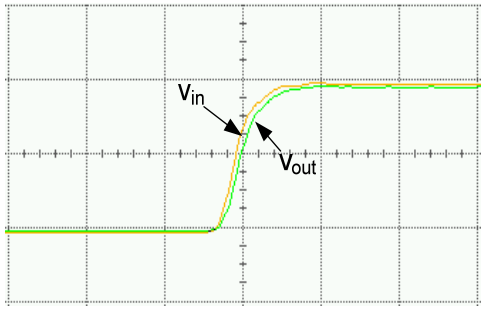


- AMI C5N 0.5µm CMOS, 1.5mmX1.5mm die size.

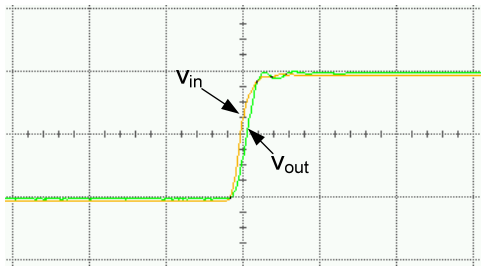
Test Results and Performance Comparison



Miller with Rz (t_s=250ns)



SLCL Indirect (t_s=60ns)



SLDP Indirect (t_s=75ns)

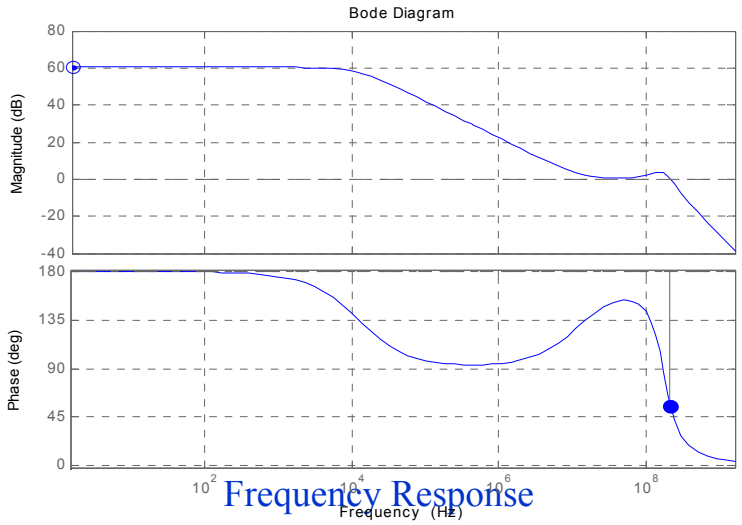
Performance comparison of the op-amps for C_L=30pF.

Op-amp Topology	A_{DC} (dB)	f_{un} (MHz)	C_C (pF)	PM	t_s (ns)	Power (mW)	Layout area (mm^2)
Miller	57	2.5	10	74°	270	1.2	0.031
Miller with R_Z	57	2.7	10	85°	250	1.2	0.034
SLCL (this work)	66	20	2	75°	60	0.7	0.015
SLDP (this work)	60	35	2	62°	75	0.7	0.015

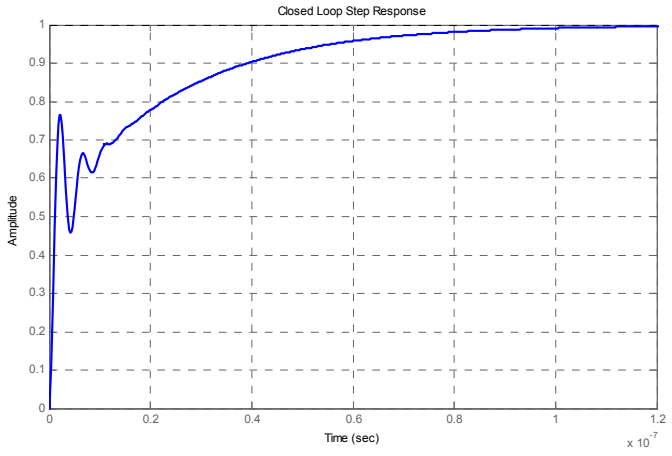
- 10X gain bandwidth (f_{un}).
- 4X faster settling time.
- 55% smaller layout area.
- 40% less power consumption.

Effect of LHP-zero on Settling

- In certain cases with indirect compensation, the LHP-zero ($\omega_{z,LHP}$) shows up near f_{un}.
  - ✓ Causes gain flattening and degrades PM
  - ✓ Hard to push out due to topology restrictions
- Ringing in closed-loop step response
  - ✓ This ringing is uncharacteristic of the 2nd order system.
  - ✓ Used to be a benign undershoot with the RHP zero, here it can be pesky
  - ✓ Is this settling behavior acceptable?
- Watch out for the $\omega_{z,LHP}$ for clean settling behavior!



Frequency Response



Small step-input settling in follower configuration

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