Short-Channel Analog Design

Additional Slides

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- Layout designers:
  - mostly care about W/L, layout matching and circuit isolation (substrate noise)

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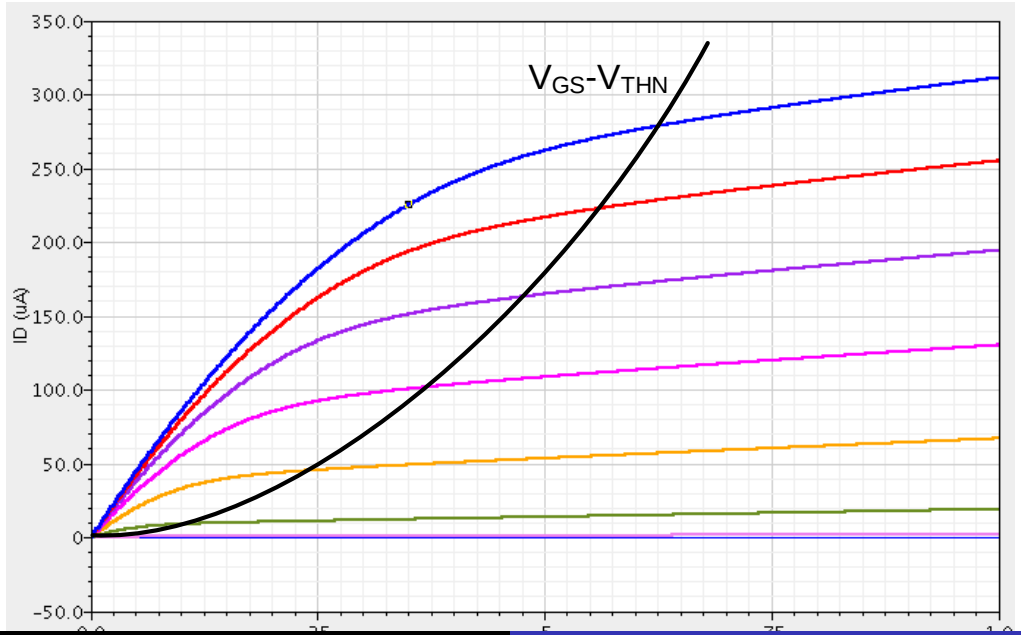
  - $V_{DD} = 1V.\ L_{min} = 50n$
  - $V_{THN} = V_{THP} = 280\,mV$

Short Channel Device Characteristics contd.

- The devices appear to go into saturation earlier than predicted by $V_{DS,sat} = V_{GS} - V_{THN}$



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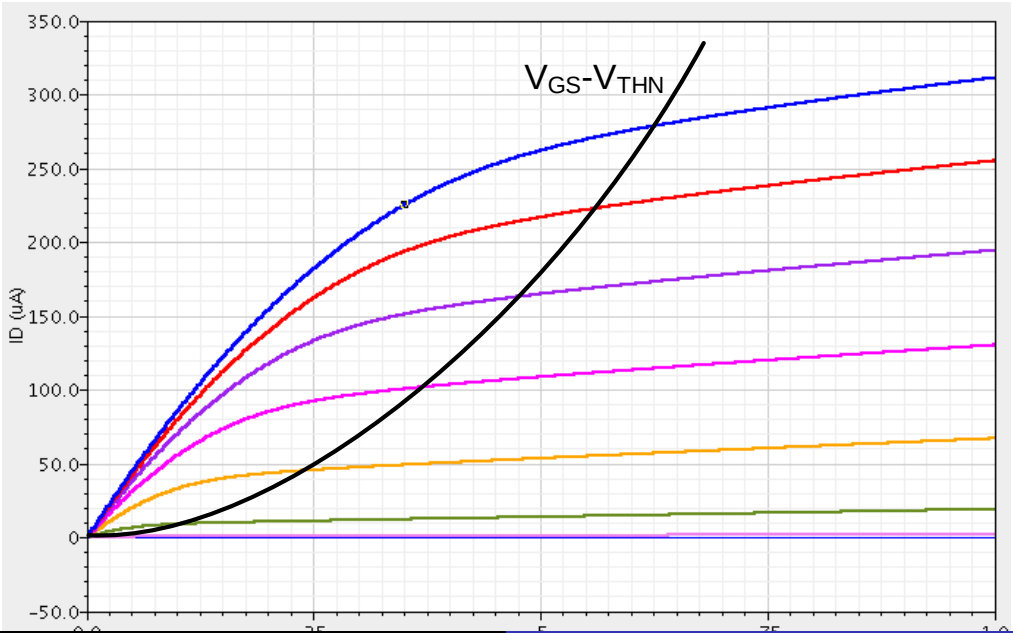

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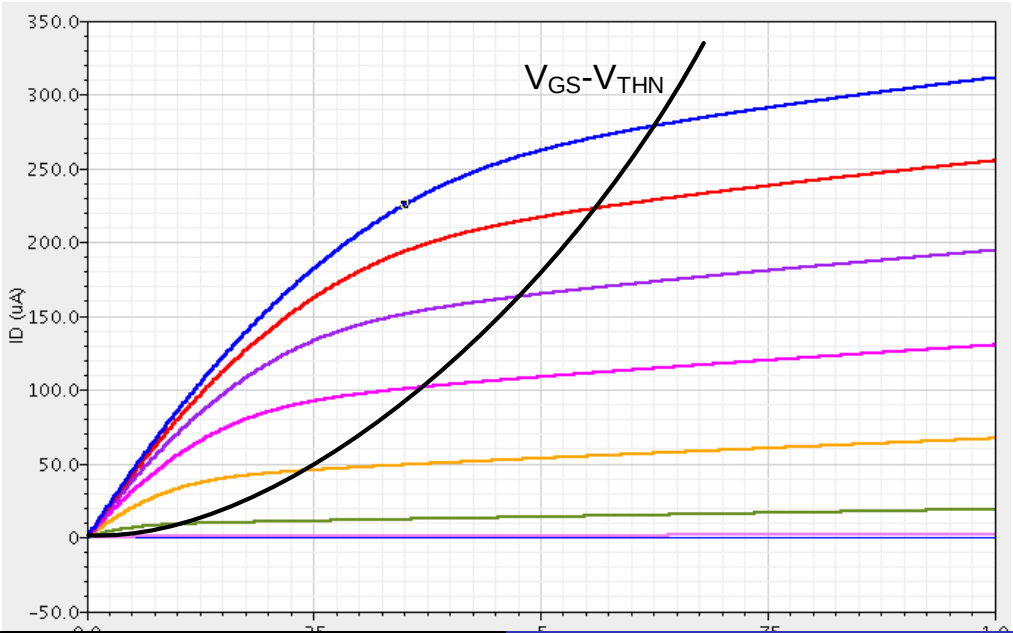

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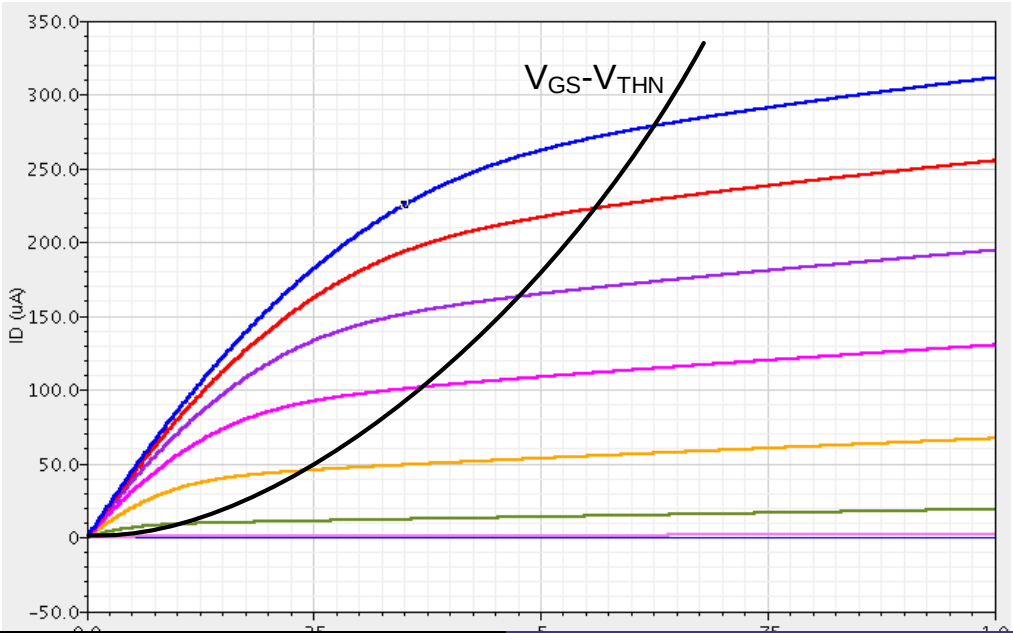
  - Is this good?
    - Not really, need to look at the region where r_o is large and that occurs when the device is well into saturation :(



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  - Increasing V_{ov} results in higher speed, but at a cost of reduced output swing

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- Just need to know the small signal parameters

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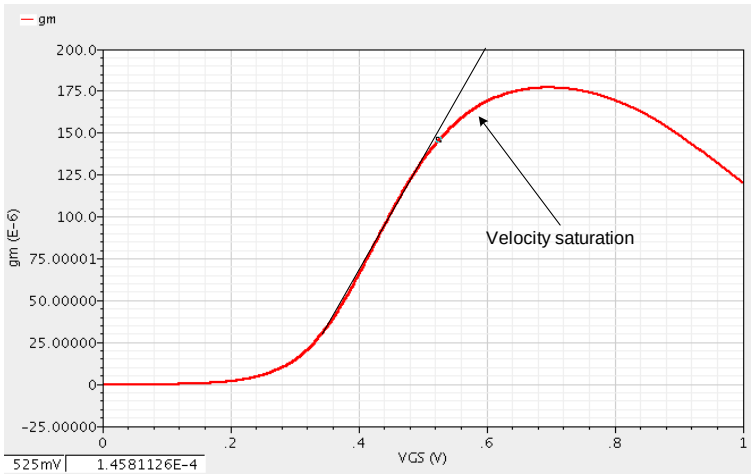
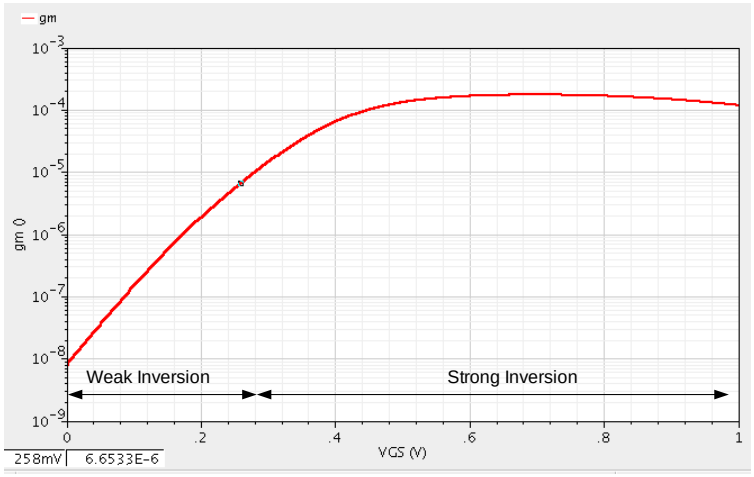
Transconductance





$$g_m = \beta\left(V_{GS} - V_{THN}\right)$$

$$g_{m_{sub-V_T}} = \frac{I_D}{nV_T}$$

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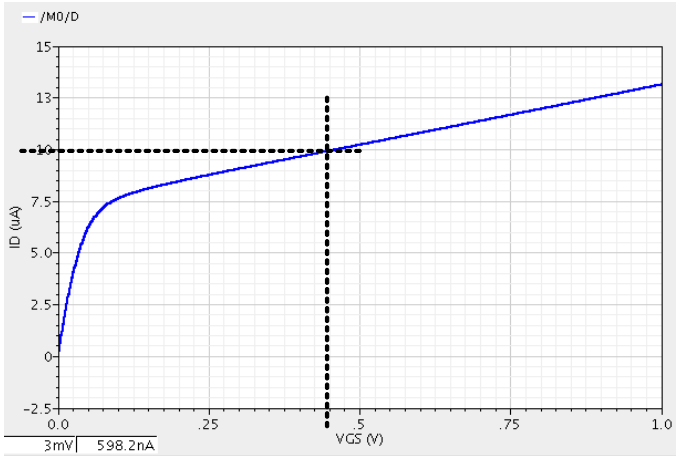

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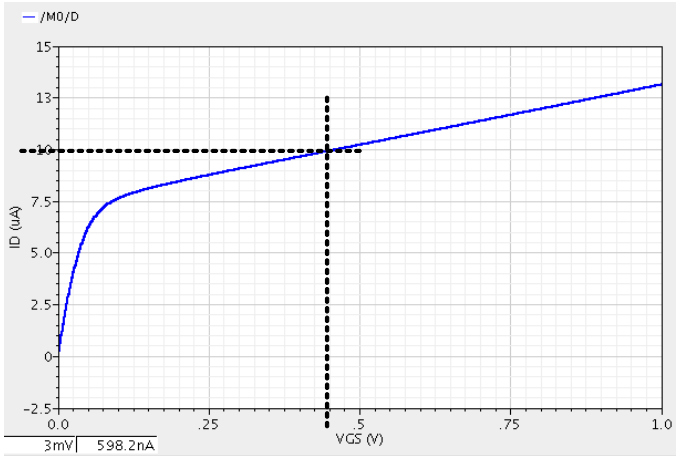

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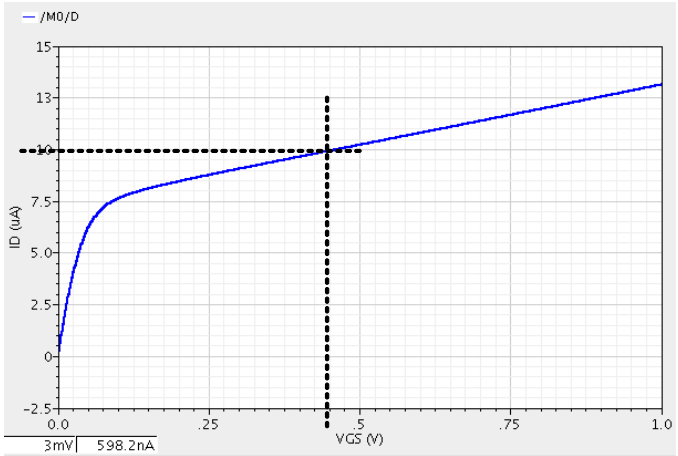

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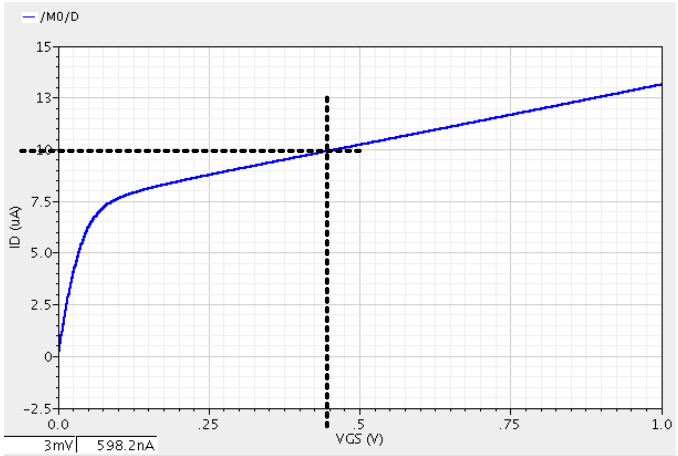

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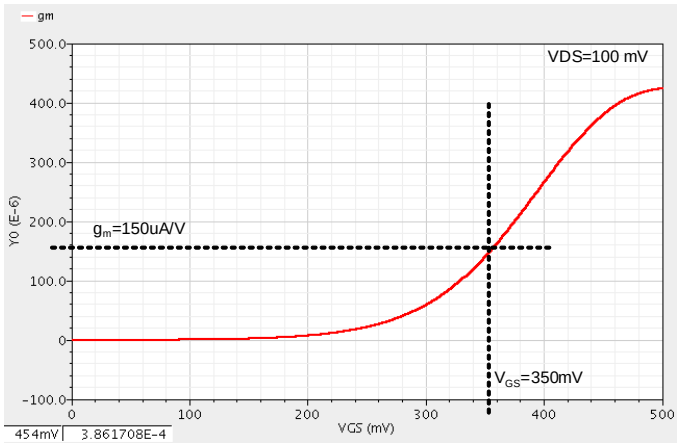

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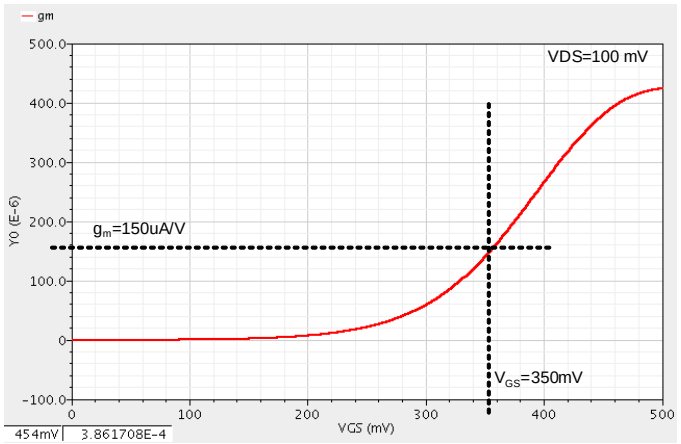

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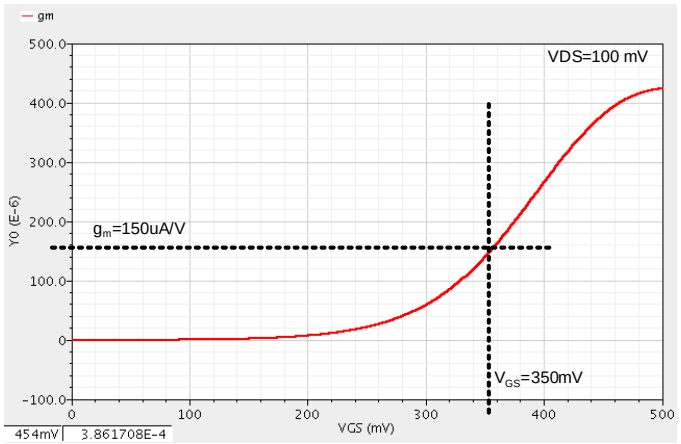

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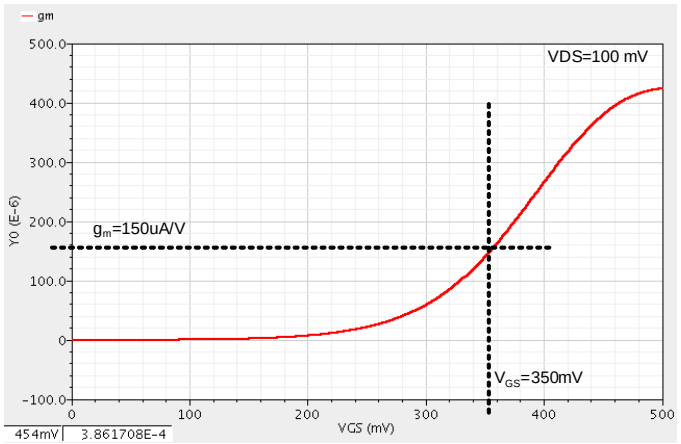

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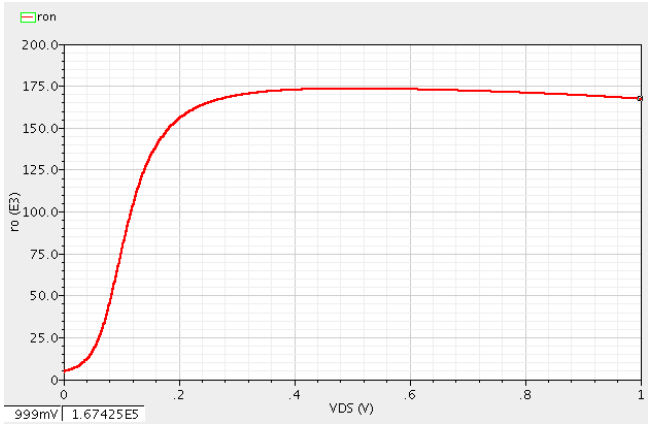

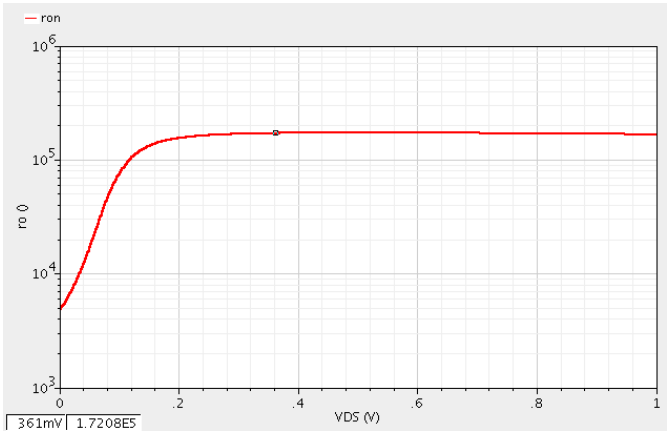

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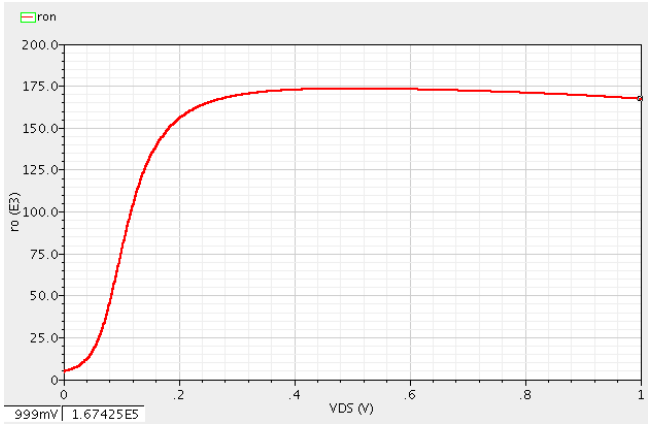

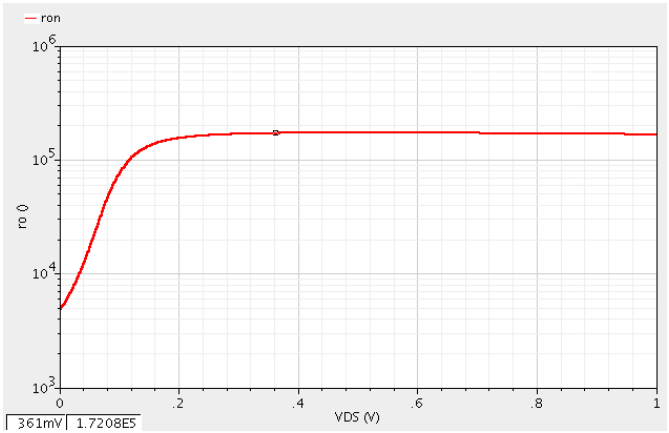

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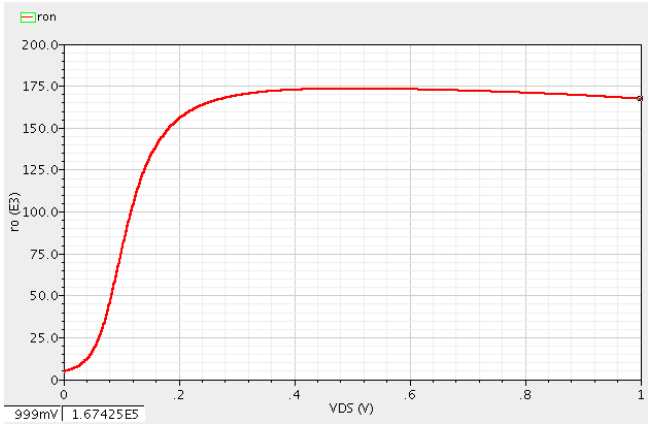

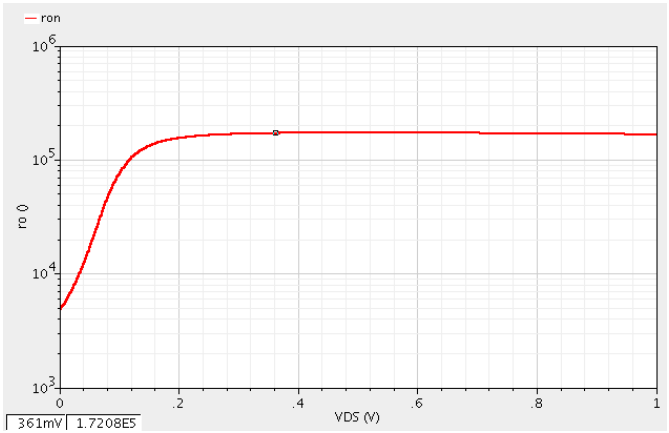

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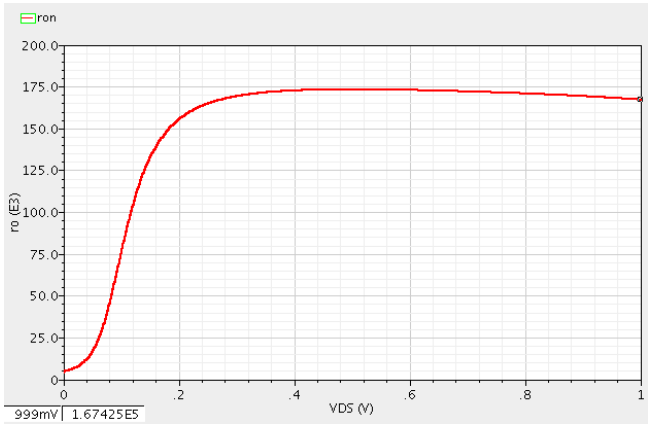
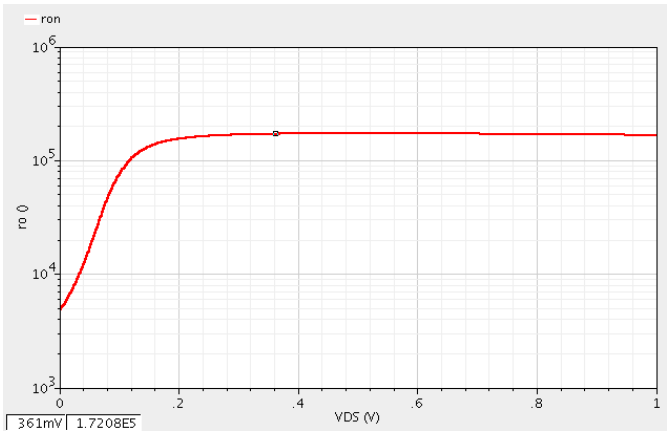
- Cannot just model by a simple equation $r_o = \frac{1}{\lambda I_{D,sat}}$

Open-loop Gain ($g_m r_o$)





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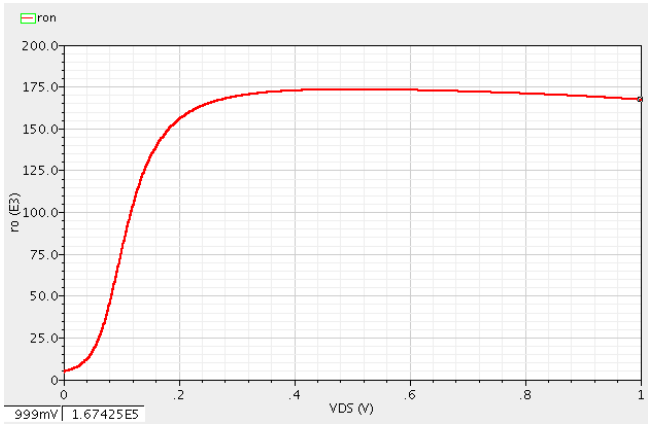
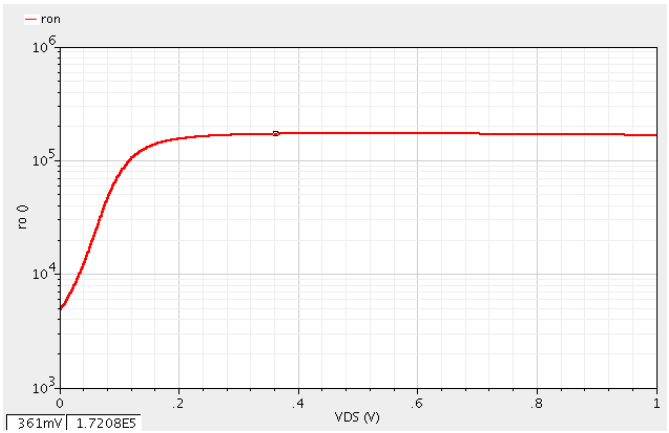
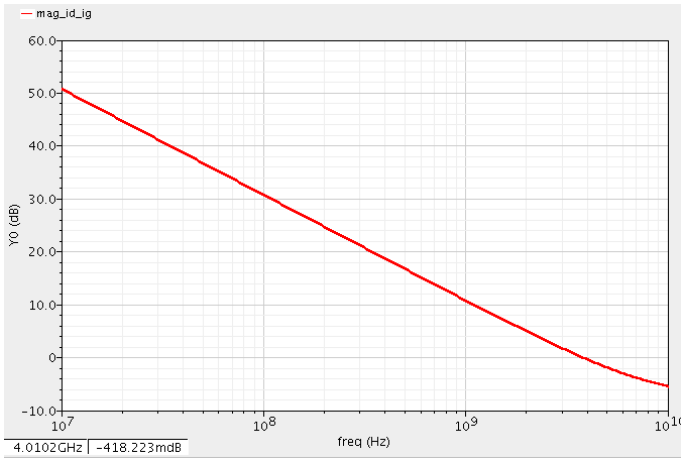




- The open loop gain is roughly $g_m r_o = 150\frac{\mu A}{V} \cdot 170k\Omega \approx 25$
  - considerably lower than the open-loop gain in a long channel process.

Transition Frequency



- f_T for a 50/2 NMOS is around 4GHz.
- Can look at the f_T when V_{GS} is swept.

Discussion

- The sizes an biasing selected in this example (from textbook) is a good starting point for a general design.
- If the sizes and biasing will eventually depend upon your design specifications.
- Also need to account for PVT shifts.
- Characterize the technology models well and generate a table for your selected design parameters.

Design Table

Table 9.2 Typical parameters for analog design using the *short-channel* CMOS process discussed in this book. These parameters are valid only for the device sizes and currents listed.

Short-channel MOSFET parameters for general analog design *VDD* = 1 V and a scale factor of **50 nm** (*scale* = 50e–9)			
Parameter	**NMOS**	**PMOS**	**Comments**
Bias current, I_D	10 µA	10 µA	Approximate, see Fig. 9.31
W/L	50/2	100/2	Selected based on I_D and V_{ov}
Actual W/L	2.5µm/100nm	5µm/100nm	L_{min} is 50 nm
$V_{DS,sat}$ and $V_{SD,sat}$ V_{ovn} and V_{ovp}	50 mV 70 mV	50 mV 70 mV	However, see Fig. 9.32 and the associated discussion
V_{GS} and V_{SG}	350 mV	350 mV	No body effect
V_{THN} and V_{THP}	280 mV	280 mV	Typical
$\partial V_{THN,P}/\partial T$	– 0.6 mV/C°	– 0.6 mV/C°	Change with temperature
v_{satn} and v_{satp}	110 x 10^3 m/s	90 x 10^3 m/s	From the BSIM4 model
t_{ox}	14 Å	14 Å	Tunnel gate current, 5 A/cm^2
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	25 fF/µm^2	25 fF/µm^2	$C_{ox} = C'_{ox}WL \cdot (scale)^2$
C_{oxn} and C_{oxp}	6.25 fF	12.5 fF	PMOS is two times wider
C_{gsn} and C_{sgp}	4.17 fF	8.34 fF	$C_{gs} = \frac{2}{3}C_{ox}$
C_{gdn} and C_{dgp}	1.56 fF	3.7 fF	$C_{gd} = CGDO \cdot W \cdot scale$
g_{mn} and g_{mp}	150 µA/V	150 µA/V	At I_D = 10 µA
r_{on} and r_{op}	167 kΩ	333 kΩ	Approximate at I_D = 10 µA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	25 V/V	50 V/V	!!Open circuit gain!!
λ_n and λ_p	0.6 V^{-1}	0.3 V^{-1}	$L = 2$
f_{Tn} and f_{Tp}	6000 MHz	3000 MHz	Approximate at $L = 2$

References I


R. J. Baker, CMOS Circuit Design, Layout and Simulation, revised 2nd Edition, Wiley-IEEE, 2008.