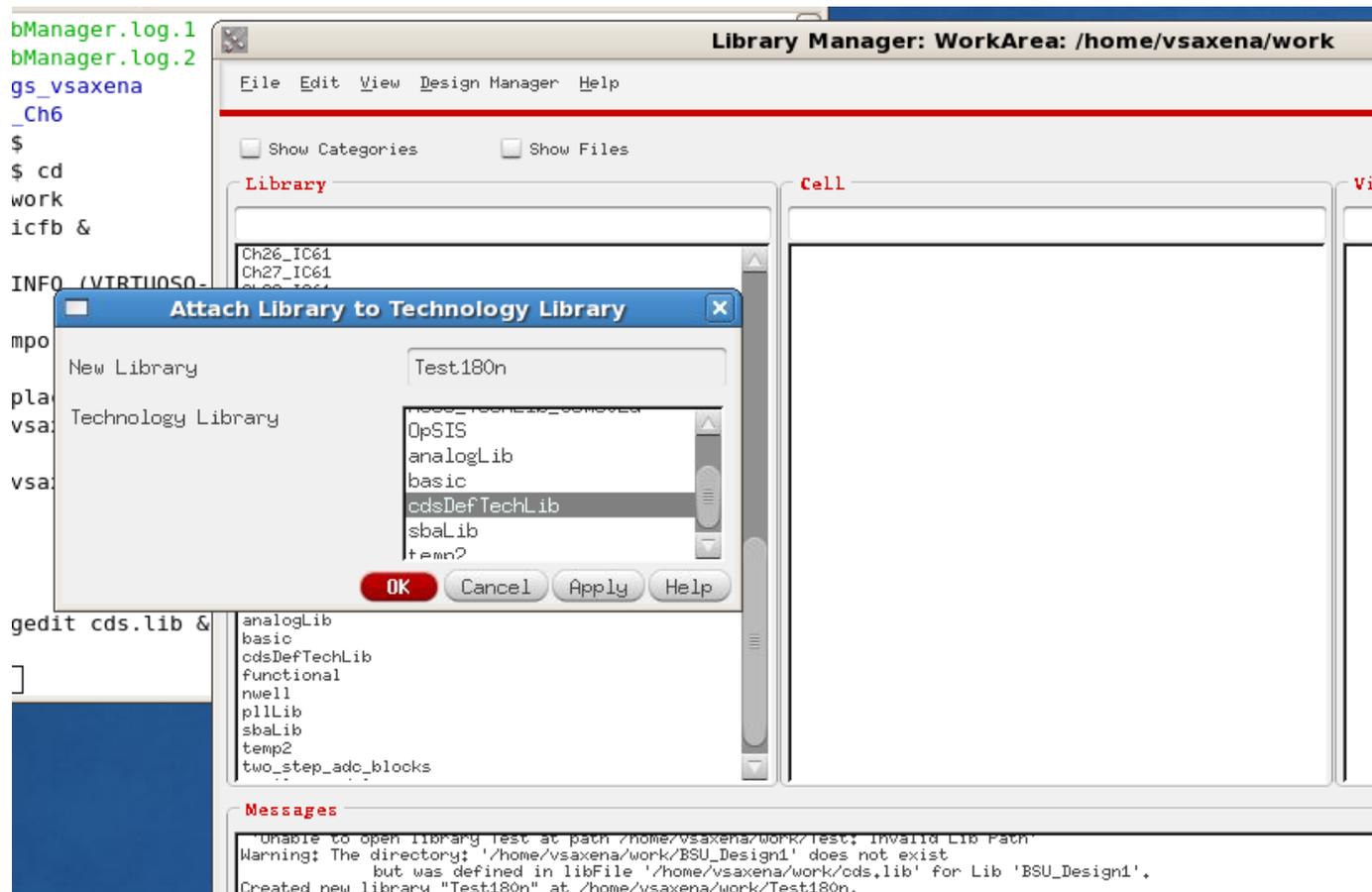
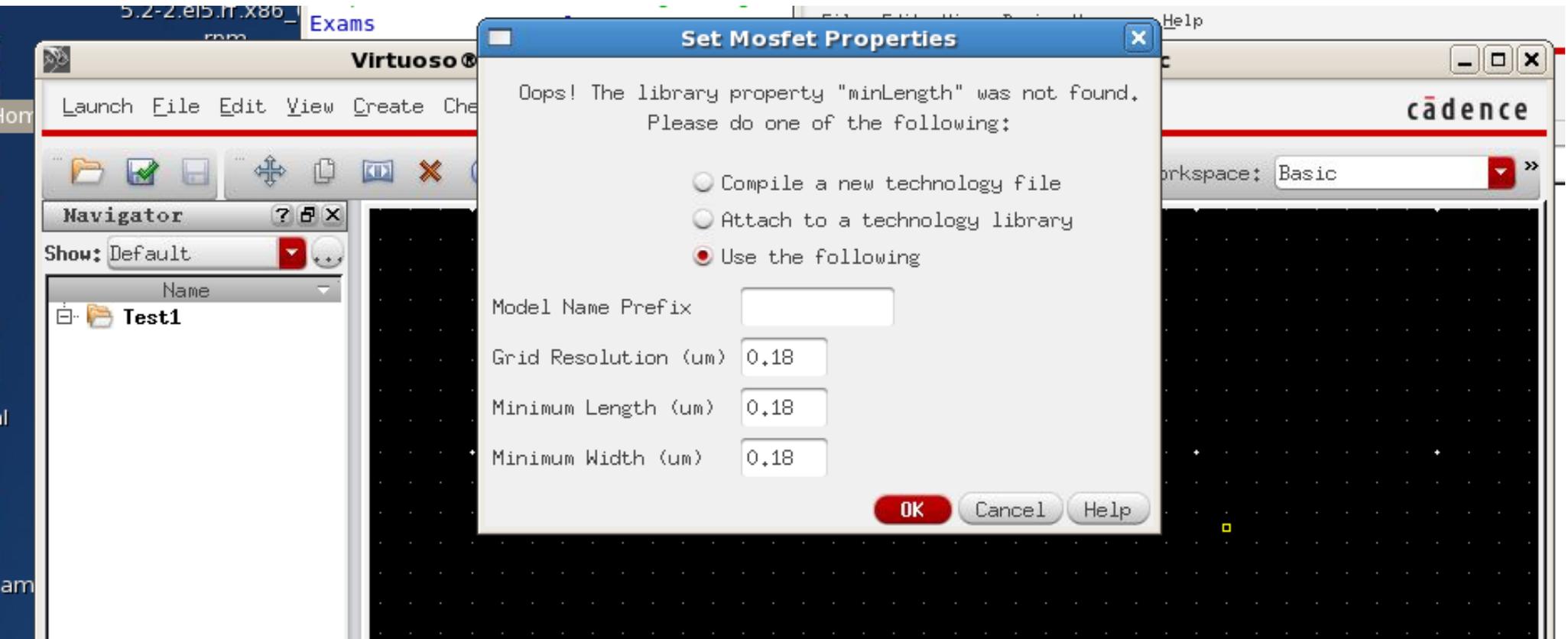


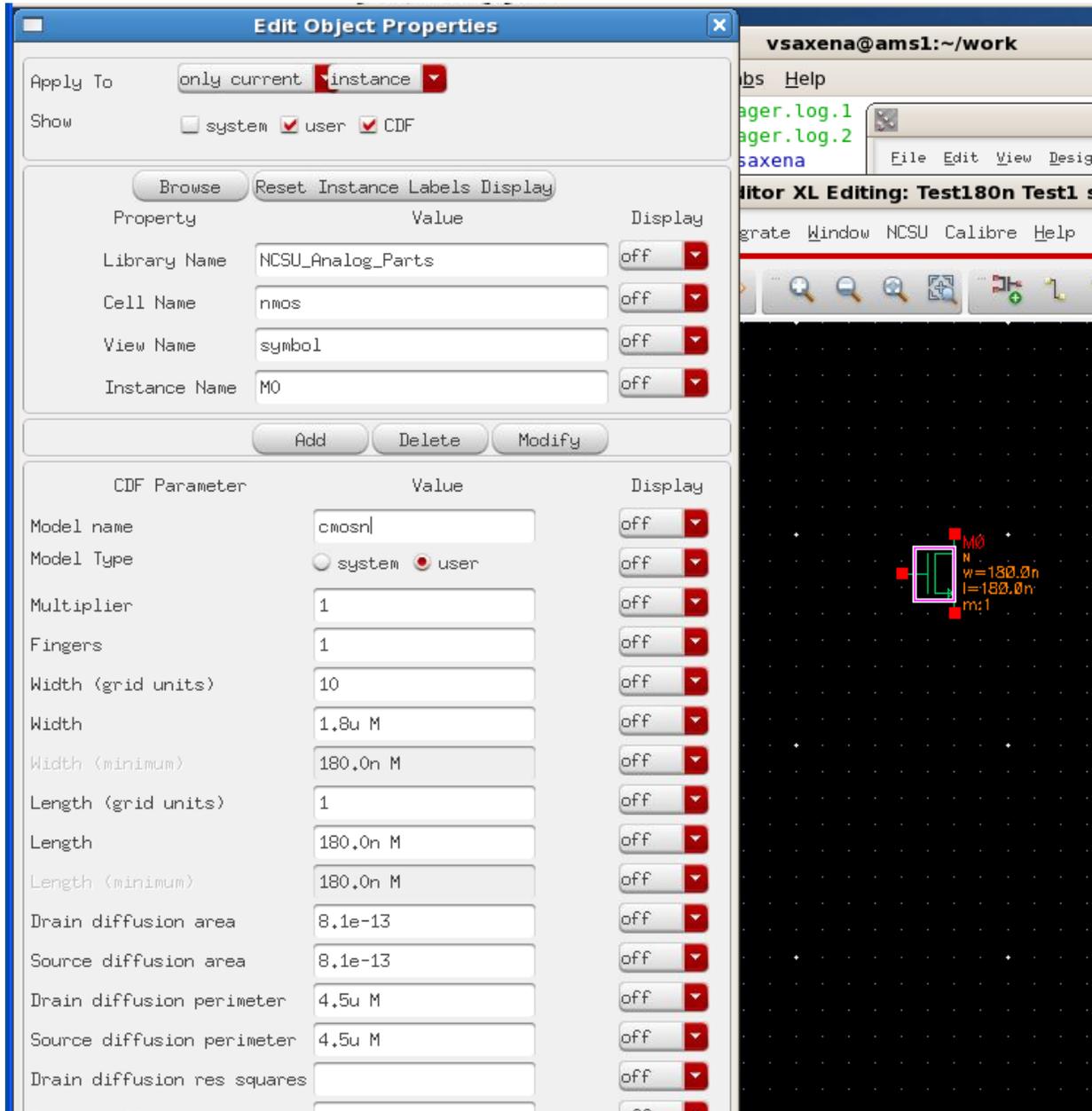
# 180n CMOS Simulation Setup



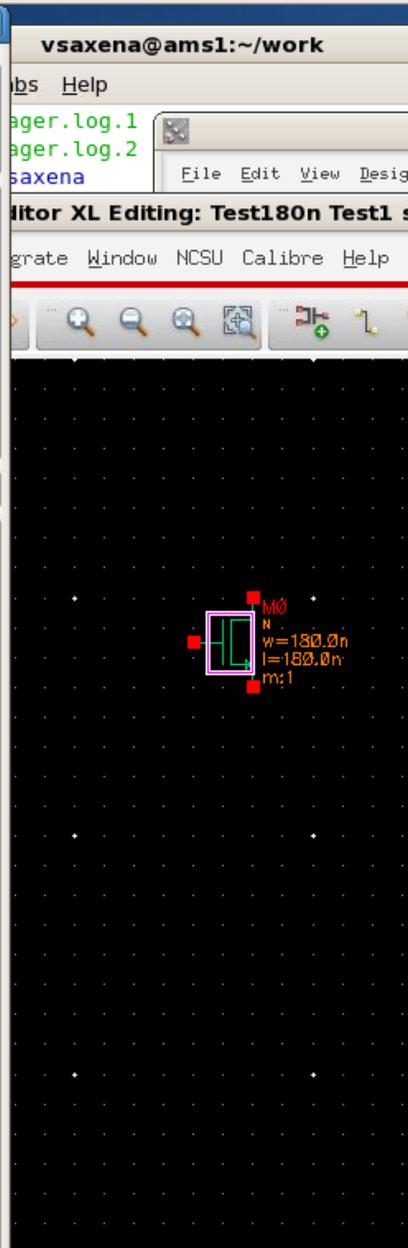
- Create a new library (Test180n here)
- Since we do not have a PDK for the 180n CMOS process, attach “cdsDeftechLib” as the techlib.

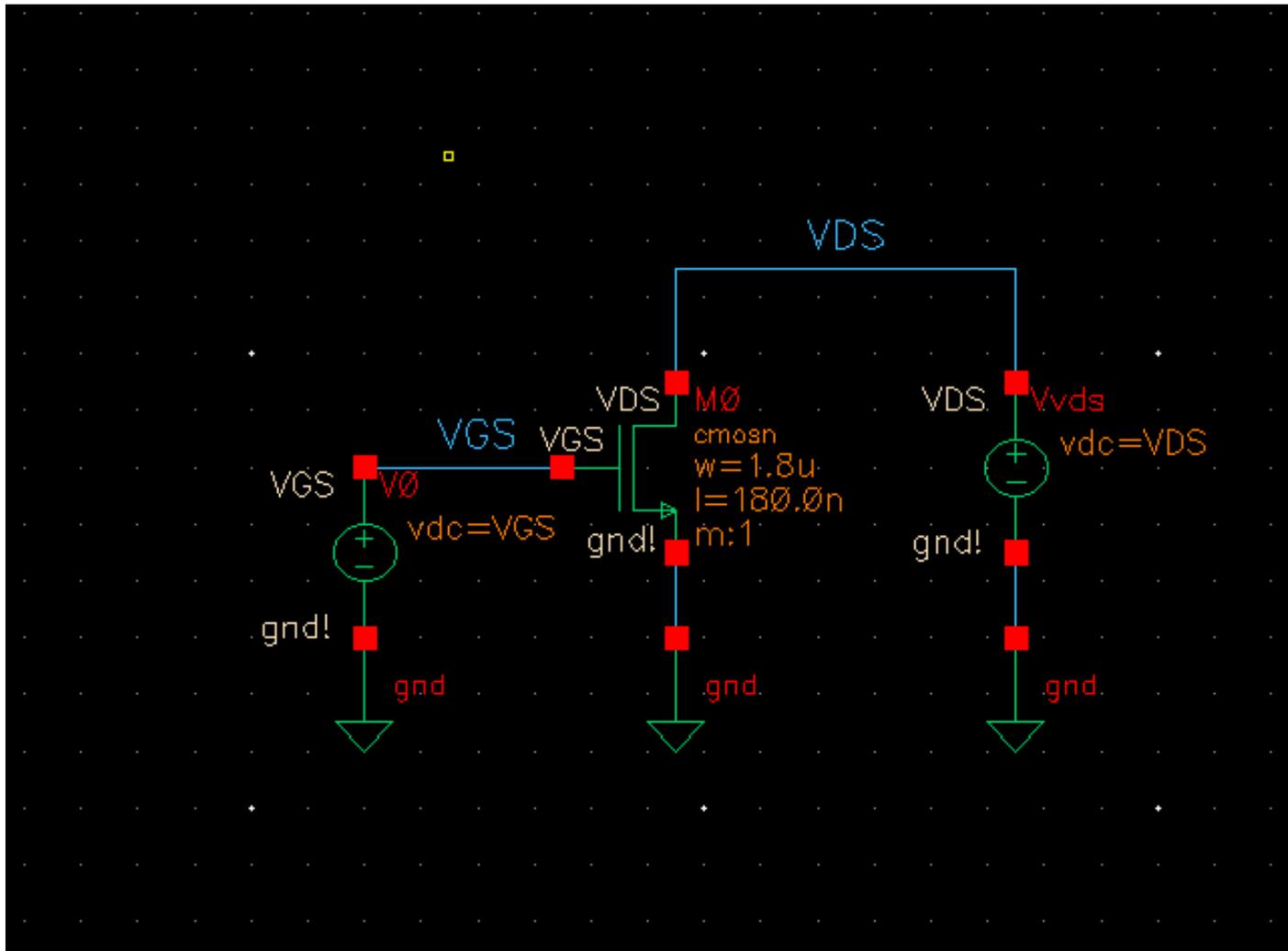


- Create a new schematic view
- You will be prompted to set the Mosfet minimum dimensions
- Enter 0.18 for all values (180n process)

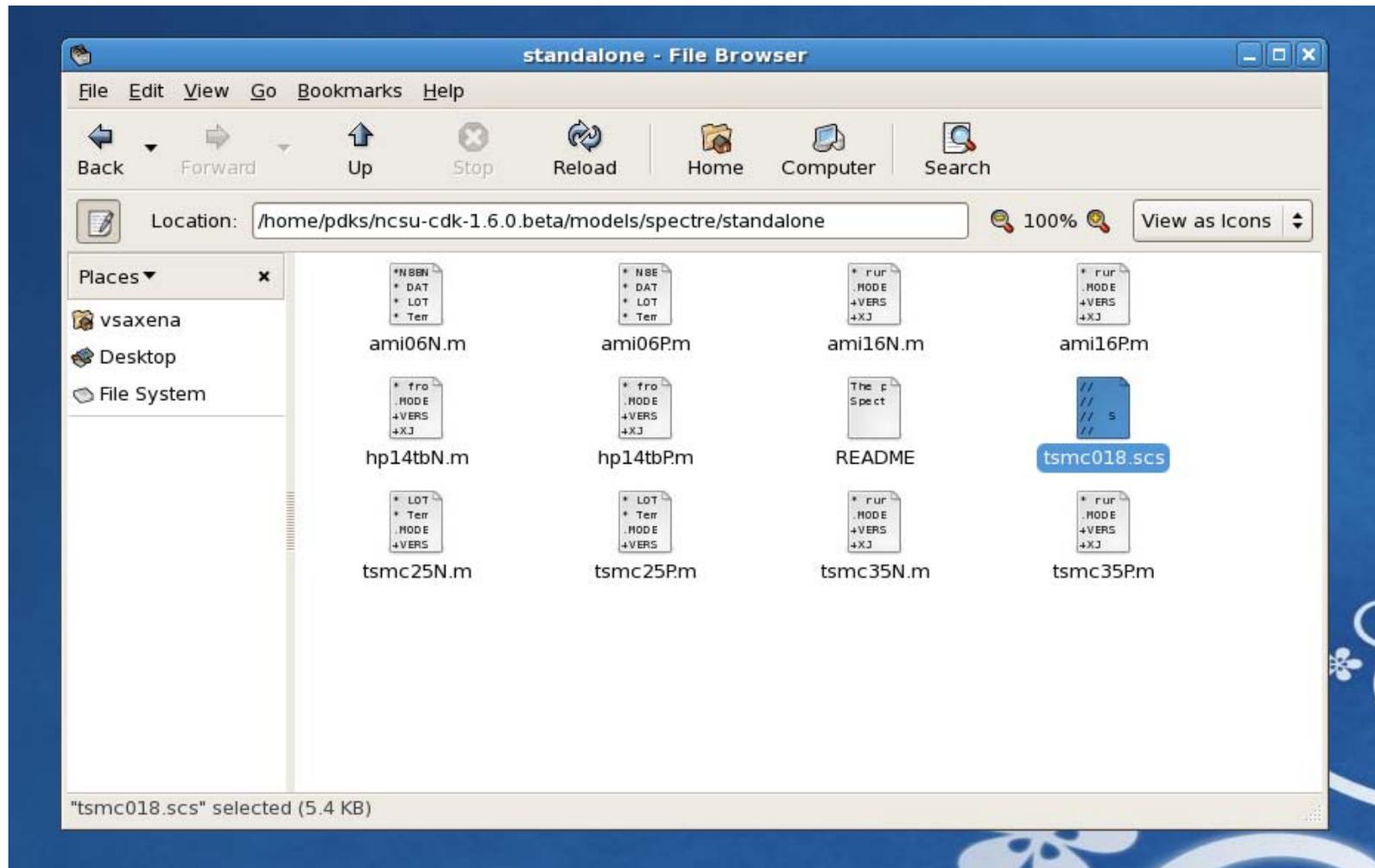


- Create NMOS instance with desired W and L.
- Make sure you set the model name to **cmosn** or **cmosp**
- Use setting of model type=user for changing this parameter

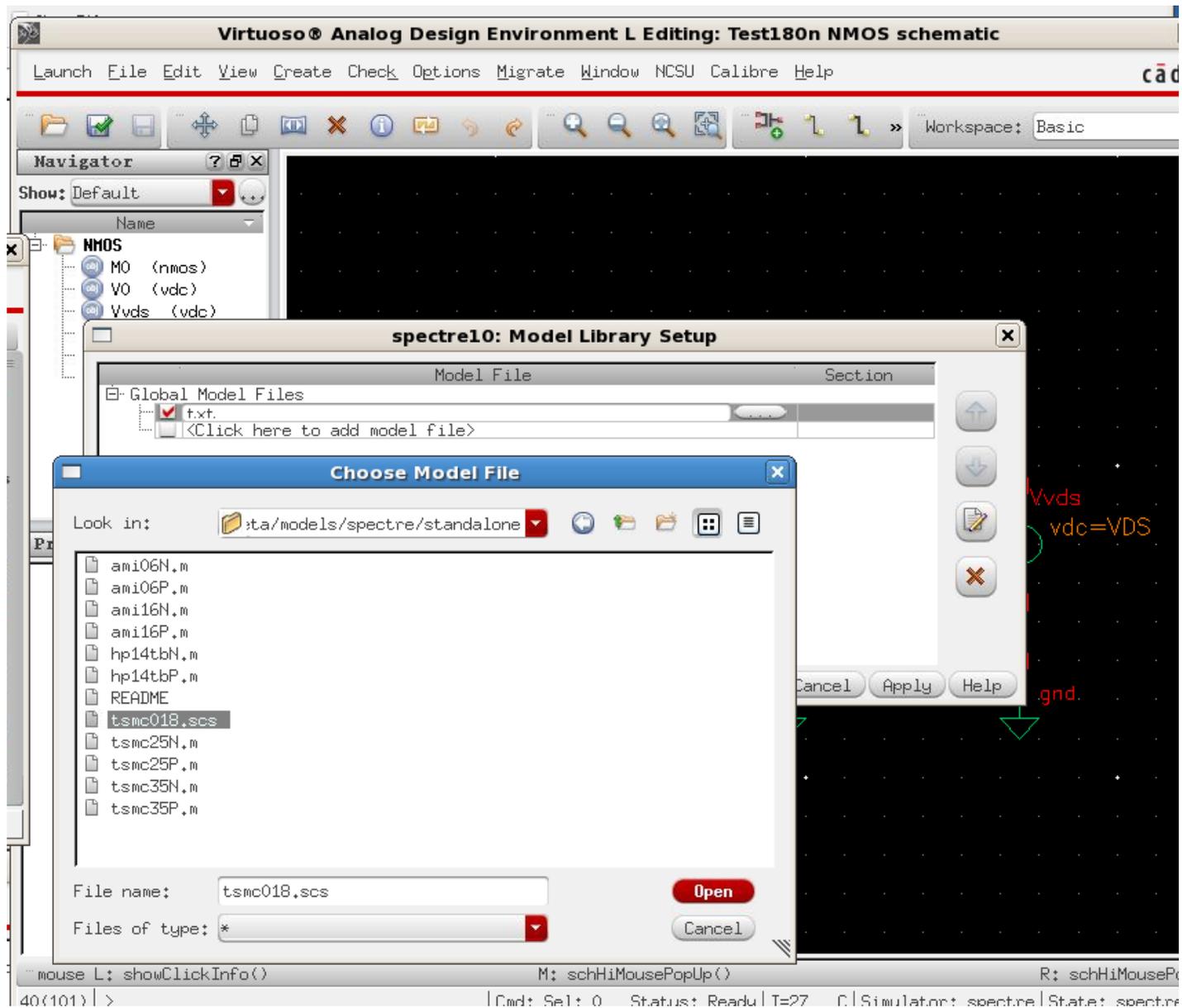




- Create your schematic



- Model location on AMS servers is at `/home/pdks/ncsu-cdk-1.6.0.beta/models/spectre/standalone`



- Set the model location (tsmc018.scs)

The image displays the Cadence Virtuoso Analog Design Environment interface. On the left, a terminal window shows the user navigating through directories and running simulation commands. The main window is titled 'Choosing Analyses -- Virtuoso® Analog Design E...', where the 'dc' analysis type is selected. Below this, the 'Sweep Variable' is set to 'Design Variable' with the name 'VGS'. The 'Sweep Range' is configured as a 'Start-Stop' sweep from 0 to 1.8, with a 'Step Size' of 100u. The schematic on the right shows an NMOS transistor with its gate connected to a VGS source and its drain to a VDS source. The transistor parameters are listed as  $w = 1.8\mu$  and  $l = 180.0n$ .

```

Exams          logs_vsaxena
Fig11_21.run1  My_Ch6
[vsaxena@ams1 ece510]$
[vsaxena@ams1 ece510]$ cd
[vsaxena@ams1 ~]$ cd work
[vsaxena@ams1 work]$ icfb &
[1] 30585
[vsaxena@ams1 work]$ INFO (VIRTUOSO-
b' has been replaced
with 'virtuoso'. A temporary link to
se.
Cadence recommends replacing all cas
*WARNING* file /home/vsaxena/CDS.log
s.
*WARNING* file /home/vsaxena/CDS.log
ess.

[vsaxena@ams1 work]$
[vsaxena@ams1 work]$
[vsaxena@ams1 work]$ gedit cds.lib &
[2] 3073
  
```

**Choosing Analyses -- Virtuoso® Analog Design E X**

Analysis  tran  dc  ac  noise

xf  sens  dcmatch  stb

pz  sp  envlp  pss

pac  pstb  pnoise  pxf

psp  qpss  qpac  qpnoise

qpxf  qpsp

DC Analysis

Save DC Operating Point

Hysteresis Sweep

Sweep Variable

Temperature

Design Variable Variable Name VGS

Component Parameter

Model Parameter

Sweep Range

Start-Stop Start 0 Stop 1.8

Center-Span

Sweep Type

Linear  Step Size 100u

Number of Steps

Add Specific Point

Enabled

**Environment L Editing: Test180n NMOS schematic**

Migrate Window NCSU Calibre Help

Workspace: Basic

Schematic Diagram: NMOS transistor with VGS and VDS sources. Parameters:  $w = 1.8\mu$ ,  $l = 180.0n$ .

- Set up your desired analysis (VGS DC sweep in this example)

Terminal window showing commands and output:

```
[vsaxena@ams1 ~]$ cd work
[vsaxena@ams1 work]$ icfb &
[1] 30585
[vsaxena@ams1 work]$ INFO (VIRTUOSO-
b' has been replaced
with 'virtuoso'. A temporary link to
se.
Cadence recommends replacing all cas
*WARNING* file /home/vsaxena/CDS.log
s.
*WARNING* file /home/vsaxena/CDS.log
ess.

[vsaxena@ams1 work]$
[vsaxena@ams1 work]$
[vsaxena@ams1 work]$ gedit cds.lib &
[2] 3073
```

Navigator window showing a hierarchical tree structure:

```
Test180n
├── Ch27_IC61
├── Ch28_IC61
├── Ch29_IC61
├── Ch30_IC61
├── FDOpamps
├── MagTapeout
├── MemRistor
├── NCSU_Analog_Parts
├── NCSU_Digital_Parts
├── NCSU_TechLib_ami06
├── NCSU_TechLib_tsmc02d
├── NwellRes
├── OpSIS
├── Opamp_test1
├── Process_Char
├── TIA_130n
├── Test180n
├── Tutorial_1
├── ahdlLib
├── analogLib
├── basic
├── cdsDefTechLib
└── Functional
```

DC Response plot showing current I (mA) versus VGS (V):

VGS (V)	I (mA)
0.0	0.000
0.25	0.000
0.5	0.000
0.75	0.100
1.0	0.300
1.25	0.600
1.5	0.900
1.75	1.000
2.0	1.000

Schematic diagram showing an NMOS transistor (M0) connected to a voltage source (VDS) and ground (gnd!). The transistor parameters are:  $w = 1.8\mu$ ,  $l = 180.0n$ , and  $m = 1$ . The voltage source is labeled VDS and the current is labeled Vvds = Vdc = VDS.

- Run simulation