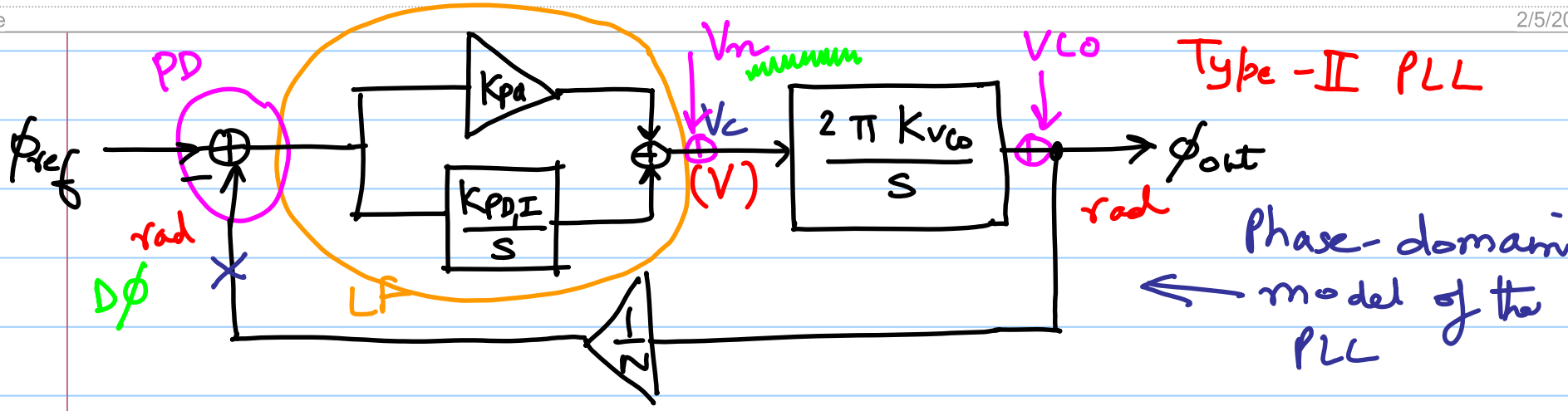
ECE 518- Lecture 7

Note Title 2/5/2015



$$L(s) = \left(K_{PD} + \frac{K_{PD,I}}{s}\right) \cdot \frac{2\pi K_{VCO}}{s} \cdot \frac{1}{N}$$

$$\omega_z = \frac{K_{PD,I}}{K_{PD}}$$

CP-PLL $\Rightarrow$

$$K_{PD,I} = \frac{I_0}{2\pi C}$$

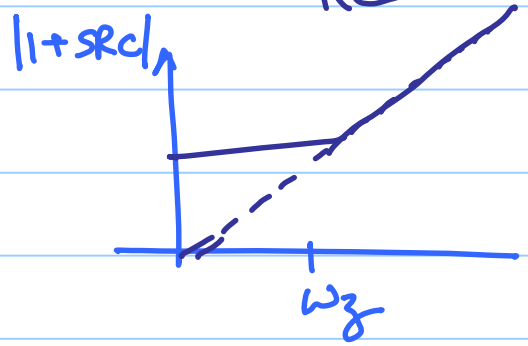
CP current source

$$K_{PD} = \frac{I_0 R}{2\pi}$$

$$L(s) = \left(\frac{I_0 R}{2\pi} + \frac{I_0}{2\pi SC} \right) \cdot \frac{2\pi K_{VCO}}{N \cdot S}$$

$$= \frac{(1 + SRC)\, K_{VCO} I_0 R}{N S^2 RC}$$

$$\omega_z = \frac{1}{RC}$$



for $\omega \simeq \omega_{u,loop}$, the unity-gain frequency

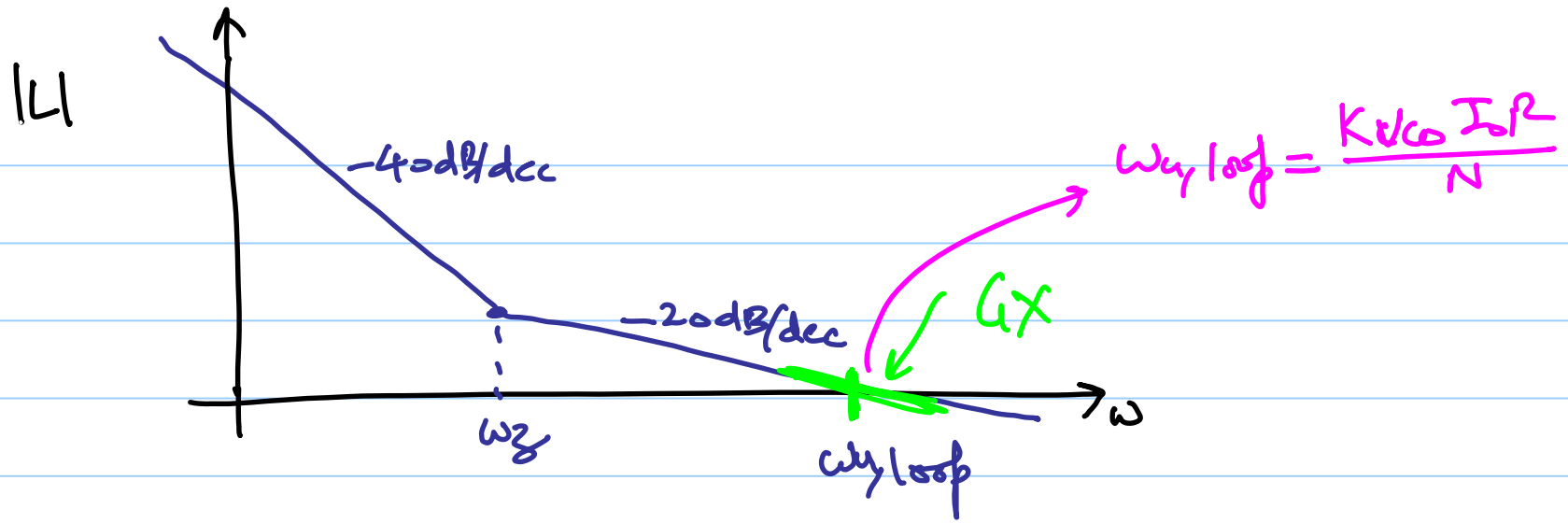
$\omega >> \omega_z$

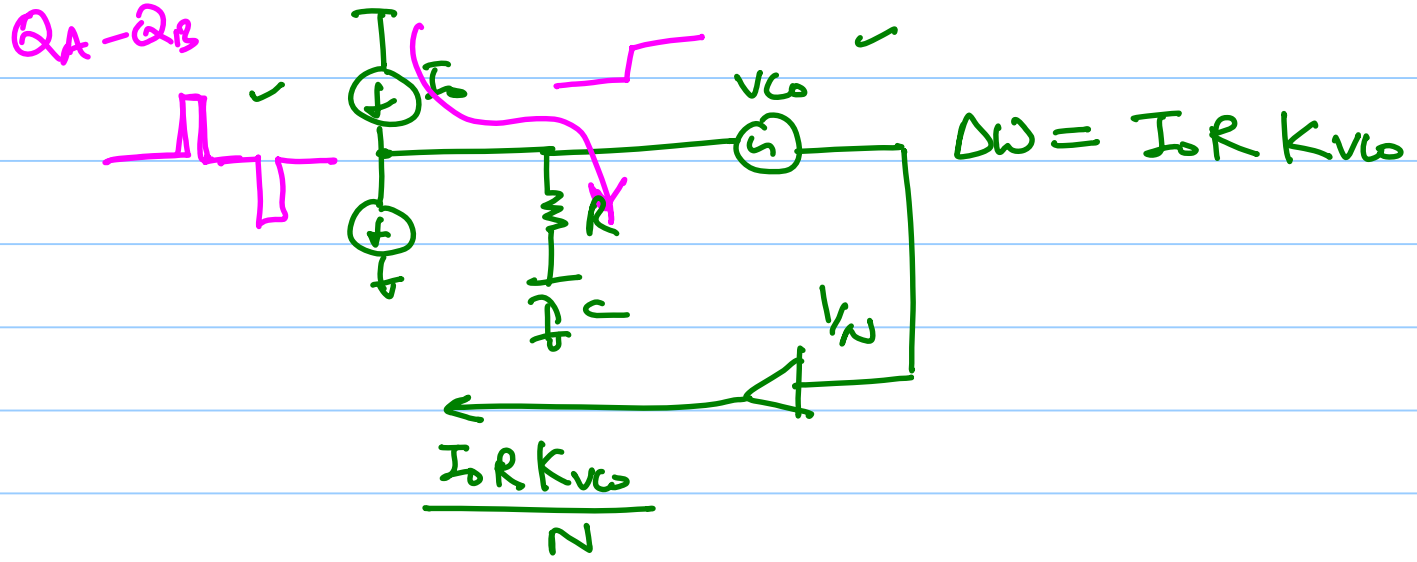
$1 + SRC \simeq SRC$

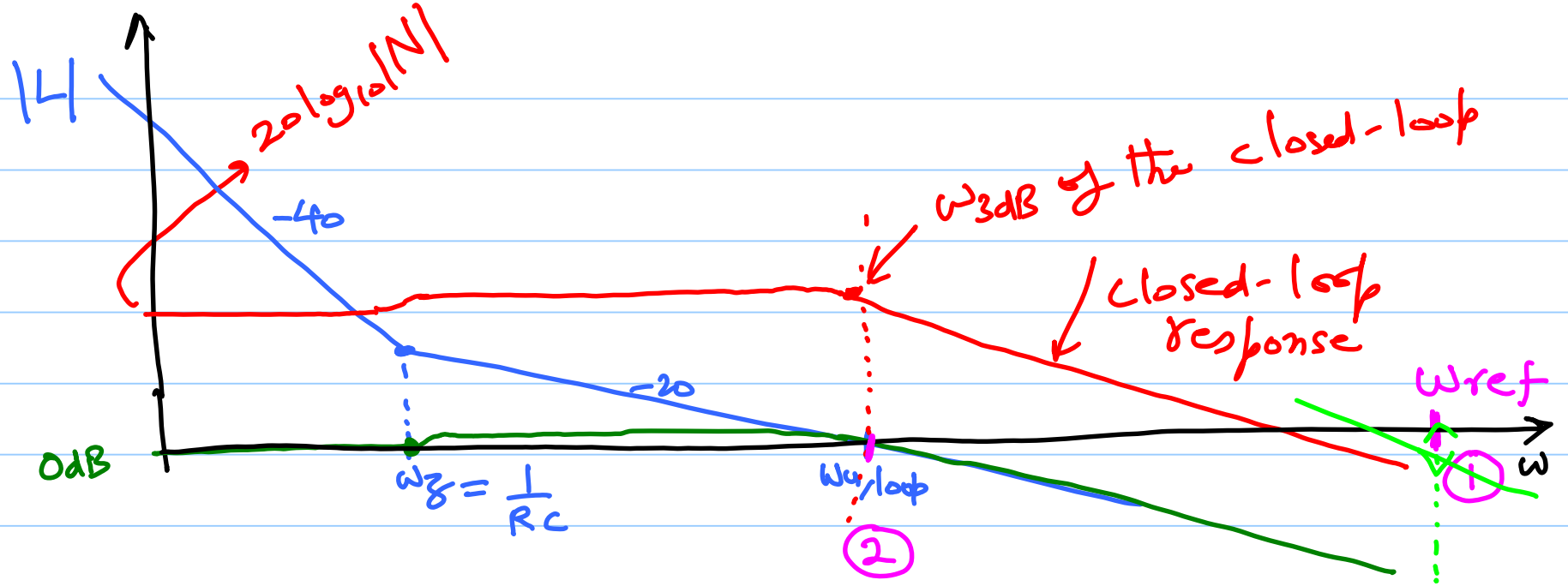
$$L(s) \simeq \frac{SRC \cdot K_{VCO} I_0 R}{S^2 RC \cdot N}$$

$$= \frac{K_{VCO} I_0 R}{SN} \Rightarrow$$

$$\boxed{\omega_{u,loop} = \frac{K_{VCO} I_0 R}{N}}$$


|L|
-40dB/dec
-20dB/dec
ω
ωz
ωu,loop
GX
ωu,loop = KVCO IoR / N


QA-QB
Io
VCO
R
C
1/N
ΔW = IoR KVCO
IoR KVCO / N



$\omega_① \gg \omega_②$

$\omega_{ref} \gg \omega_{u,loop} \Rightarrow$ $\boxed{\omega_{ref} > 10\,\omega_{u,loop}}$

$\omega_{u,loop} < \frac{\omega_{ref}}{10}$ for CT approximation

① CT approx is valid

② suppression of reference feedthrough

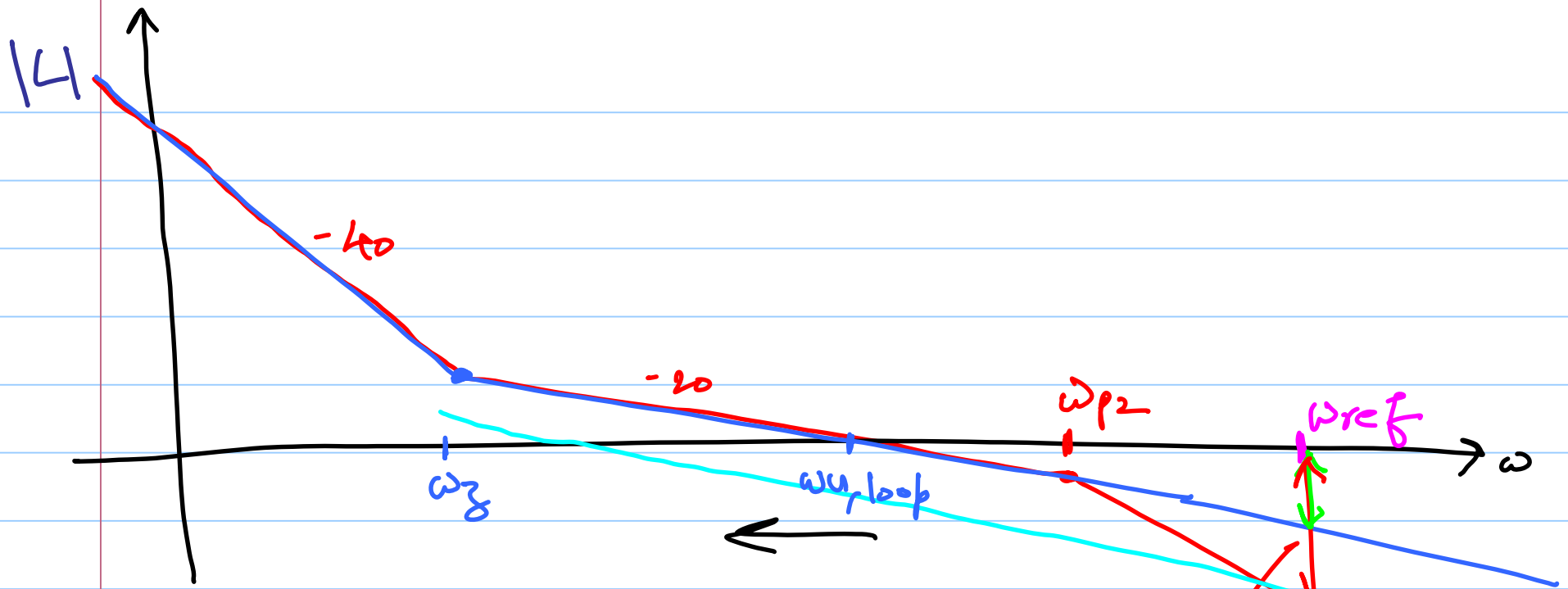
loop-bandwidth

$$\omega_{3dB} \simeq \omega_{u,loop} = \frac{K_{VCO} \cdot I_R}{N}$$

↳ how fast the PLL can switch from one frequency to another ($N = N_0 \rightarrow N_0 + 1$)

* A higher $\omega_{u,loop}$ ⇒ PLL settles faster
⇒ more periodic disturbance from ref in the output

$\omega_{u,loop}$ presents a fundamental tradeoff B/W
Settling speed & noise in the PLL output.

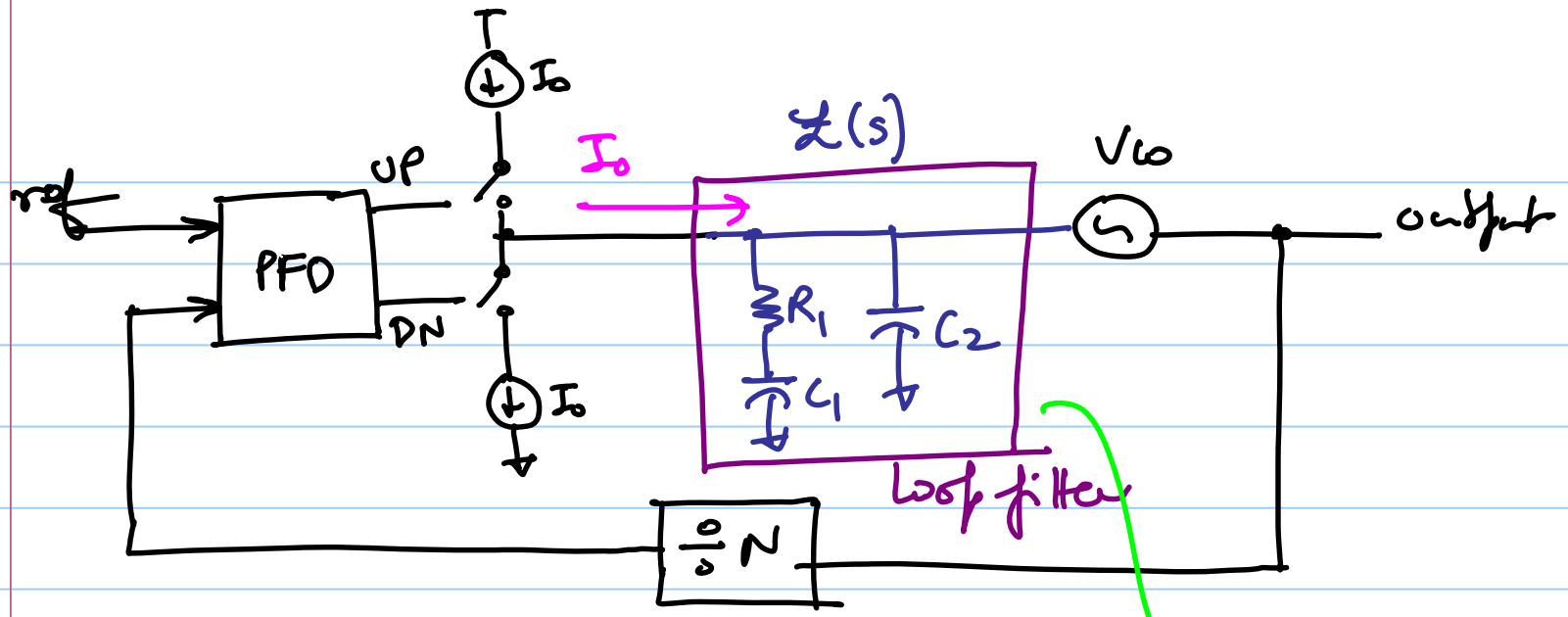


Note that:

$\omega_{p2} > \omega_{u,loop}$.

higher suppression of the reference feed through

without changing the $\omega_{u,loop}$ "loop-BW"



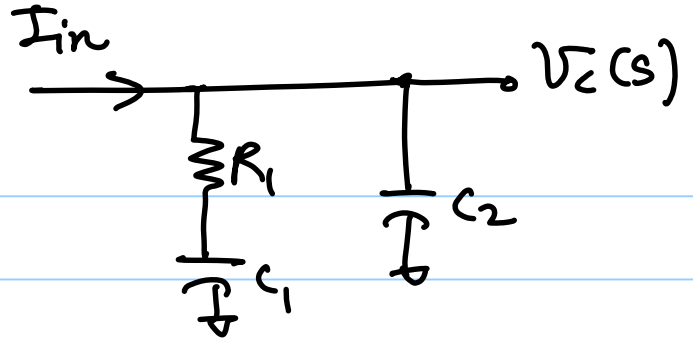
seen in most practical PLLs

2nd order

$$L(s) = \frac{2\pi K_{VCO}}{N \cdot S}\left(\frac{I_o R_1}{2\pi} + \frac{I_o}{2\pi s C_1}\right) = \frac{K_{VCO} I_o}{sN} \cdot Z(s)$$

$Z(s) \rightarrow R_1 + \frac{1}{sC_1}$

* Third-order:



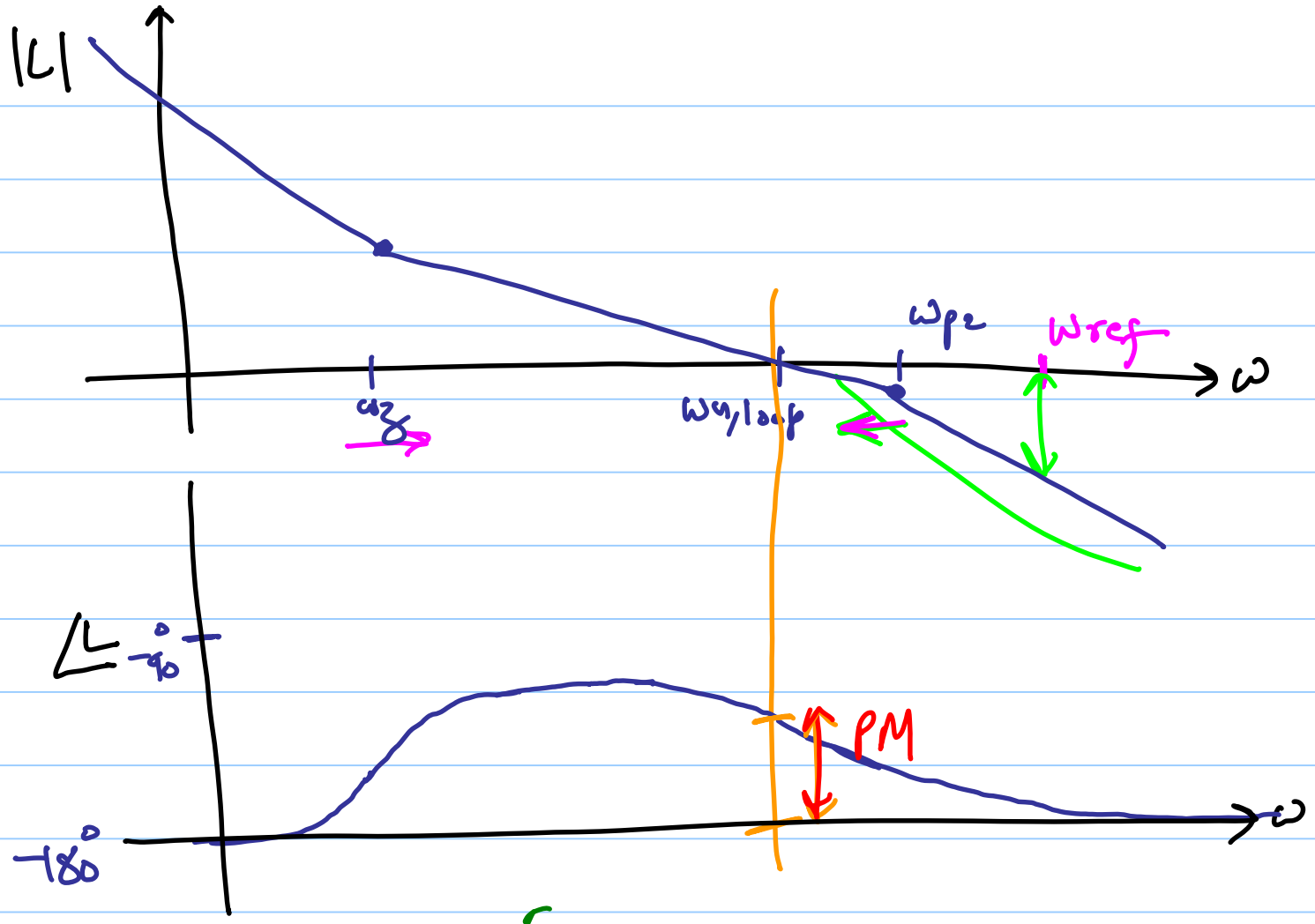
$$Z(s) = \left(R_1 + \frac{1}{sC_1}\right) \| \frac{1}{sC_2}$$

$$= \frac{\left(R_1 + \frac{1}{sC_1}\right)\frac{1}{sC_2}}{R_1 + \frac{1}{sC_1} + \frac{1}{sC_2}} = \frac{(1 + sR_1C_1)}{s(C_1+C_2)\left(1 + sR_1\frac{C_1C_2}{C_1+C_2}\right)}$$

$$= \frac{(1 + sR_1C_1)}{s(C_1+C_2)(1 + sR_1 C_1 \| C_2)}$$

$$\Rightarrow L(s) = \frac{K_{VC} I_o}{s^2(C_1+C_2)N} \cdot \frac{(1 + sR_1C_1)}{(1 + sR_1 C_1 \| C_2)} = \frac{K_{VC} I_o \left(1 + s/\omega_z\right)}{N(C_1+C_2)s^2\left(1 + s/\omega_{p2}\right)}$$

$$\omega_{p2} \simeq \frac{1}{R_1 \cdot C_1 \| C_2}$$



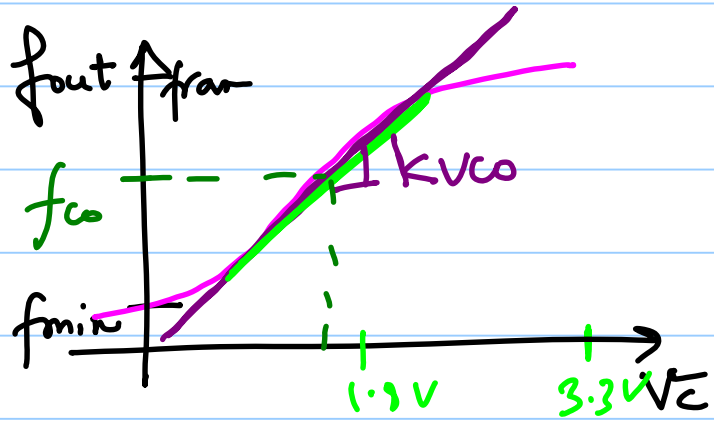
- reference suppression
- phase margin
- loop-bandwidth

PLL Design Example:

Spec: $f_{out} = 1\,GHz$ $\Rightarrow$ $N = 100$

$f_{ref} = 10\,MHz$

$K_{VCO} \equiv$ VCO gain $= 100\ \frac{MHz}{V}$



$\omega_{u,loop} \leq \frac{\omega_{ref}}{10}$

We arbitarily choose $\omega_{u,loop} = \frac{\omega_{ref}}{25} = 400\,kHz \times 2\pi$

$\omega_{u,loop} \simeq \frac{K_{VCO} \cdot I_0 R}{N} = 2\pi \times 400\,kHz$

$\Rightarrow \quad I_0 R = \frac{100 \times 400 \times 10^3}{100 \times 10^6} \times 2\pi \simeq 2.5V$

$\boxed{I_0 R = 2.5V}$

Let's pick $I_o = 200\,mA$ ✗

$\Rightarrow R = 12.5\,\Omega$

we need $\omega_z \ll \omega_{u,loop} = \frac{\omega_{u,loop}}{5}$

$\omega_z = 2\pi \times 8k\ rad/s = \frac{1}{RC}$

$\Rightarrow C = \frac{1}{2\pi}\,\mu F = 159\,nF$

Redesign:

$I_o = 200\,\mu A \Rightarrow R = 12.5\,k\Omega$

$C = 159\,pF$

Area is dominated by "C"

Time to settle $\Rightarrow$ $t_s = \frac{4.7}{\omega_{u,loop}} = 12.5\,\mu s$

assuming 1st-order

How many cycles of 1GHz ⇒ 12,800 cycles

Need to simulate for > 25000 cycles.