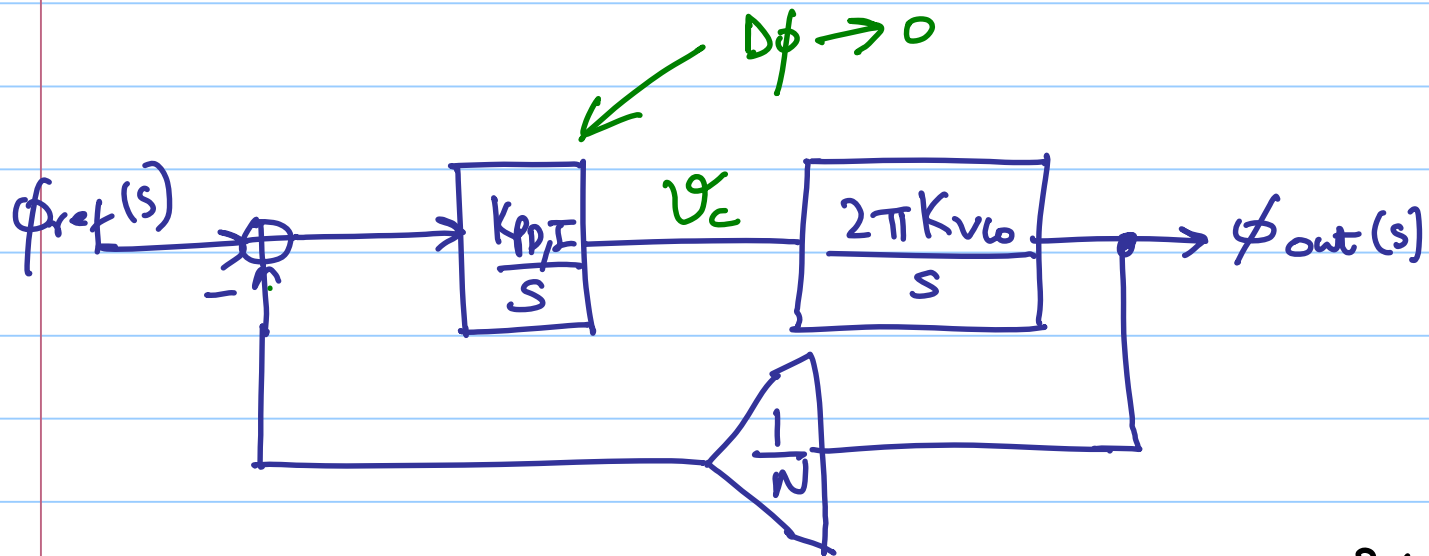


ECE 518 - Lecture 6

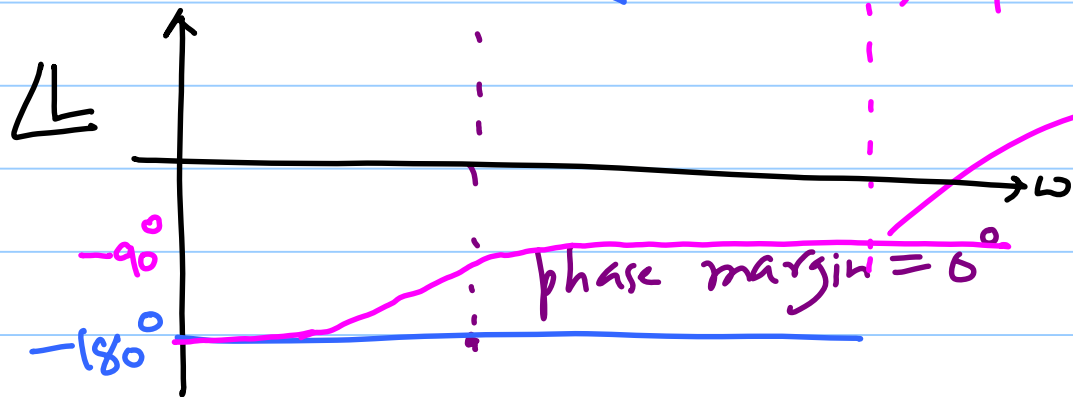
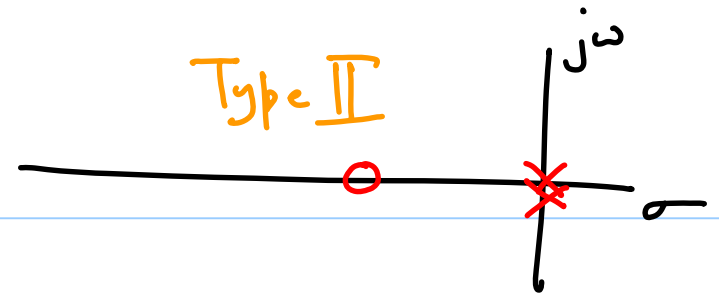
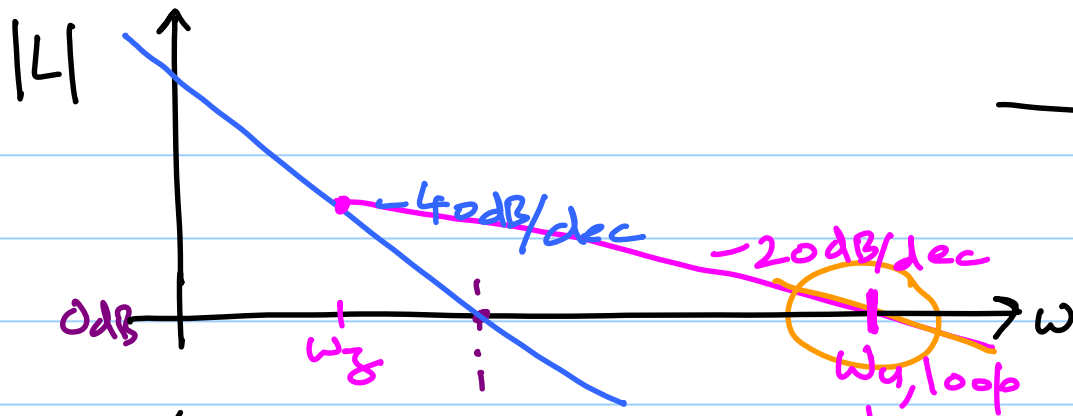
Note Title

2/3/2015



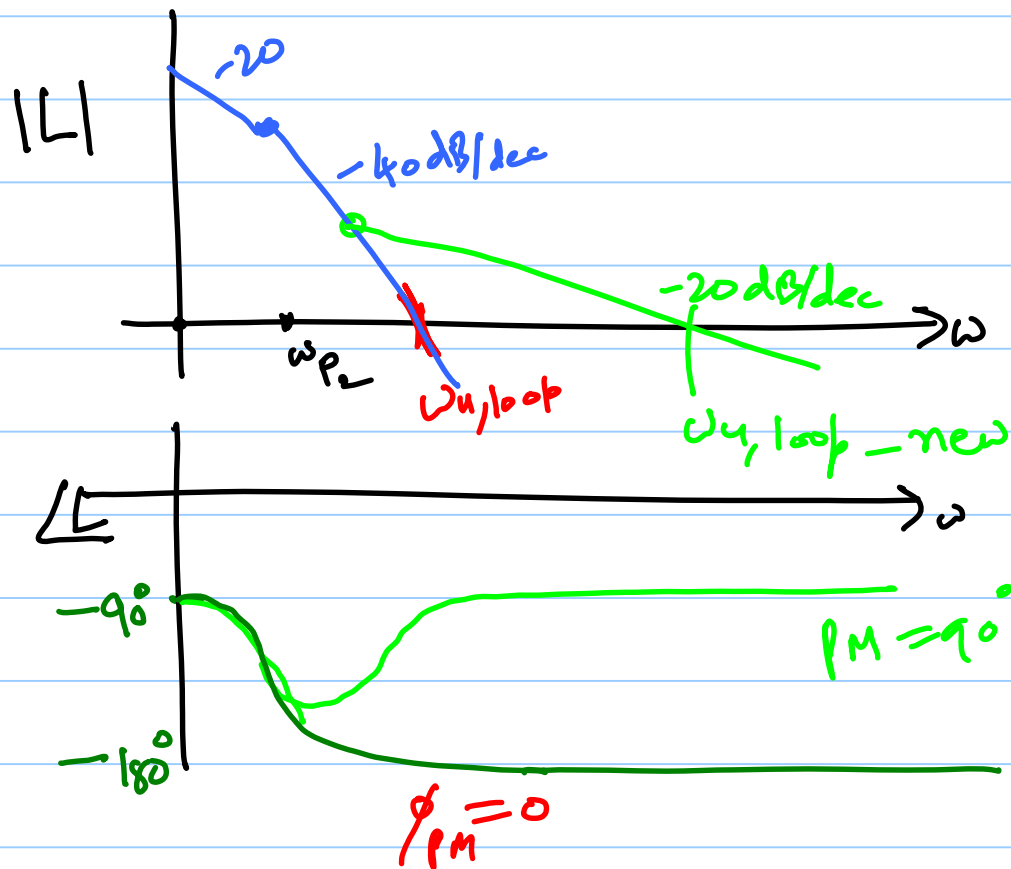
$$L(s) = \frac{2\pi K_{PD,I} \cdot K_{VCO}}{N \cdot s^2}$$

2-poles at DC

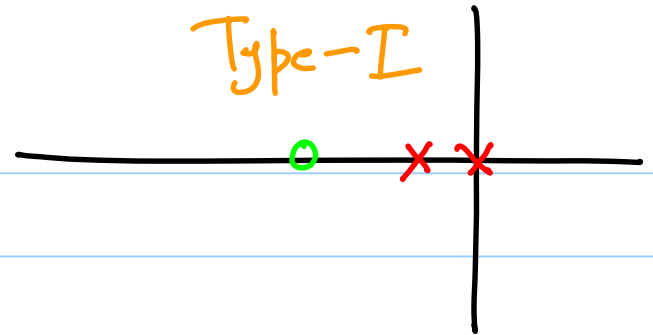


Phase margin $\leq 90^\circ$

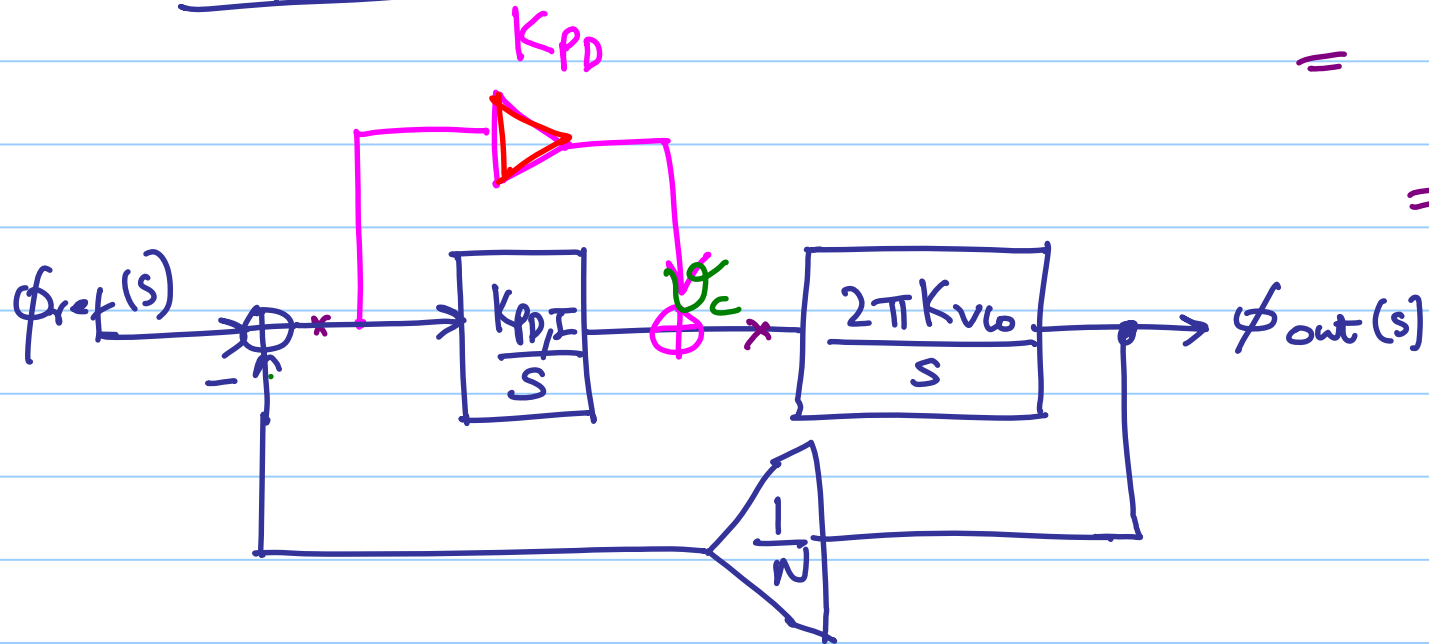
Aside



Type-I



Type-II PLL



$$\begin{aligned}
 LF(s) &= K_{PD} + \frac{K_{PD,I}}{s} \\
 &= \frac{(sK_{PD} + K_{PD,I})}{s} \\
 &= \left(\frac{1 + sK_{PD}/K_{PD,I}}{s/K_{PD,I}} \right) \\
 &= \frac{\left(1 + \frac{s}{\omega_z} \right)}{s/K_{PD,I}}
 \end{aligned}$$

Type II $\Rightarrow$ 2 poles at DC

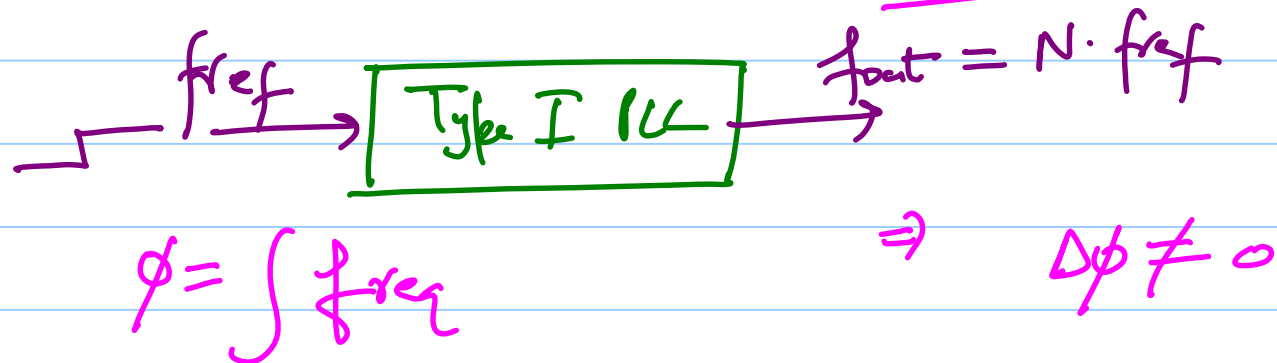
$\hookrightarrow$ not same as the order

$$\omega_z = \frac{K_{PD,I}}{K_{PD}} \checkmark$$

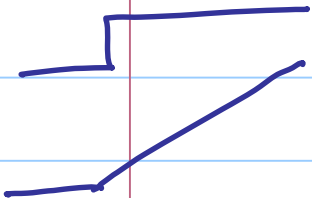
Type II $\Rightarrow$ 2 poles at DC

* With a Type-I system $\Rightarrow$ the steady-state error to a step input = 0

ss error due to a ramp input $\neq 0$



A type II PID $\Rightarrow$ ss error with input step & input ramp = 0



$$\Delta f_{f_{ref}} \rightarrow 0$$

$$\Delta\phi \rightarrow 0$$

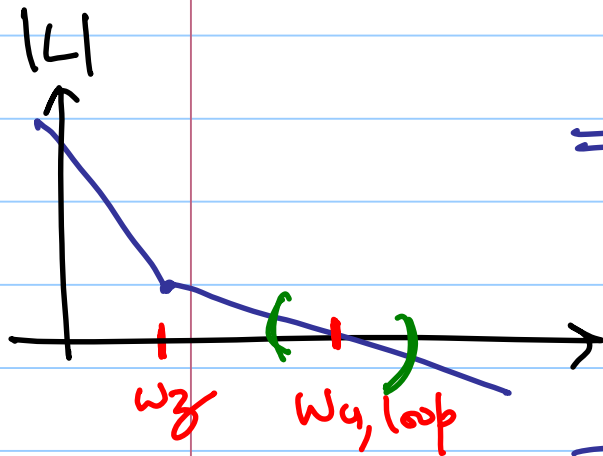
$$L(s) = \frac{1}{\underline{s}} \leftarrow \text{Type I} \longleftrightarrow \underline{\underline{\mu(t)}}$$

$$\frac{1}{\underline{s^2}} \leftarrow \text{Type II} \longleftrightarrow \underline{\underline{t \mu(t)}}$$

$$L(s) = \left(k_{PD} + \frac{k_{PD,I}}{s} \right) \cdot \frac{2\pi K_{VCO}}{s} \cdot \frac{1}{N}$$

$$= \frac{2\pi K_{VCO} (s k_{PD} + k_{PD,I})}{N s^2}$$

$$= 2\pi K_{VCO} \cdot k_{PD,I} \frac{\left(1 + \frac{s k_{PD}}{k_{PD,I}} \right)}{N \cdot s^2}$$



$$= \frac{2\pi K_{VCO} k_{PD,I}}{N} \cdot \frac{(1 + s/\omega_z)}{s^2}$$

$$\omega_z = \frac{k_{PD,I}}{k_{PD}}$$

To find $\omega_{u, loop}$ $|L|=1 \Rightarrow$ find $\omega = \omega_{u, loop}$

$$\underline{\underline{\omega \approx \omega_{u,loop} \gg \omega_z}}$$

$$\left(\frac{s}{\omega_z} + 1\right) \approx \frac{s}{\omega_z} \quad \text{for } \omega \gg \omega_z$$

pole-zero cancellation

$$L(s) \approx \frac{2\pi K_{v\omega} K_{PD,I}}{N} \cdot \frac{1}{s^2} \cdot \frac{s}{\omega_z}$$

$$= \frac{2\pi K_{v\omega} \cancel{K_{PD,I}}}{N s} \left(\frac{K_{PD}}{\cancel{K_{PD,I}}} \right)$$

$$= \frac{2\pi K_{v\omega} K_{PD}}{N s}$$

$$\text{for } |L|=1$$

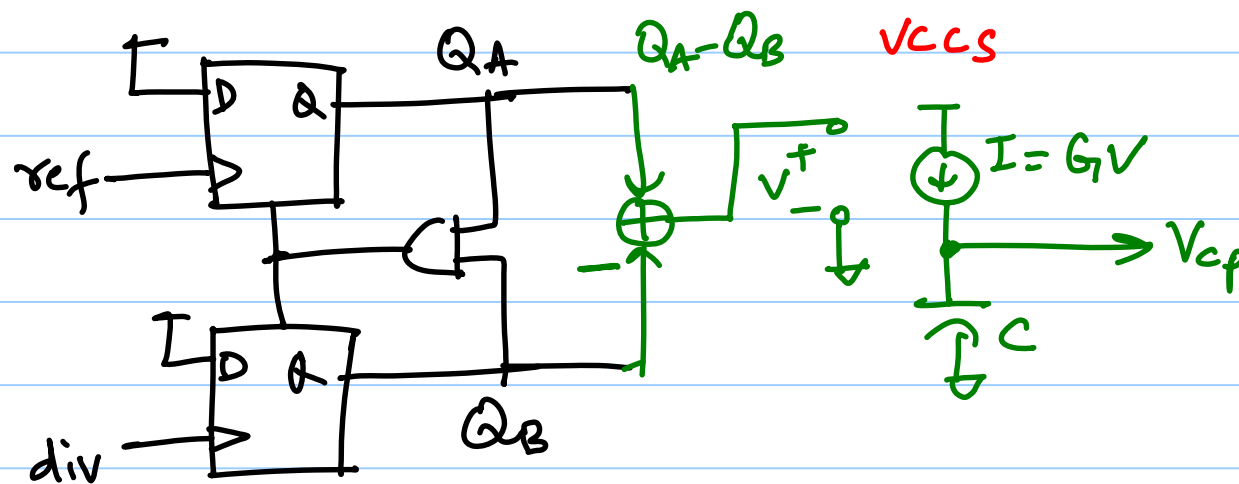
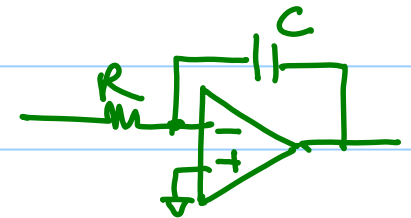
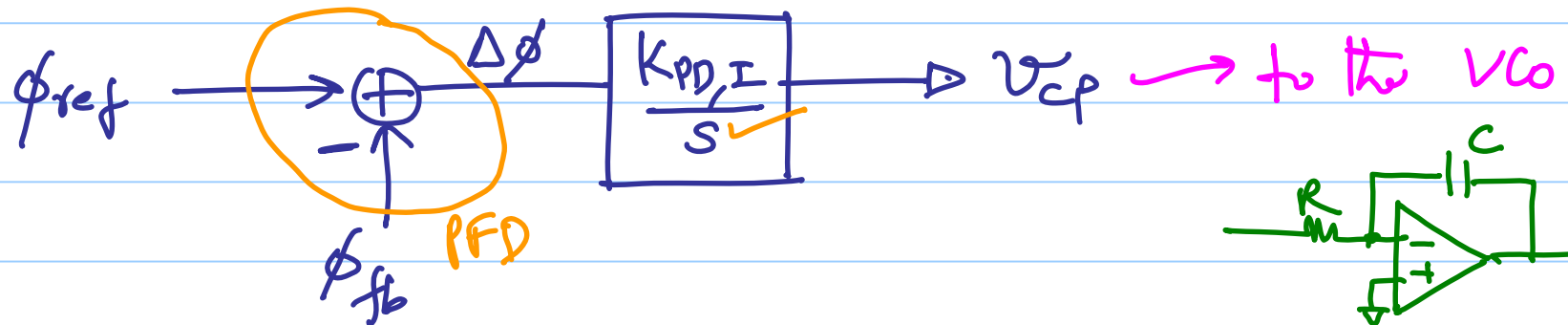
$$\Rightarrow$$

$$\omega_{u,loop} \approx \frac{2\pi K_{v\omega} \cdot K_{PD}}{N}$$

* Σ^n looks the same as the Type-I
PLL

But, $\Delta\phi \rightarrow 0$

* Need to construct the integrating loop-filter

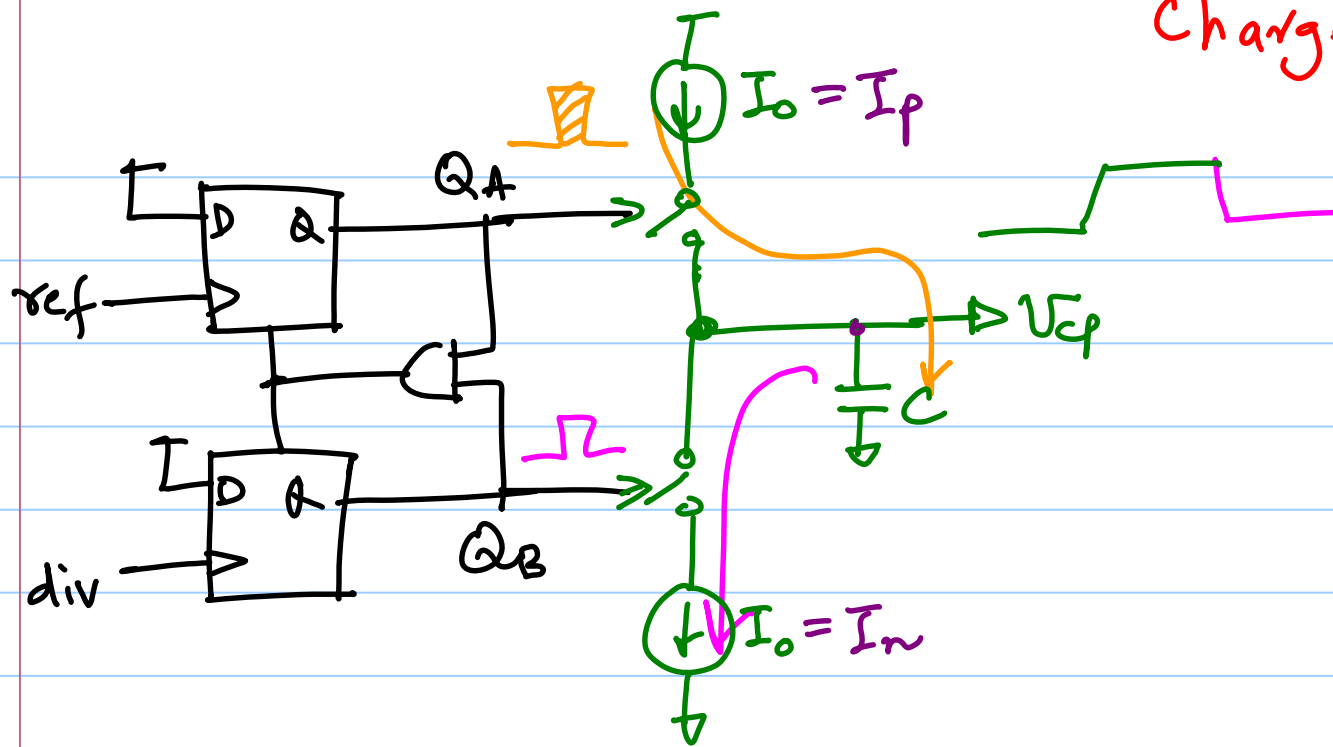


Circuit diagram of a current source and capacitor. A current source i is connected to a capacitor C . The output voltage is V_c .

$$V_c = \frac{1}{C} \int i dt$$

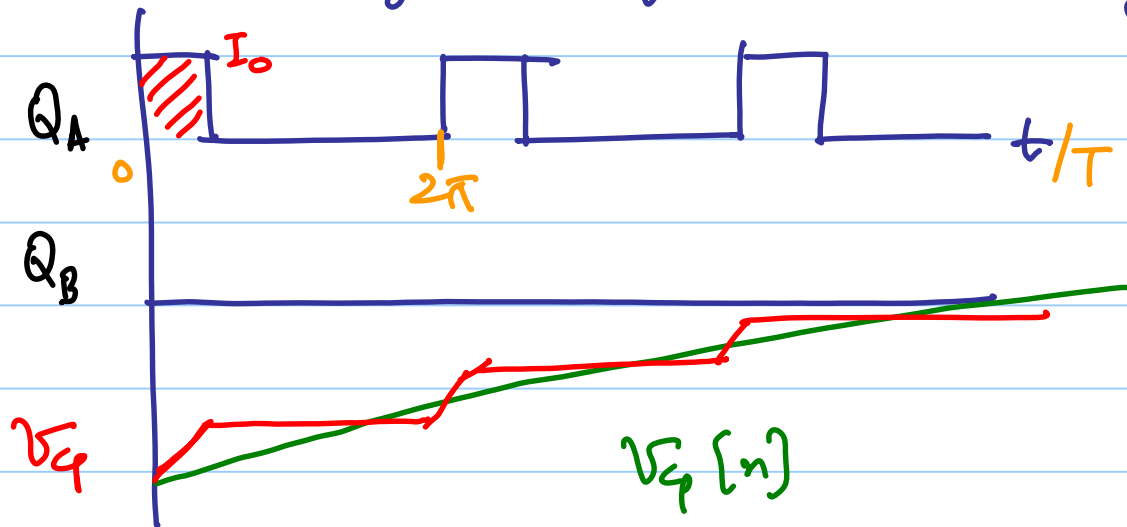
$$= \frac{I}{sC}$$

Charge-pump PLL



push current $Q_A > 0$
pull current $Q_B > 0$

* Let's say the ref clock is leading div

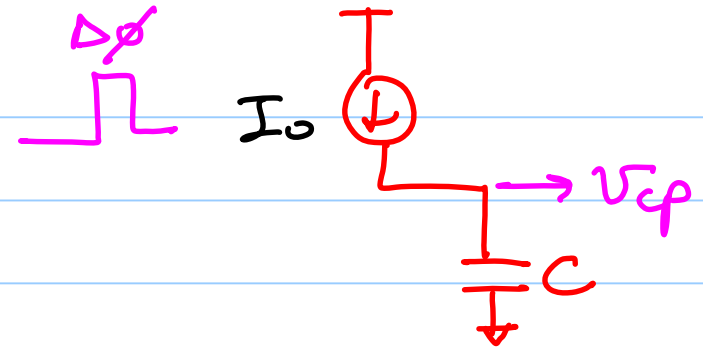
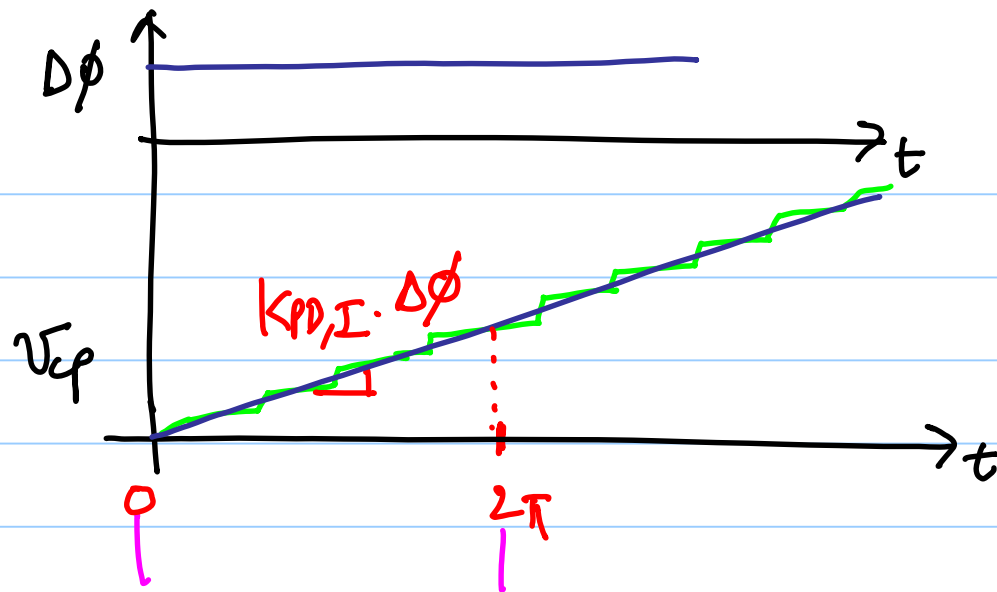


DT operation of
the PLL

CT approximation
for $\omega_{n,loop} < \omega_{ref}$
 $\omega_{n,loop} \leq \frac{\omega_{ref}}{10}$

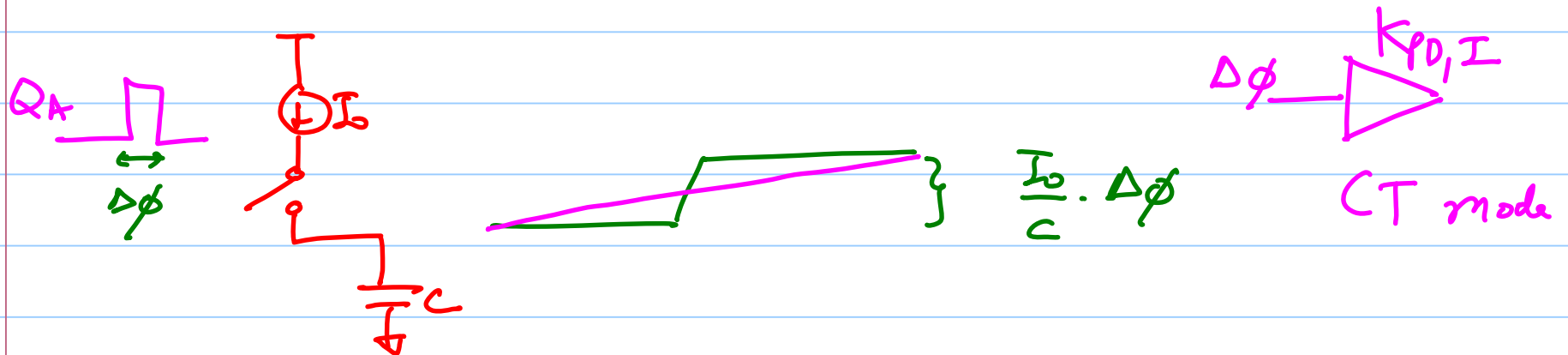
We can approximate this system as a CT for analysis
as long as $\omega_{cl,loop} \leq \frac{\omega_{ref}}{10}$

$\Rightarrow$ PLL response is much slower than
the frequency of phase detection
(sampling)



change in V_{cp} in one cycle = $\frac{I_o}{C} \cdot \Delta\phi$
of ω_{ref}

$$= K_{PD,I} \cdot \Delta\phi \cdot 2\pi$$



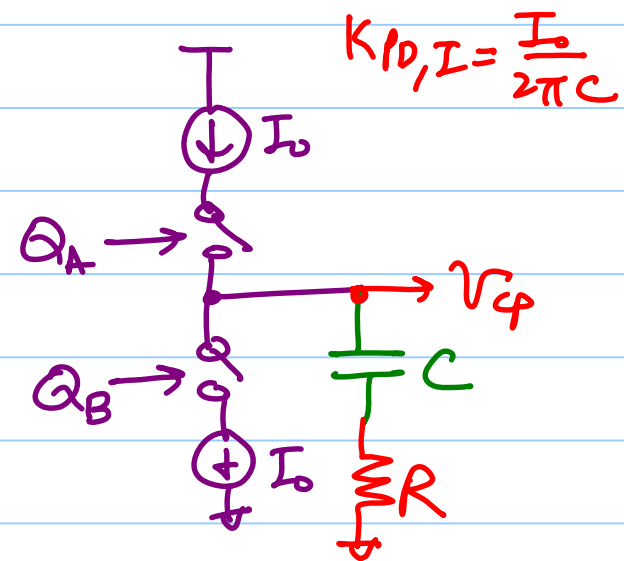
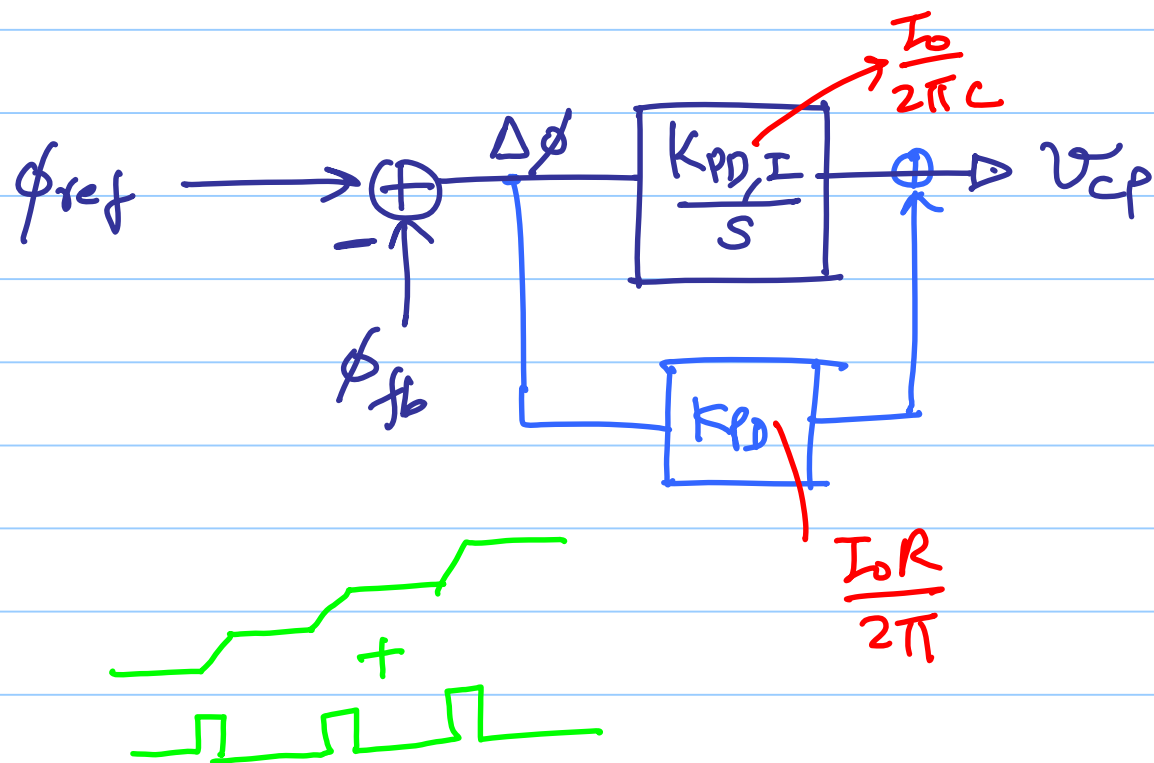
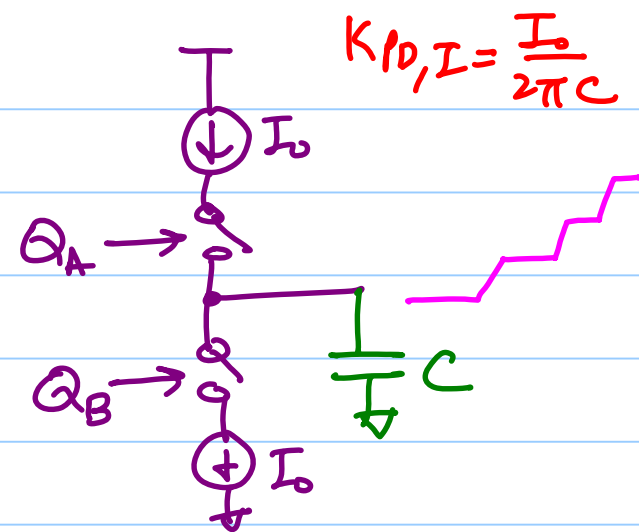
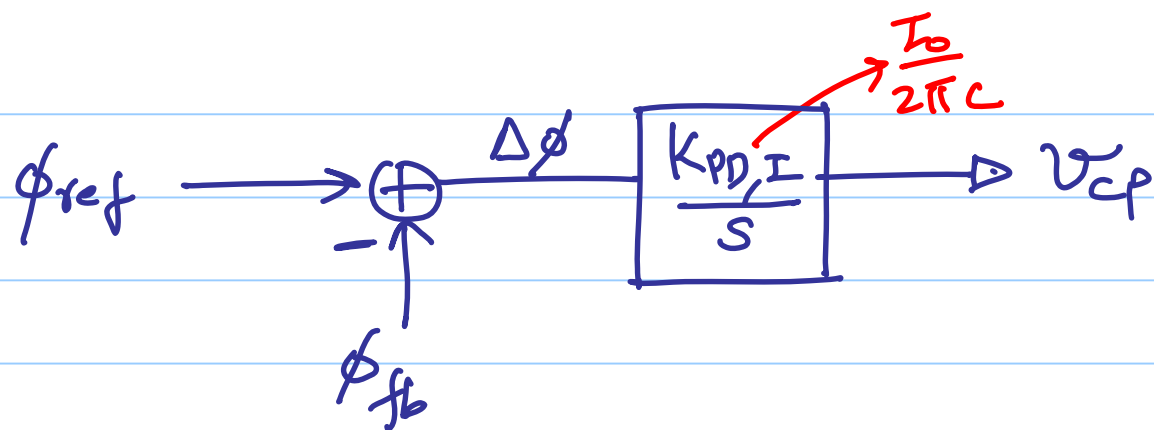
matching the DT step = CT approx by a $\frac{K_{PD}I}{s}$ block

$$\frac{I_0}{C} \cdot \cancel{\Delta\phi} = K_{PD,I} \cdot \cancel{\Delta\phi} \cdot 2\pi$$

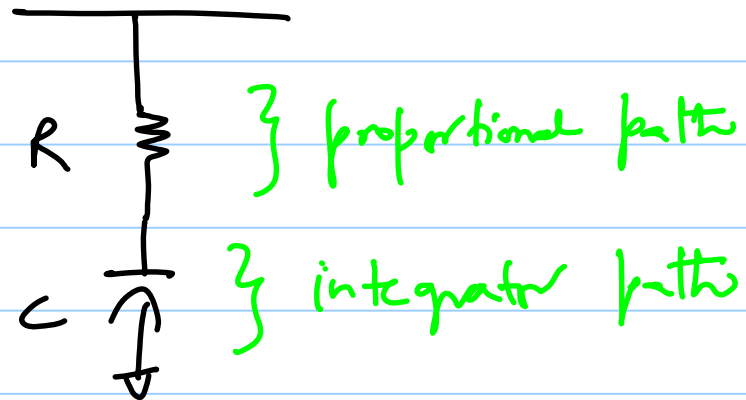
$$K_{PD,I} = \frac{I_0}{2\pi C}$$

* assuming a LT system

* in reality the system is DT and
NL

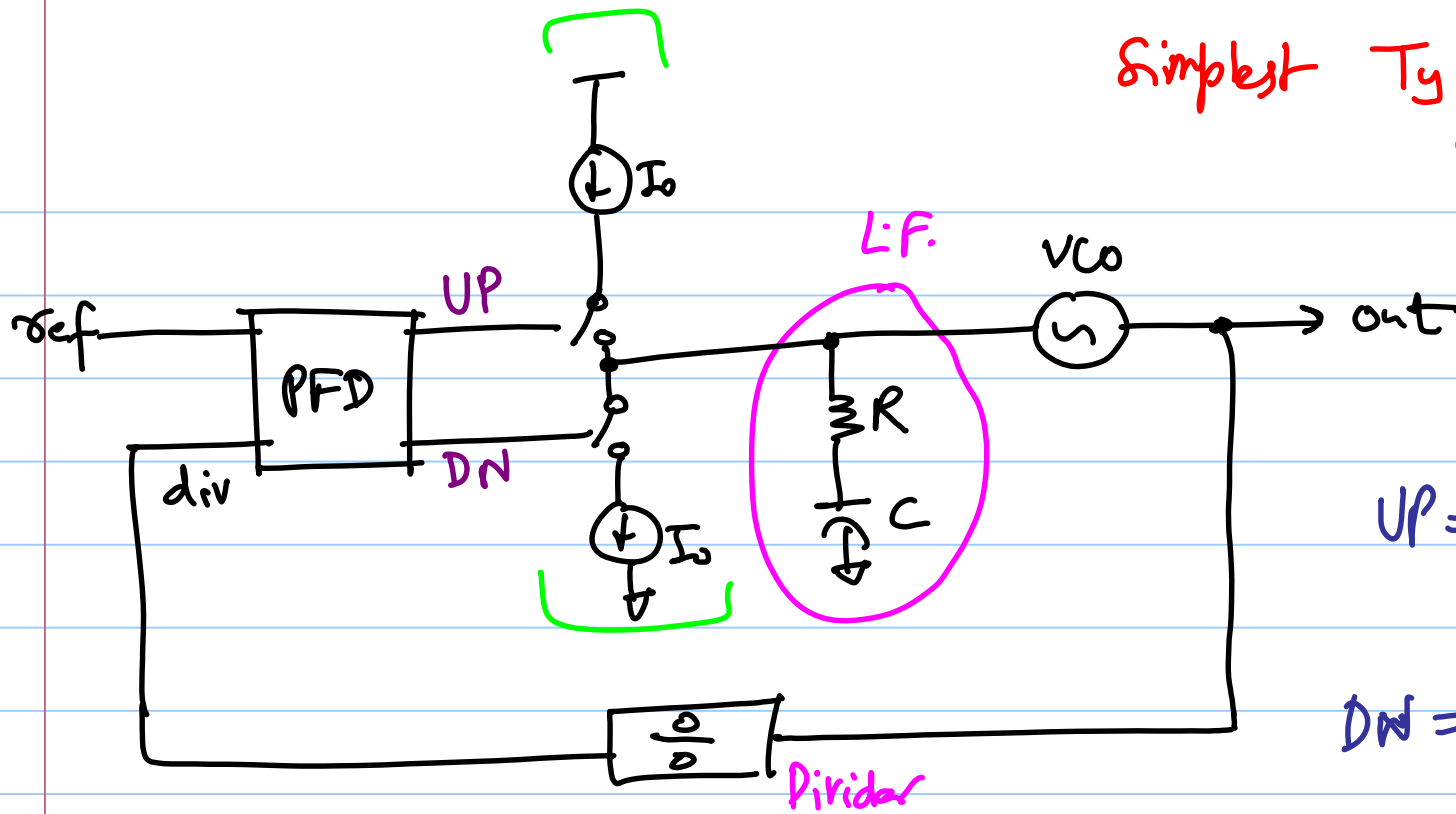


Same logic before



$$K_{PD} = \frac{I_0 R}{2\pi}$$

Simplest Type-II CP PLL architecture



UP $\Rightarrow$ increment V_{CO} frequency

DN $\Rightarrow$ decrement V_{CO} frequency