ECE 518- Lecture 24

Note Title 4/7/2015

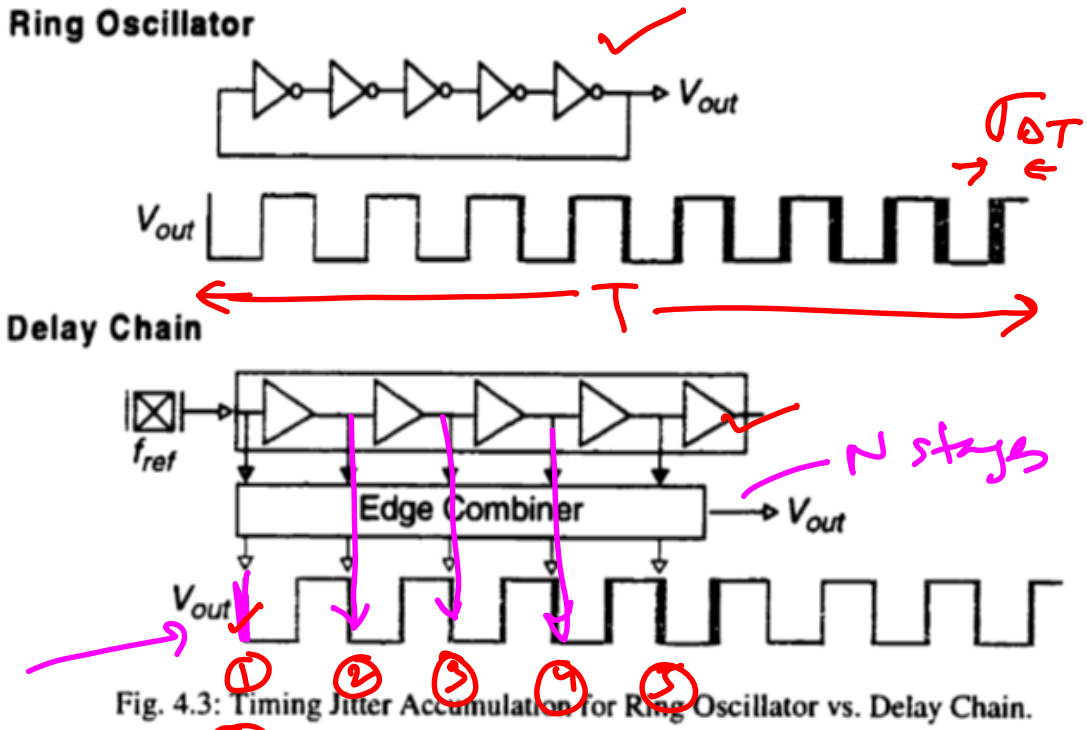


Fig. 4.3: Timing Jitter Accumulation for Ring Oscillator vs. Delay Chain.

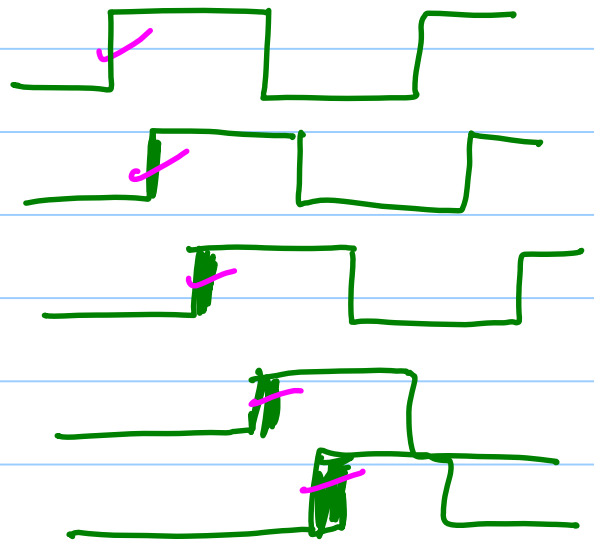
$\sigma_{\Delta T} \propto \sqrt{T}$

T

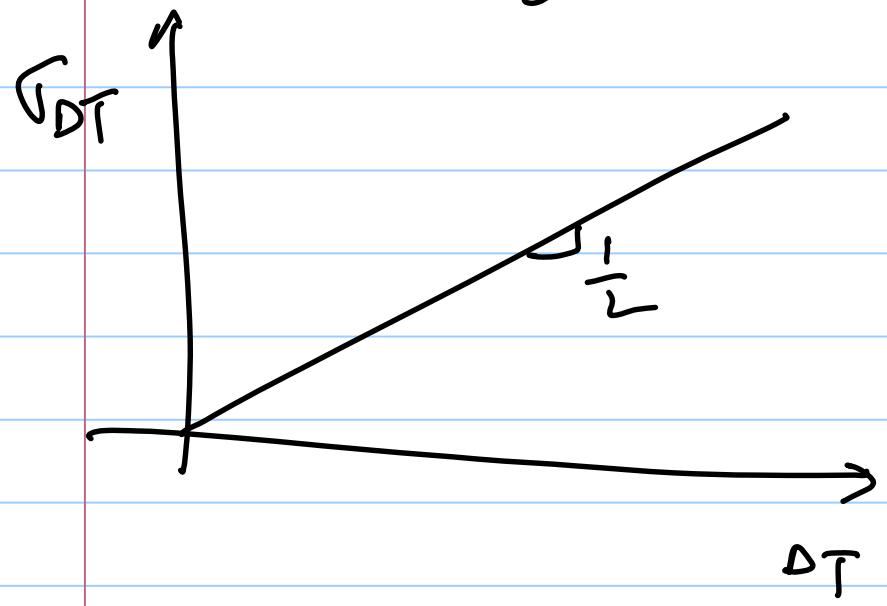
N stages

@ N tap

Multiplying DLL

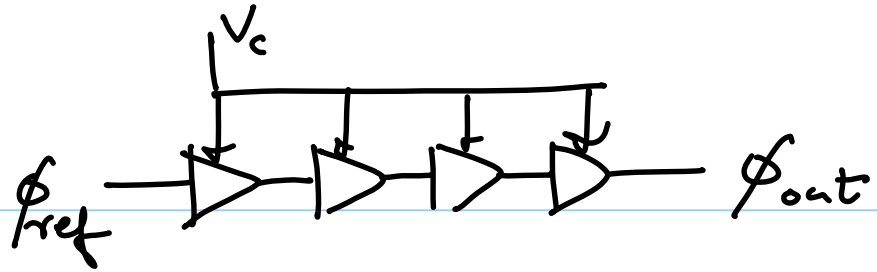


Ring VCO



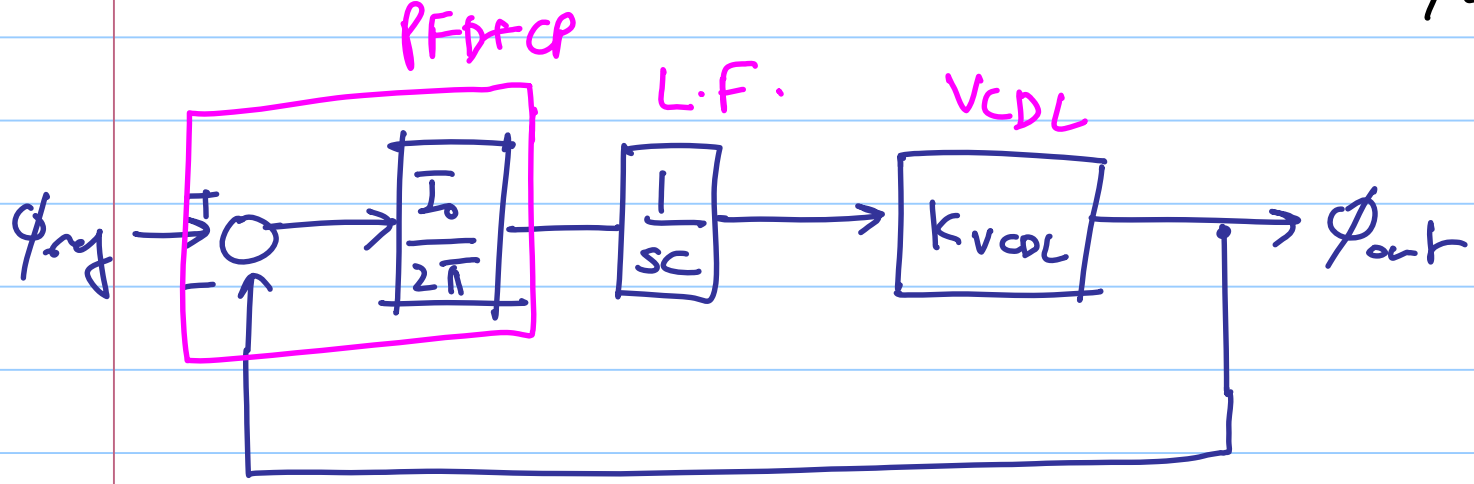
Delay line with edge comb.

Phase-domain Model



$$\phi_{out} = \phi_{ref} + K_{VCDL} V_c$$

$$K_{VCDL} \rightarrow \frac{rad}{V}$$



$$L(s) = \frac{I_0}{2\pi} \cdot \frac{K_{VCDL}}{sC}$$

← Type-I, 1st order

$$H_{CL}(s) = \frac{\phi_{out}}{\phi_{ref}}(s) = \frac{L(s)}{1+L(s)}$$

$$= \frac{\frac{I_o}{2\pi}\frac{K_{VCDL}}{sC}}{1+\frac{I_o}{2\pi}\frac{K_{VCDL}}{sC}}$$

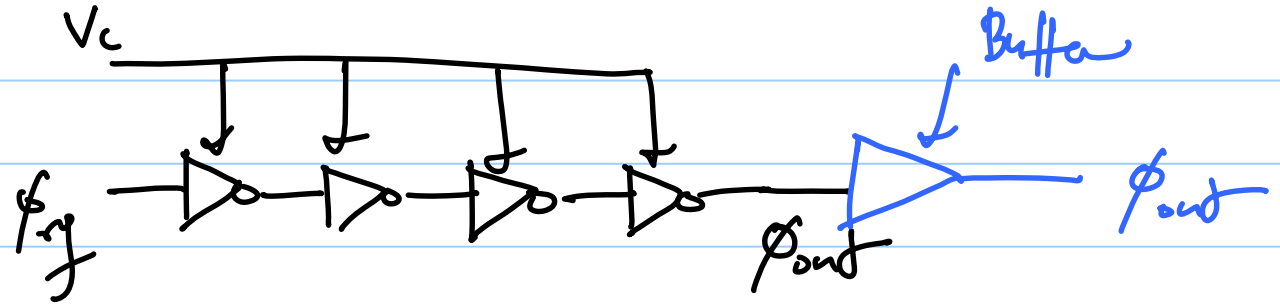
$$= \frac{1}{1+\frac{2\pi sC}{I_o \cdot K_{VCDL}}}$$

$$= \frac{1}{1+s/\omega_{3dB}}$$

$$\omega_{3dB} = \omega_{u,loop} = \frac{I_o \cdot K_{VCDL}}{2\pi C}$$

$$\text{rise-time} \Rightarrow \frac{2.2}{\omega_{3dB}} = 2.2\,\tau$$

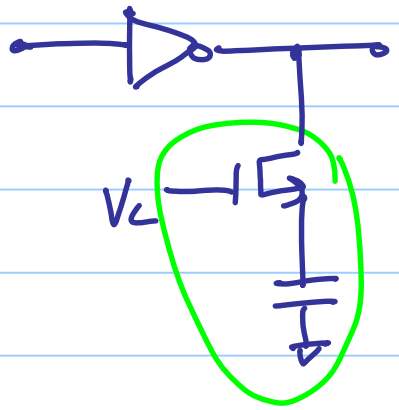
VCDL design



current-starved delay cells

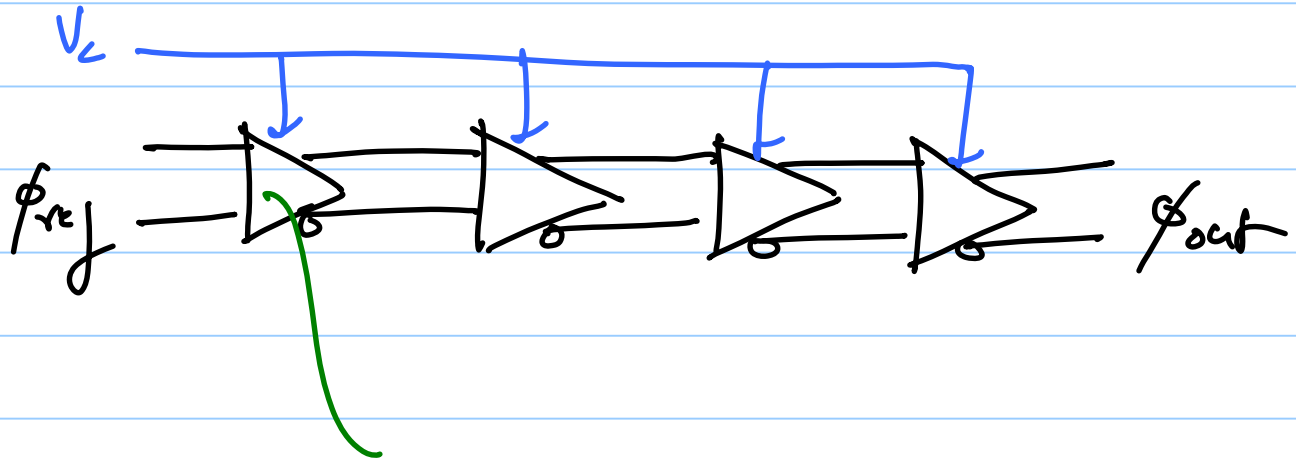
V_{DD}- tuning

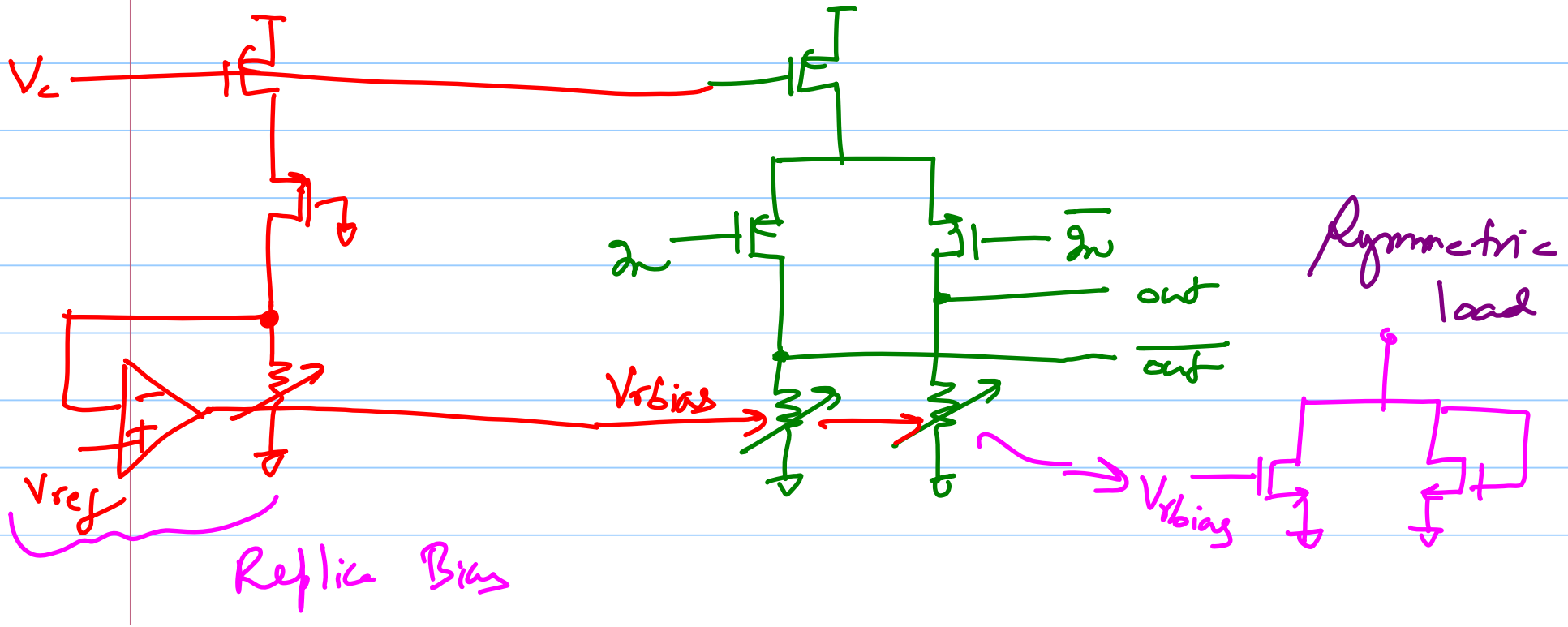
load- tuning



$C_{eff} = f(V_c)$

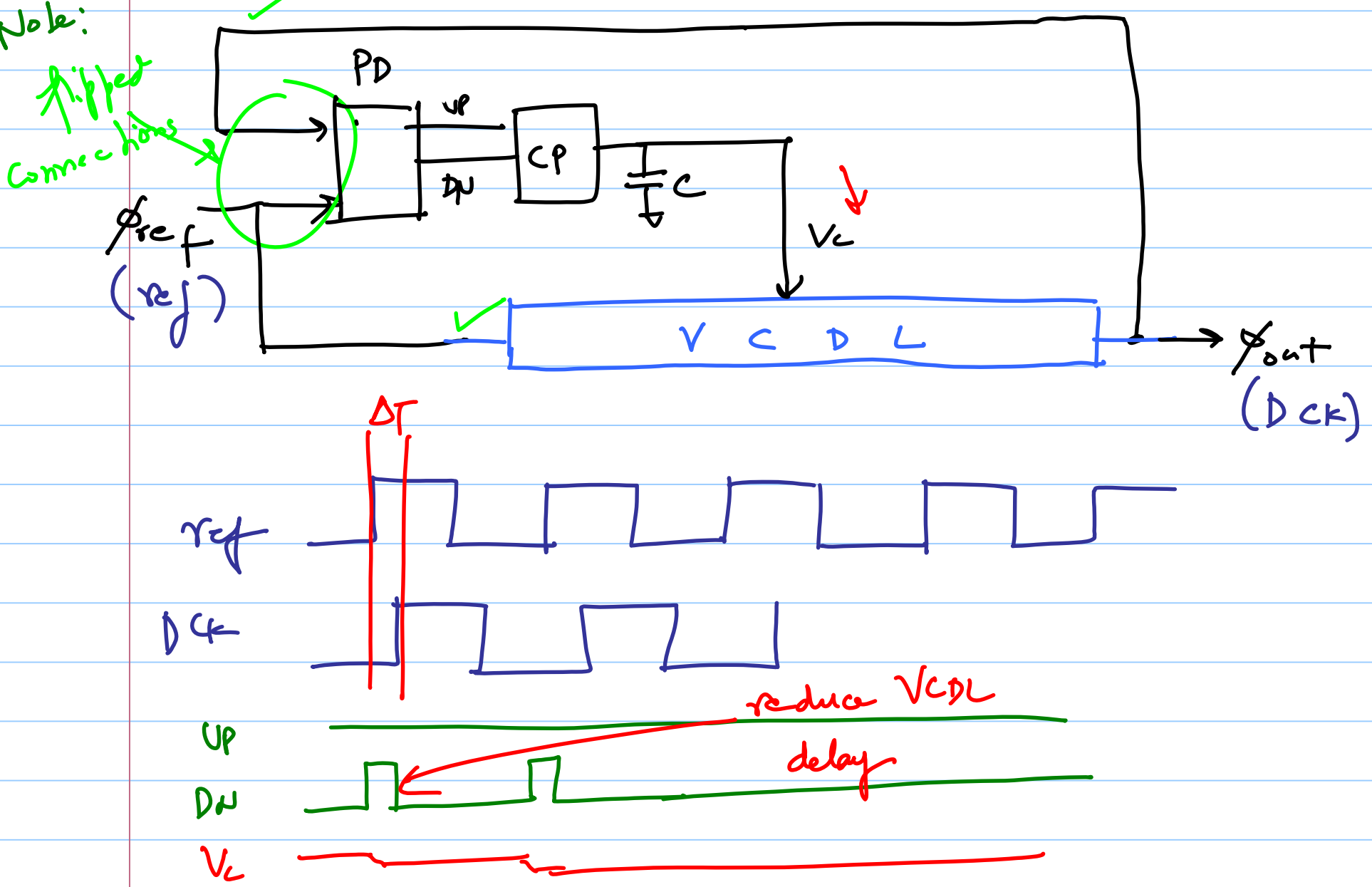
PSRR issues with single-ended delay cells.


V_c
ϕ_{ref}
ϕ_{out}


V_c
in
$\overline{in}$
out
$\overline{out}$
V_{rbias}
V_{ref}
Replica Bias
Symmetric load
V_{rbias}

Harmonic locking

Note:

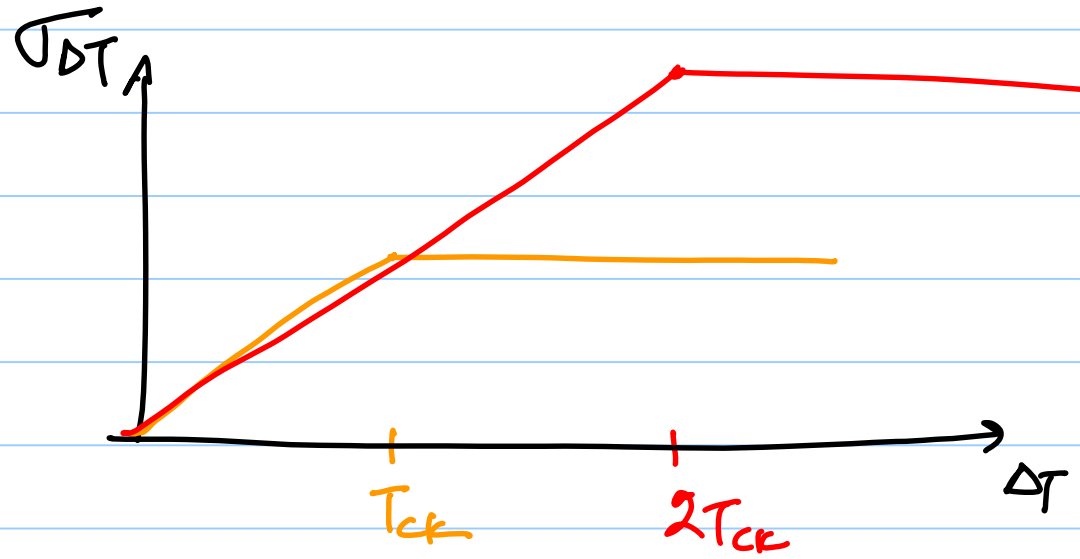


VCDL delay $\longrightarrow T_D \backsim \frac{T_{clk}}{2} \rightarrow 2.5\, T_{CLK}$

VCDL tuning range

Can possibly lock with

$T_D = 2\,T_{ck}$ instead of T_{ck}



more jitter accumulation in DCK.

* false locking ⇒

false-lock detection logic

↳ reset the VCDL to $T_{D,min}$

* We could limit VCDL delay

$$0.5T_{CK} < T_D < 1.5T_{CK}$$

but then we are restricted to

around $f_{CK} = \frac{1}{T_{CK}}$