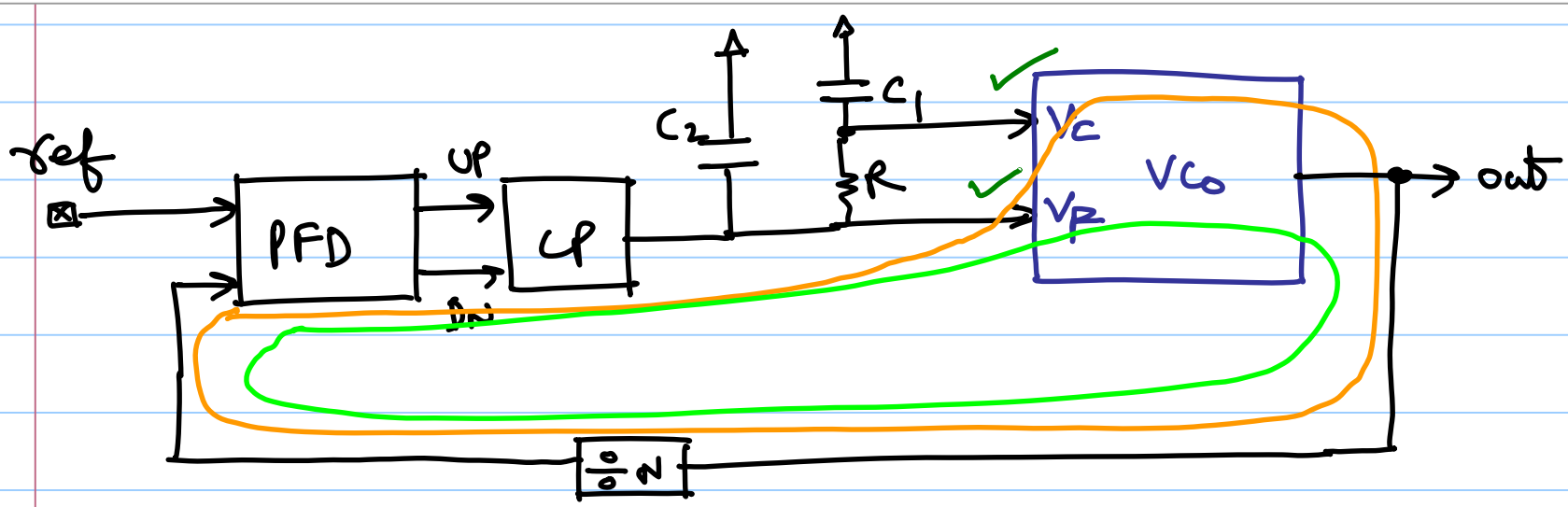
# ECE 518 – Lecture 21

Note Title 4/2/2015




Split-tuned PLL with continuous tuning

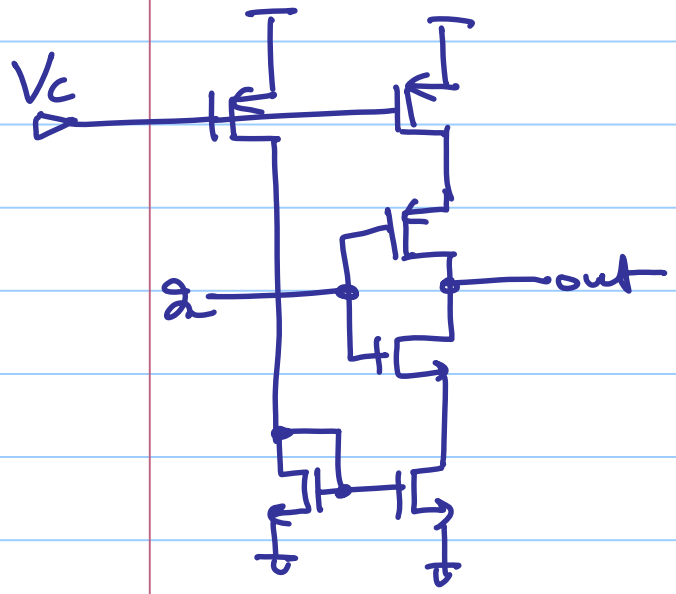
high-gain coarse cntrl ($V_C$)

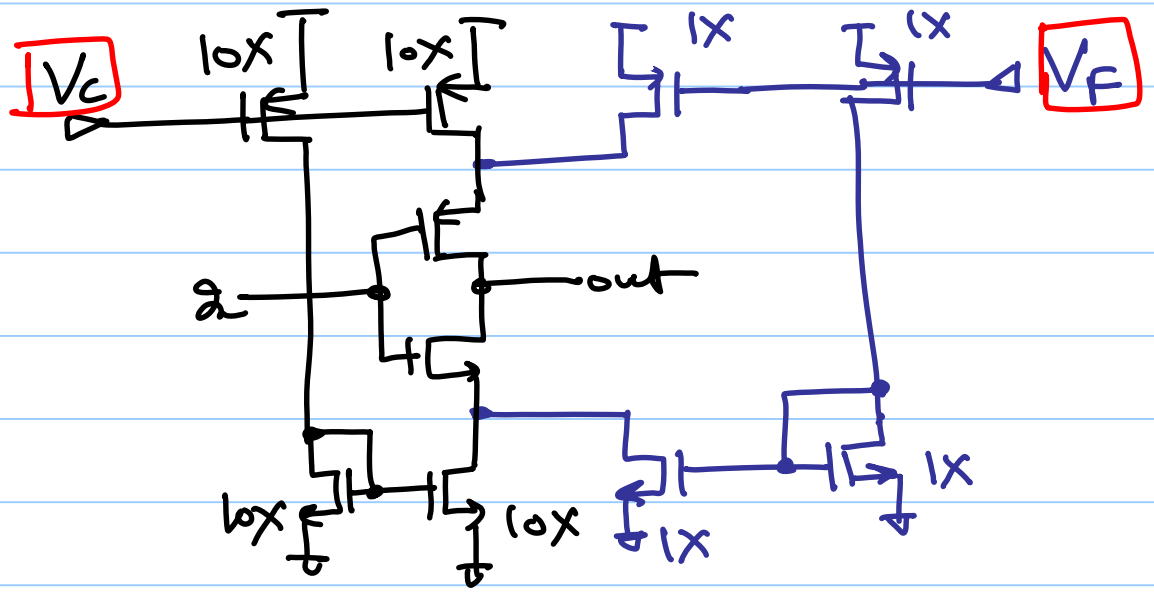
low-gain fine cntrl ($V_F$)

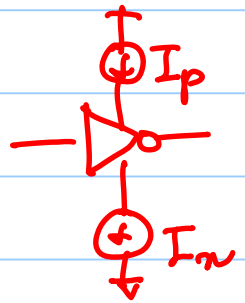
* Two coupled feedback loops

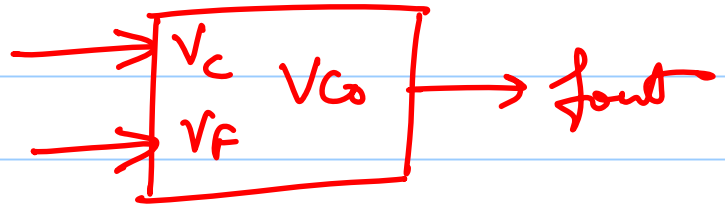
  * potential instability

# Example Split-tuned delay cell



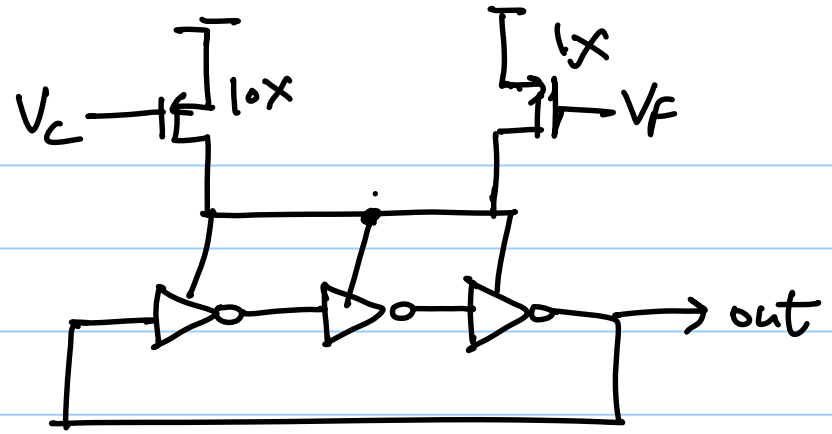




Coarse $K_{VCO}$ gain = 10 X

fine $V_{CO}$ gain

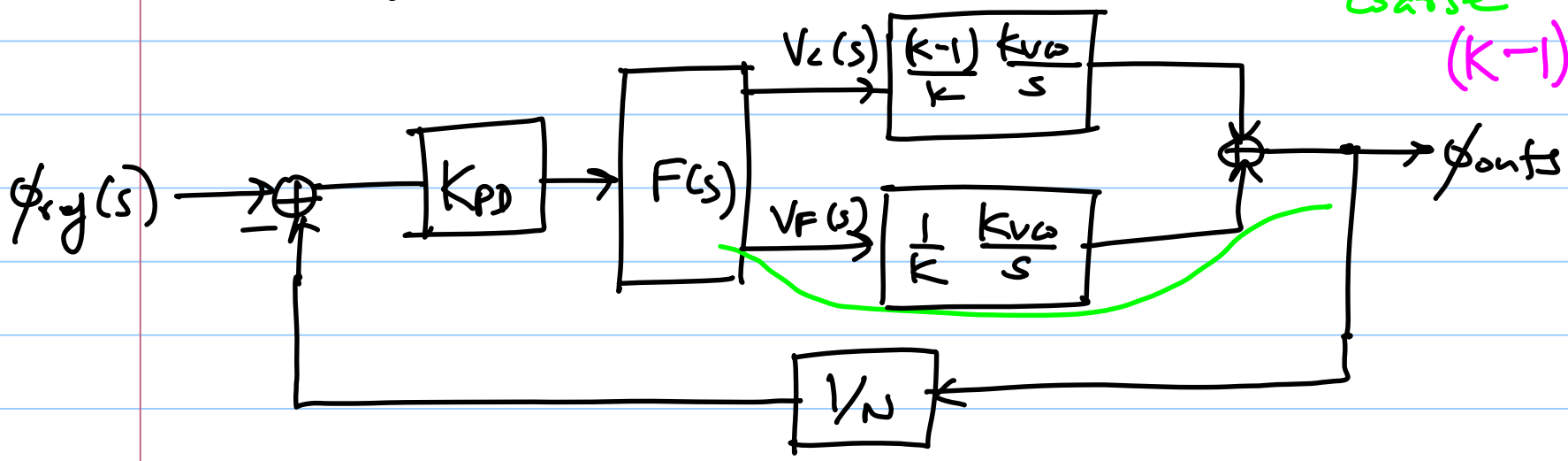

$V_C$
10x
1x
$V_F$
out

# Stability Analysis

$\frac{(K-1)K_{VCO}}{K}$ & $\frac{K_{VCO}}{K}$

coarse | fine

$(K-1):1$

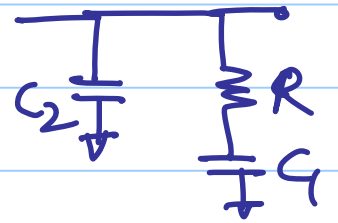



loop-gain

$$LG(s) = \frac{I_{cp}}{2\pi}\frac{F(s)\frac{K_{VCO}}{K}}{s\cdot N} + \frac{I_{cp}}{2\pi}\cdot\frac{F(s)}{1+sRC_1}\cdot\frac{(K-1)}{K}\cdot\frac{K_{VCO}}{s}$$

$$= \frac{I_{cp}}{2\pi}\frac{F(s)}{N}\frac{K_{VCO}/K}{s}\left(1+\frac{K-1}{1+sRC_1}\right)$$

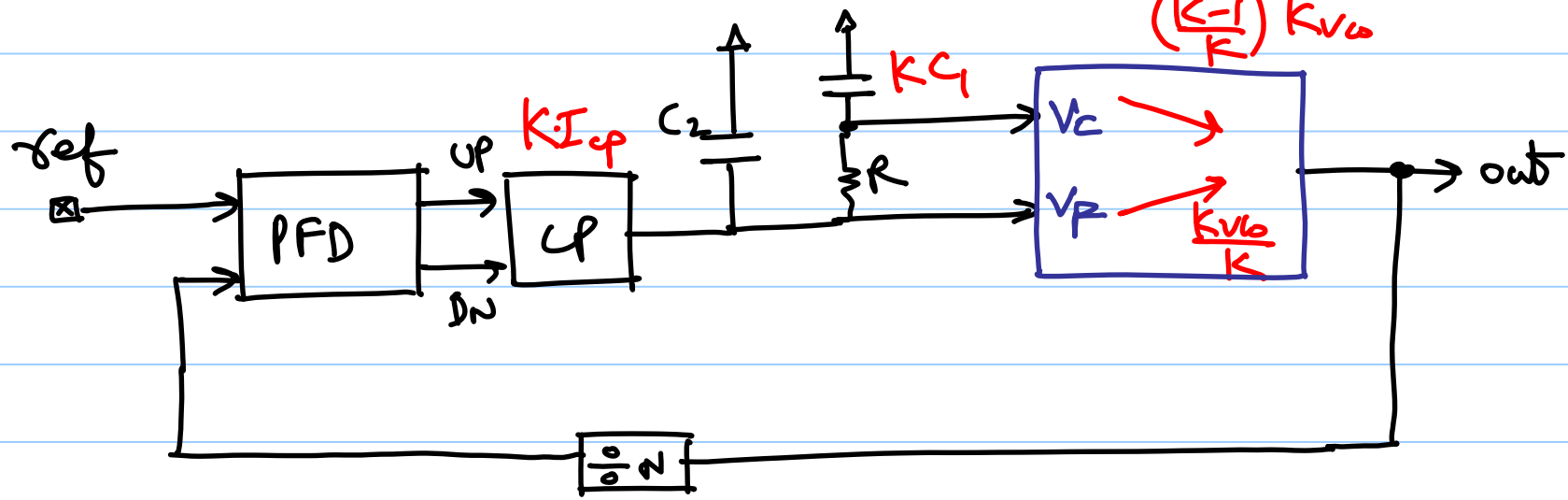
here $$F(s) = \frac{s+\frac{1}{RC_1}}{sC_2\left(s+\frac{1}{RC_1\|C_2}\right)}$$



$$LG(s) = \frac{I_{cp}}{2\pi N} \cdot \frac{K_{VCO}}{s^2} \frac{1}{(C_1 + C_2)} \cdot \left( \frac{1 + sRC_1/K}{1 + sR\frac{C_1 C_2}{C_1 + C_2}} \right)$$

$$\omega_z = \frac{1}{RC_1/K}, \quad \omega_{p1} = \omega_{p2} = 0, \quad \omega_{p3} = \frac{1}{R\, C_1 \| C_2}$$

* $\omega_z$ increases by the VCO gain reduction factor 'K'
  - ↳ Increase $C_1$ by K-times to retain the same $\omega_z$
    - ↳ the loop-gain drops
      - ↳ increase $I_{cp}$ to retain the same $\omega_{u,loop}$.

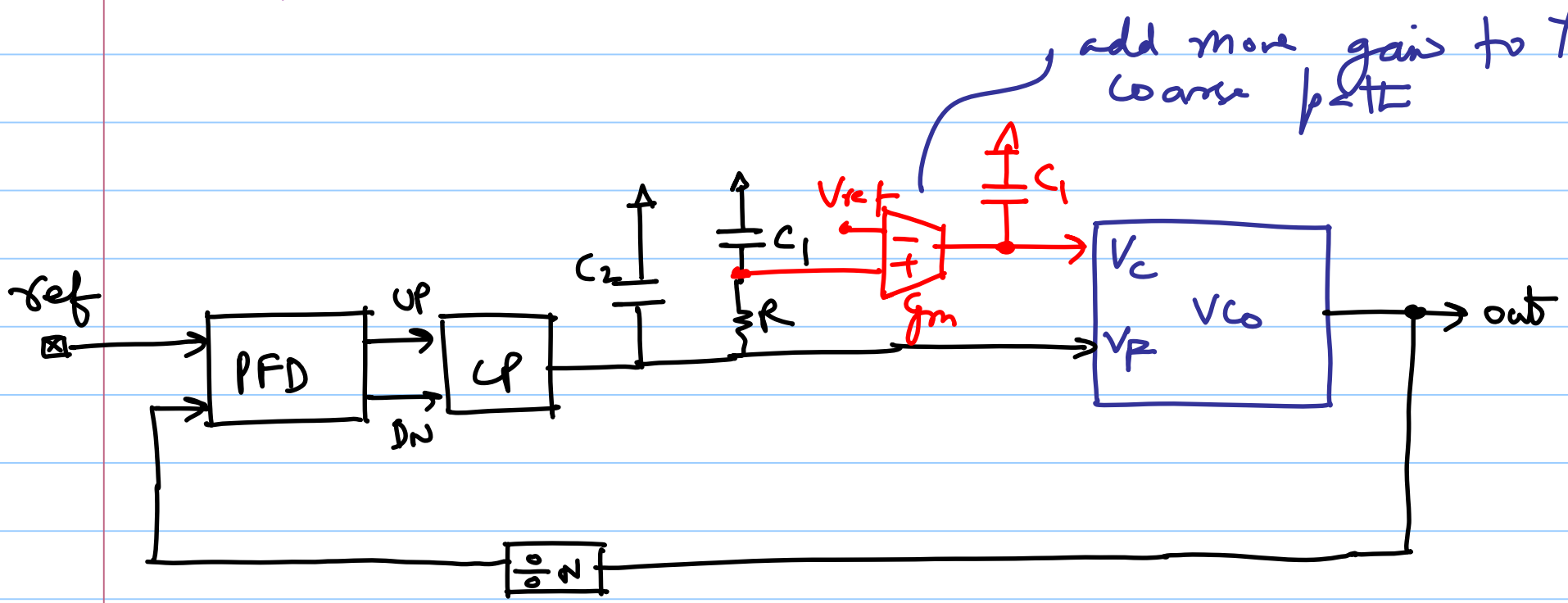



$$L(s) \simeq \frac{K \cdot I_{cp} K_{vco}}{2\pi N s^2} \frac{1}{(KC_1 + C_2)} \left( \frac{1 + sRC_1}{1 + sR\left(\frac{KC_1C_2}{KC_1 + C_2}\right)} \right)$$

$$\simeq \frac{I_{cp}}{2\pi N} \cdot \frac{K_{vco}}{s^2} \cdot \frac{1}{C_1} \left( \frac{1 + sRC_1}{1 + sR\left(\frac{KC_1C_2}{KC_1 + C_2}\right)} \right)$$

⇒ Split-tuned approach reduces the VCO gain by a factor of K at the expense of increasing the area by K-times.

# Improved split-tuned PLL

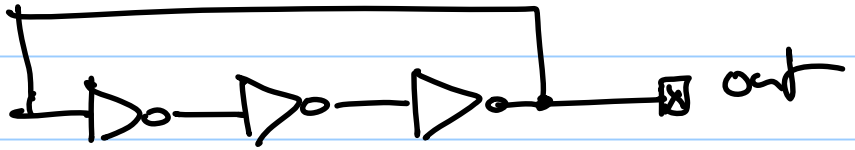


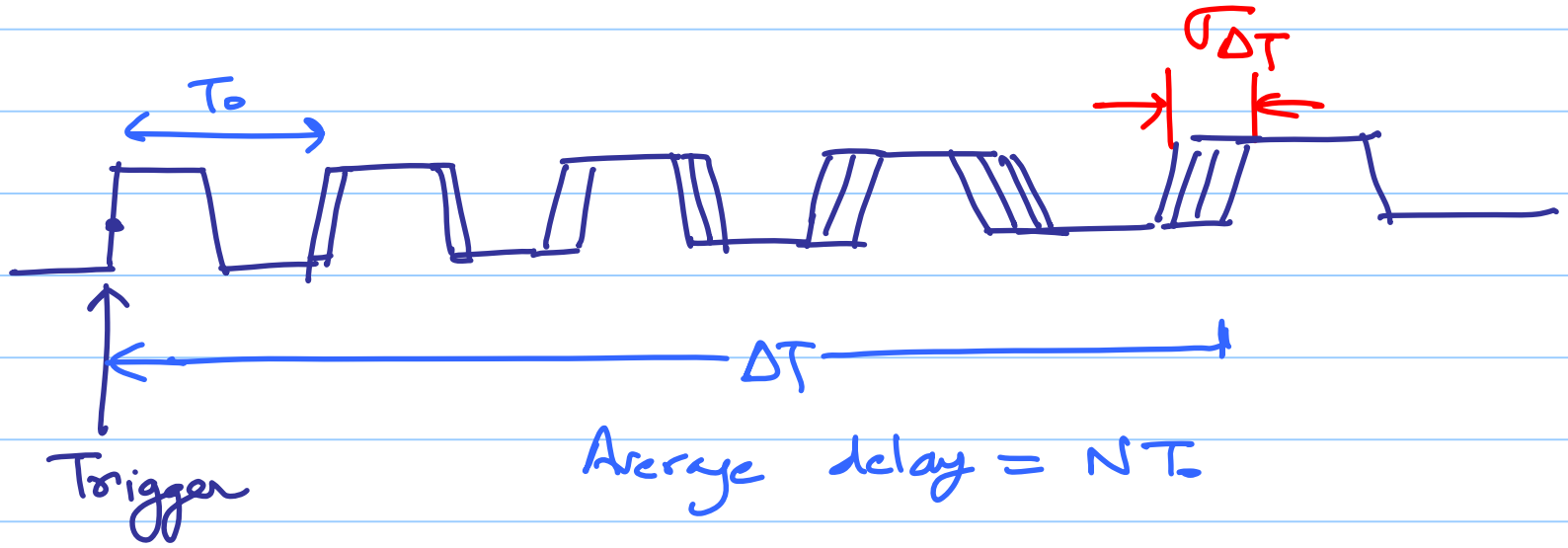

* leads to higher frequency tuning range

↳ Ensure that the two loops don't interact with each other.

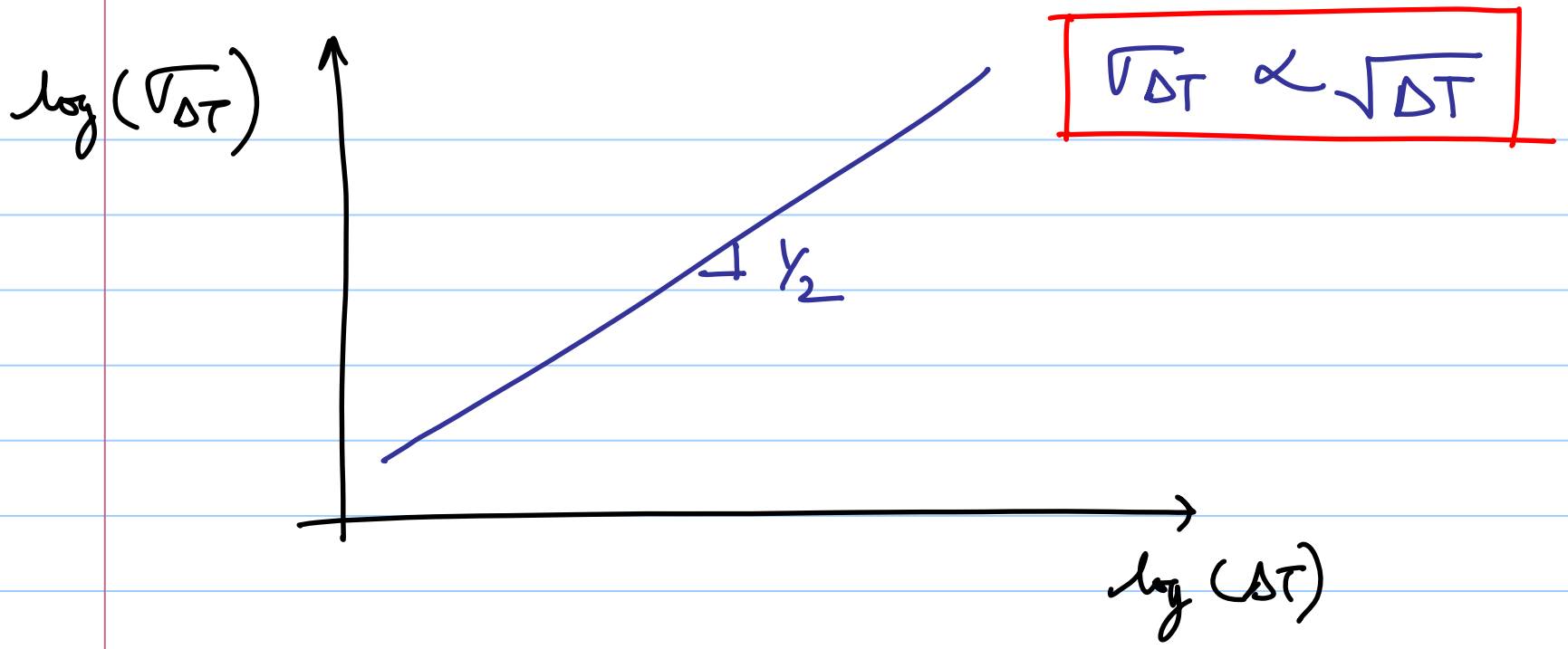
# Ring VCO Noise

ring oscillator
↳ free running ring-VCO




Average delay = $NT_0$




$$\sigma_{\Delta T} \propto \sqrt{\Delta T}$$

accumulated

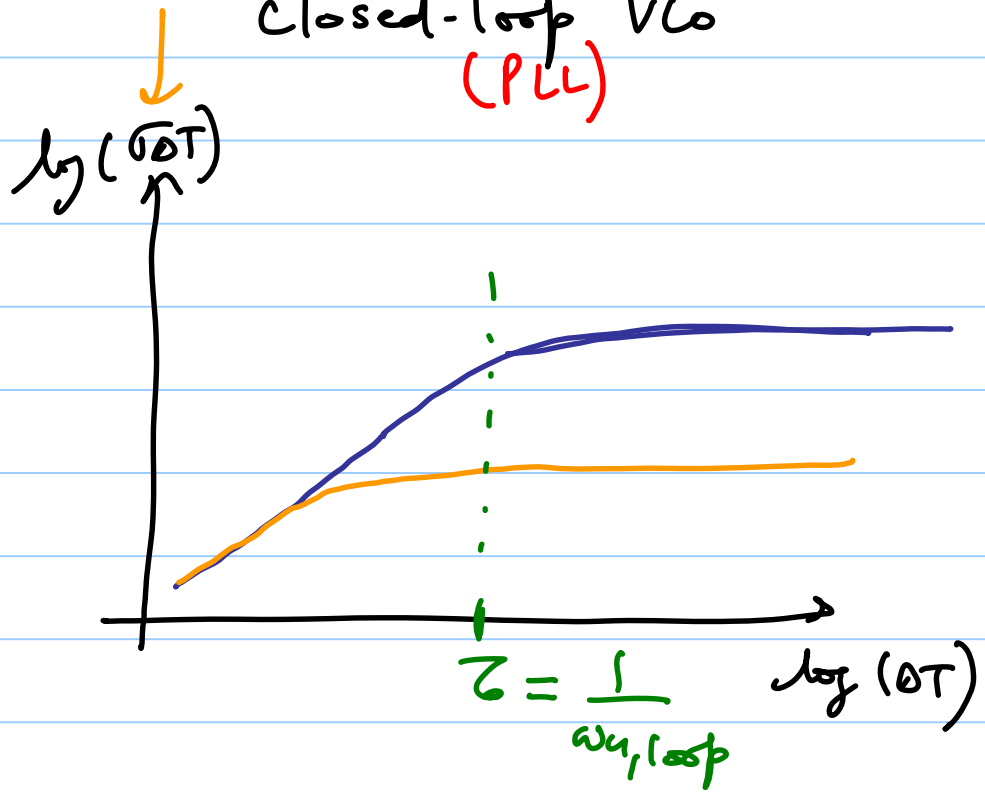
* Does this jitter depend on ring length?

↳ Depends on the edge transitions in $\Delta T$ period.

open-loop VCO
(ring oscillator)


Random Walk Process

closed-loop VCO
(PLL)



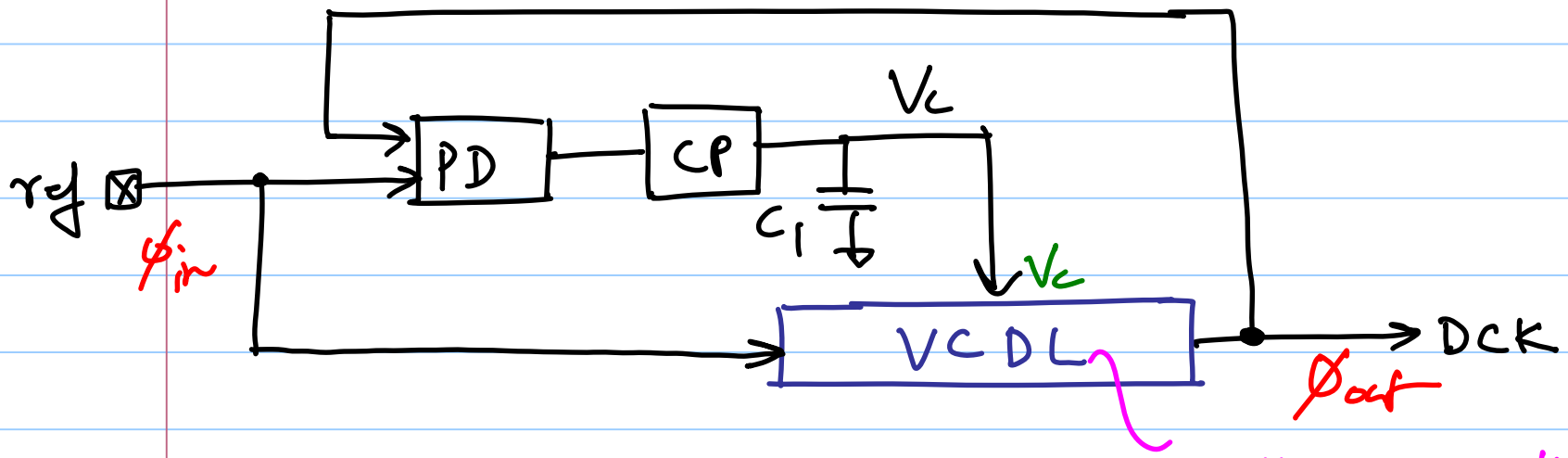
* jitter accumulation takes only upto $\tau = \frac{1}{\omega_{-3dB,loop}}$ after the jitter is suppressed

* we can't have $\omega_{-3dB,loop} \to \infty$

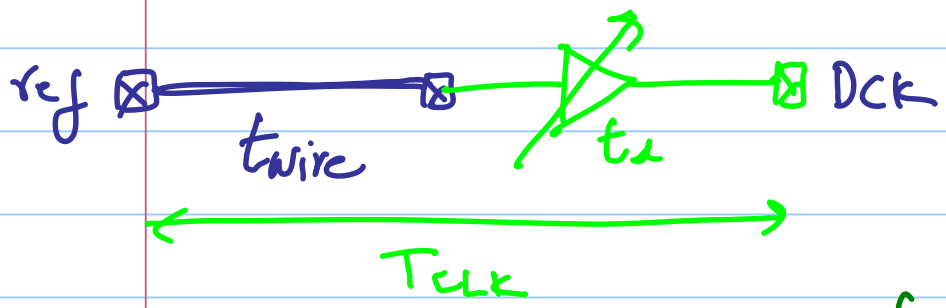
But $\omega_{-3dB,loop} < \frac{\omega_{ref}}{10}$ or $\omega_{ps}$

* Can we do better than a PLL in terms of jitter accumulation

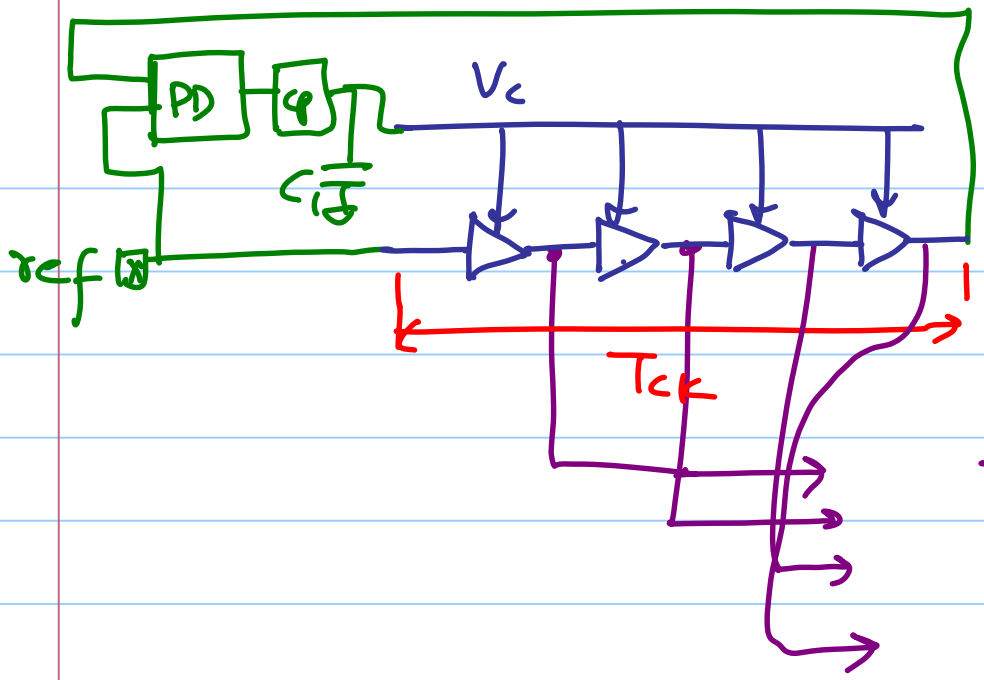
# Delay Locked Loop (DLL)



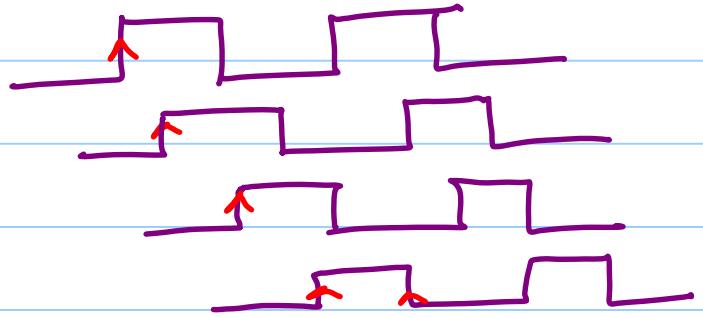

Voltage controlled delay line



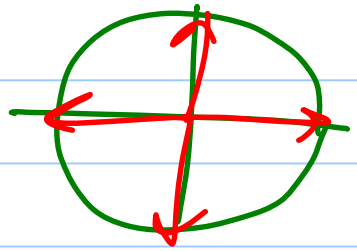

* reference is applied to both the PD as well as the VCDL



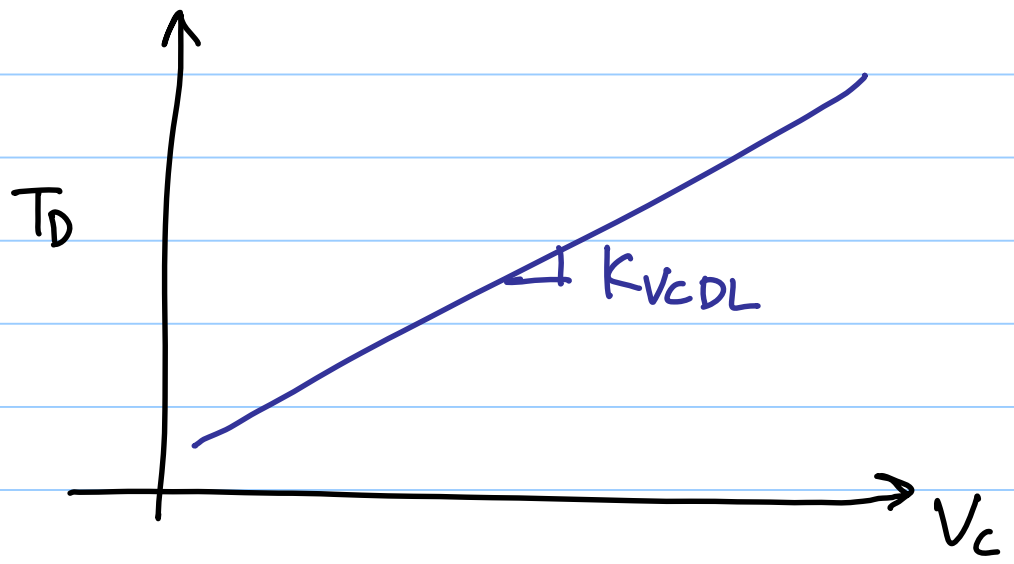

4-clock phases



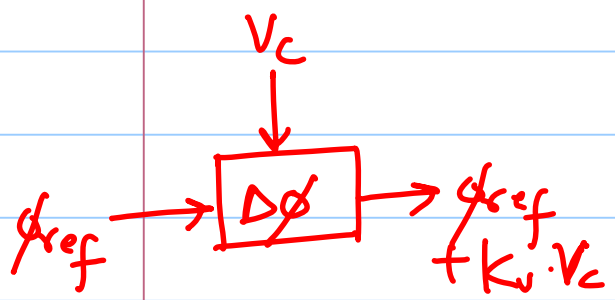
Quadrature phases



# VCDL

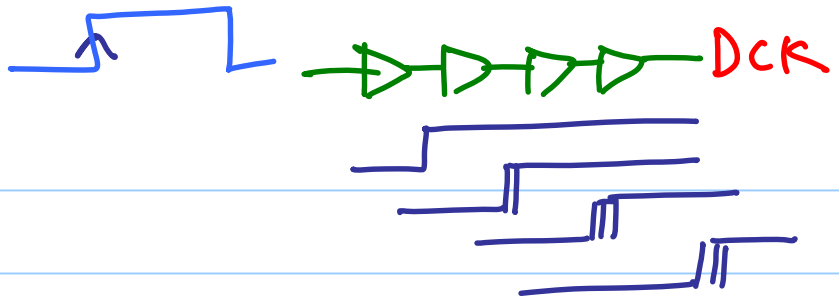



VCDL gain $K_{VCDL} = \frac{\Delta T_D}{\Delta V_c}$, $\left(\frac{Sec}{V}\right)$

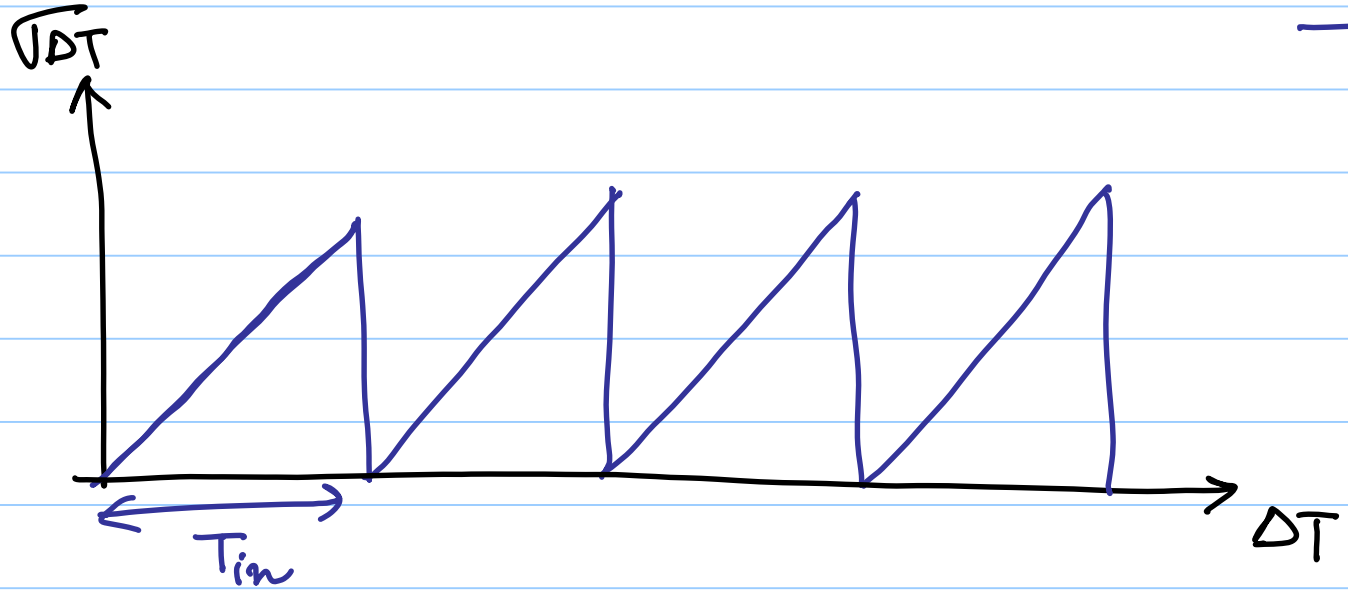



$= \frac{2\pi}{T_{ref}} \frac{\Delta T}{\Delta V_c}$ $\left(\frac{rad}{V}\right)$

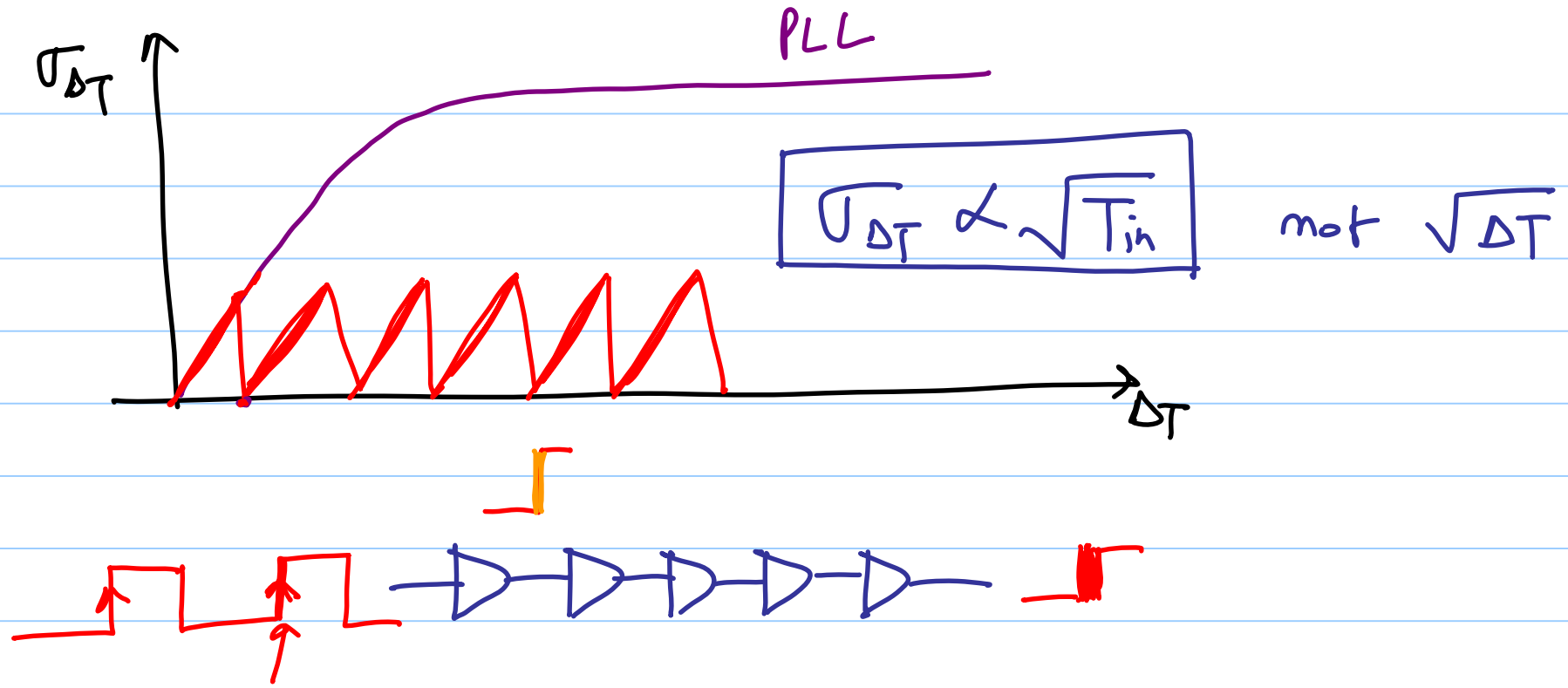
# VCDL Noise




@ DCK




* Jitter accumulates only for one input clock period
  - ↳ input clock resets jitter accumulation
  - ↳ VCDL noise is much smaller than the VCO phase noise


$\sigma_{\Delta T}$
PLL
$\sigma_{\Delta T} \propto \sqrt{T_{in}}$
not $\sqrt{\Delta T}$
$\Delta T$