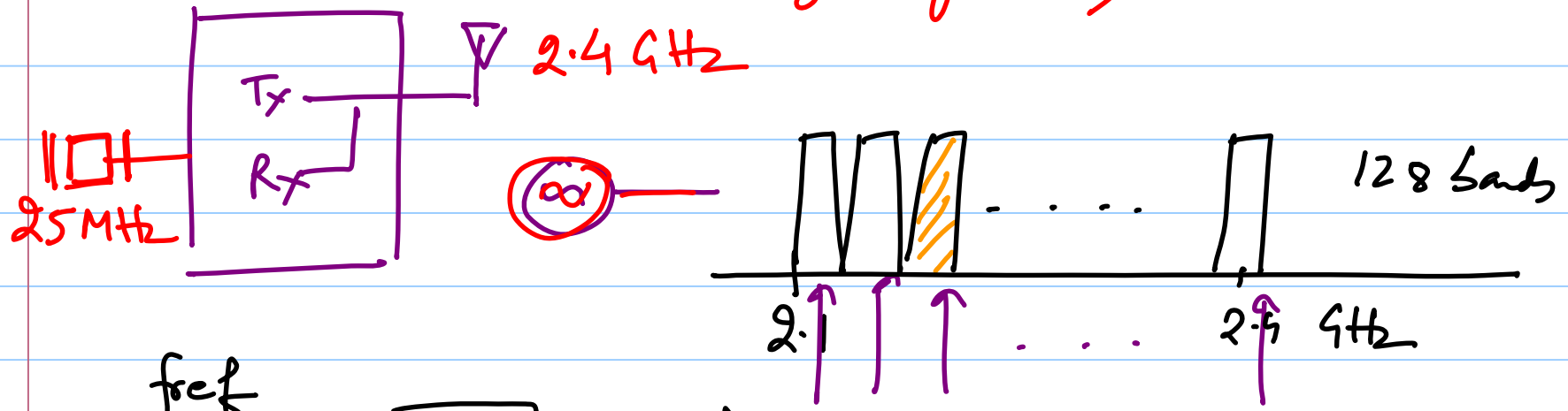
ECE 518 – Lecture 1

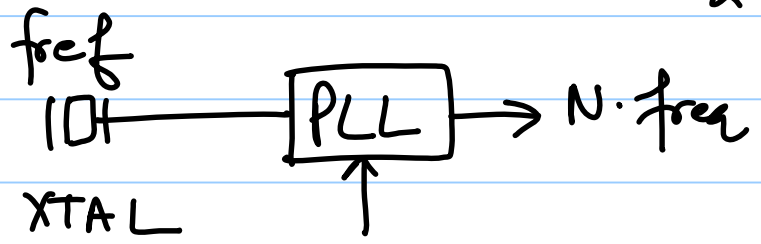
Note Title 1/13/2015

Phase-locked loops (PLLs)

↳ invented 80 years ago

① RF transceivers (frequency synthesis)





$$N = \frac{N_1}{N_2}$$

e.g. GSM 900–925 MHz
in steps of 30 kHz

② Digital systems

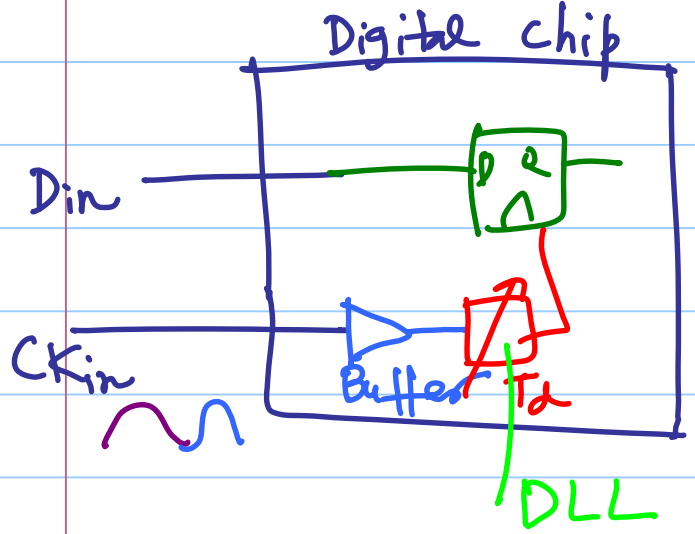
↳ CPU / DSP

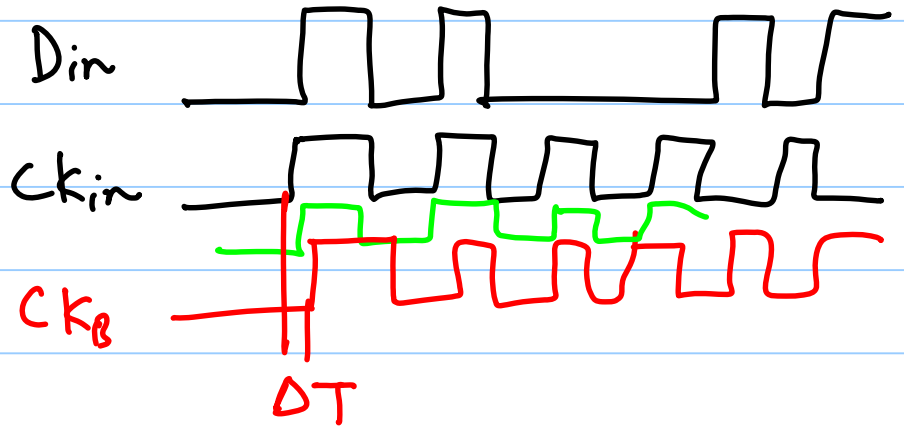
FPGA

memory, HDD, XBox (CPU),

Displays, ...

③ Skew reduction

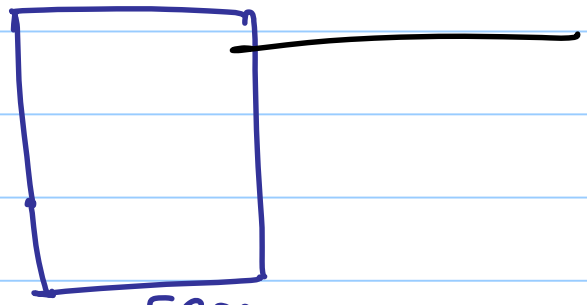




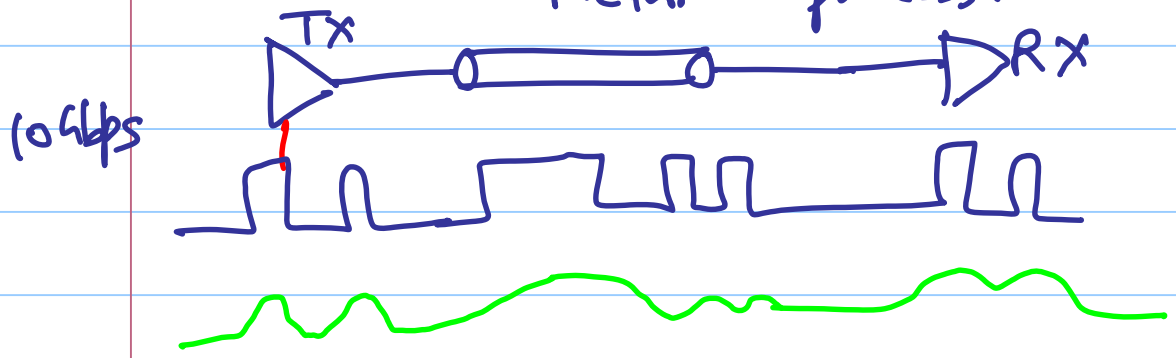
a PLL/DLL to align CK_B to CKin

④ Clock recovery

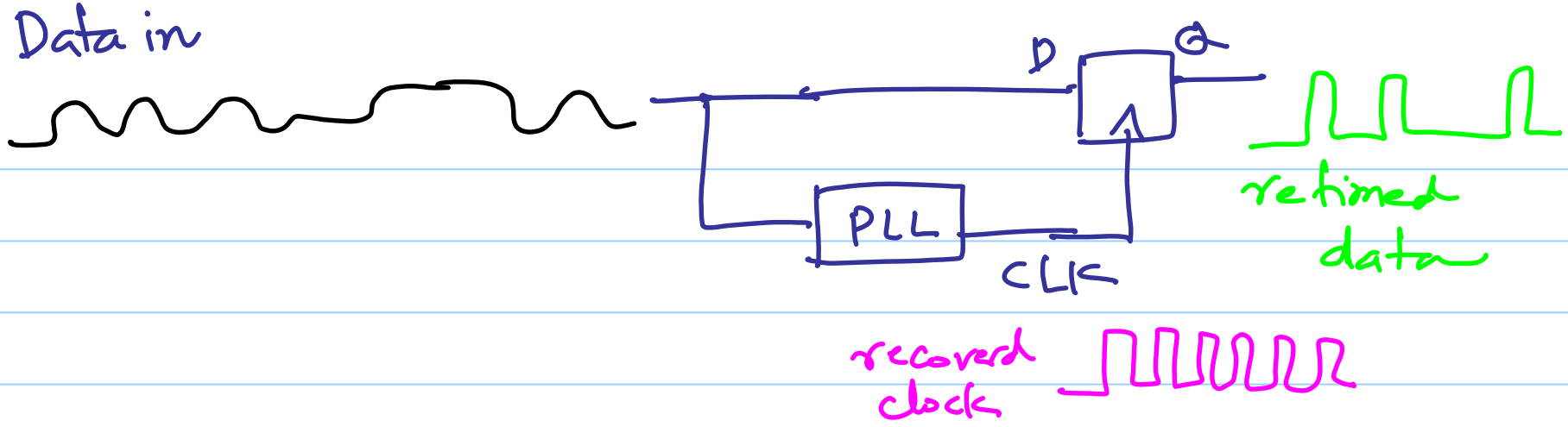
Serial Interface (10 – 32 Gbps)



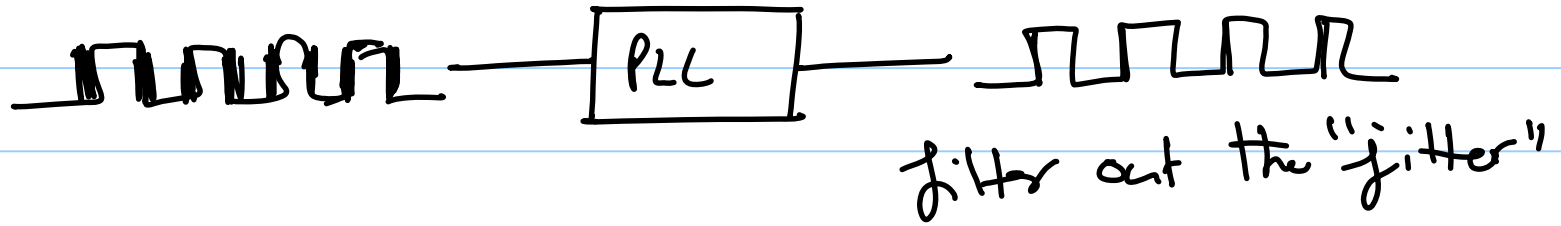
FPGA
Network processor



Clock & Data recovery (CDR)

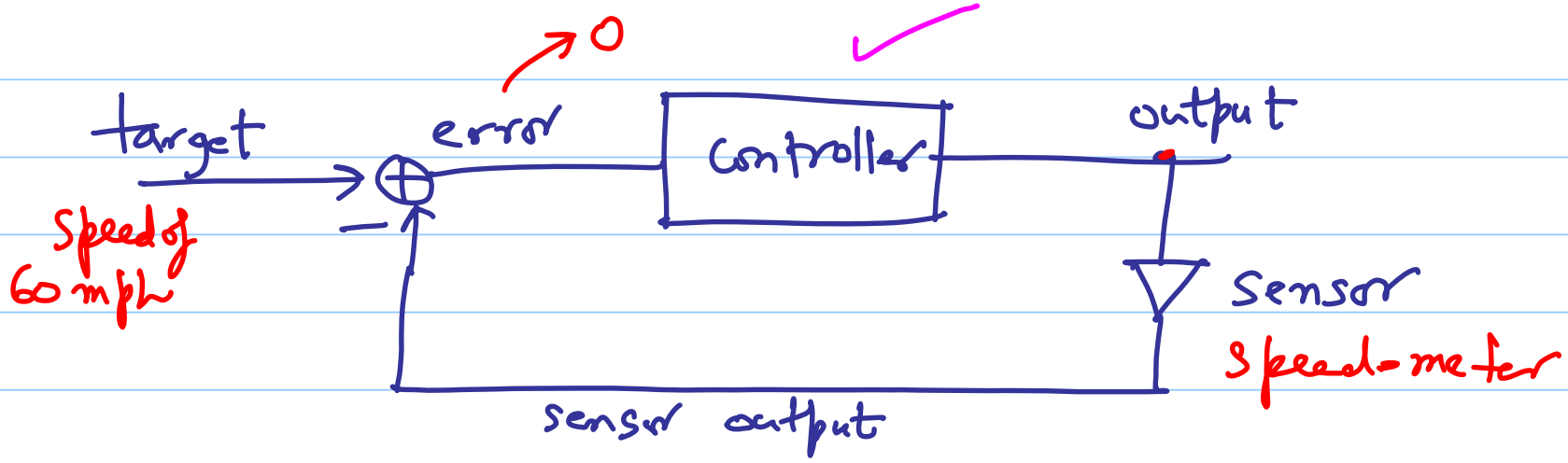


⑤ Jitter reduction



⑥ "FM demodulation"

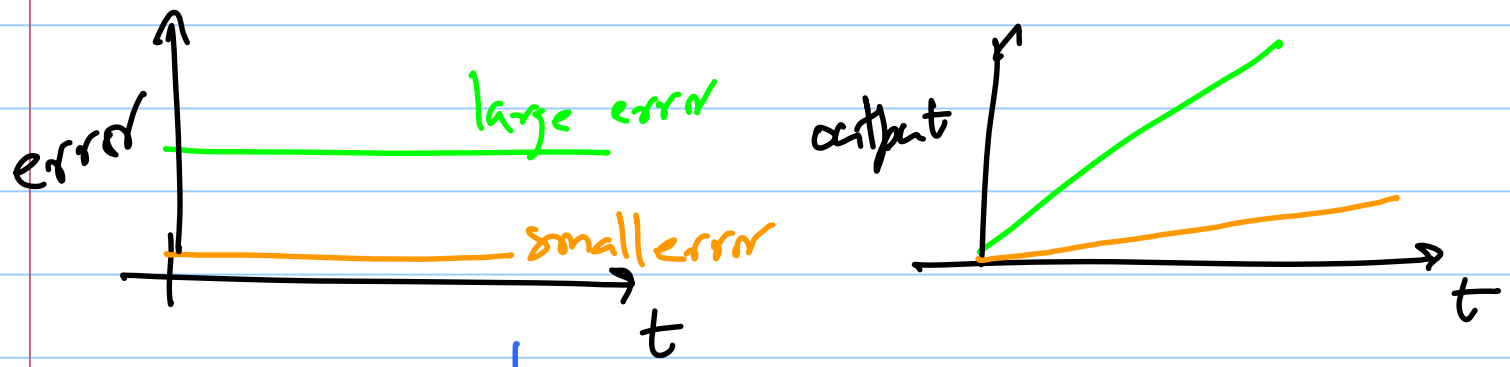
Negative feedback loops :



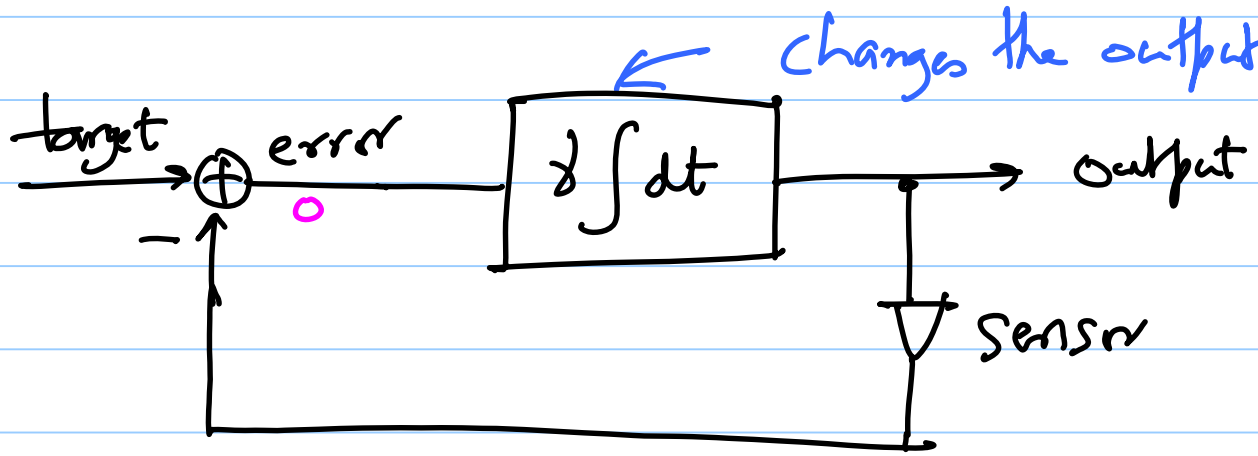
the system senses the output, compares to a desired value, and then drives the output towards the desired value

↳ error → constant

* what is the nature of the controller?



↳ an integrator is used as a controller

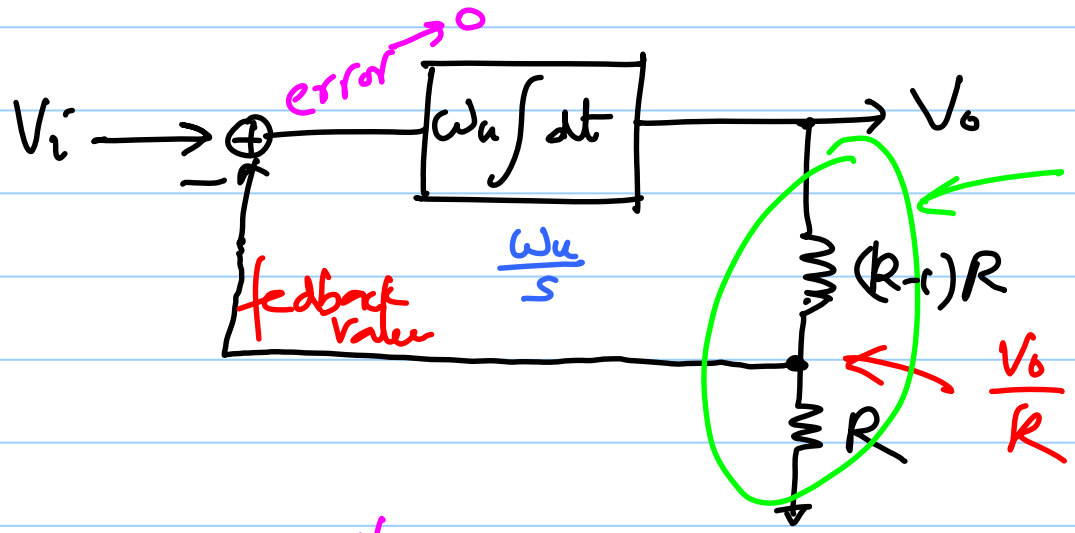


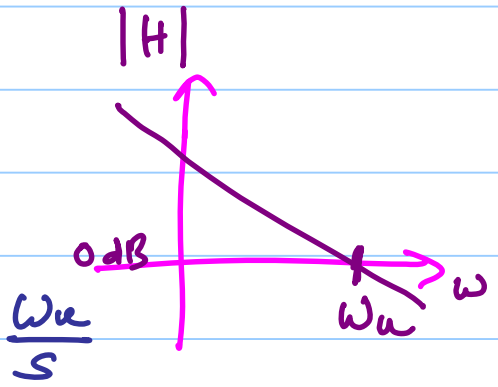
← changes the output until the error goes to zero

Example: Negative feedback amplifier

↓ gain

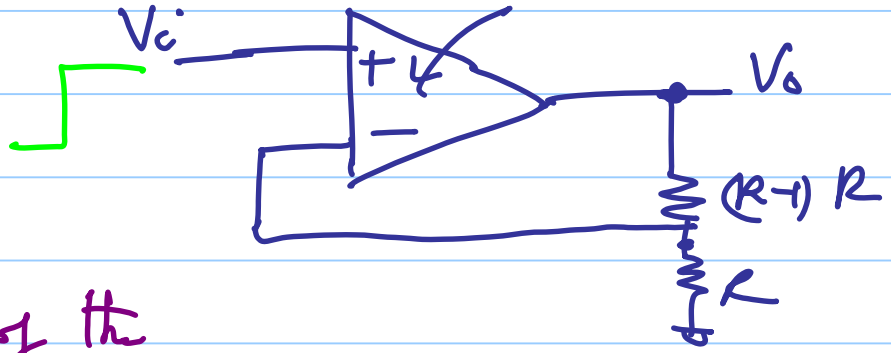
$V_o = k \cdot V_i$





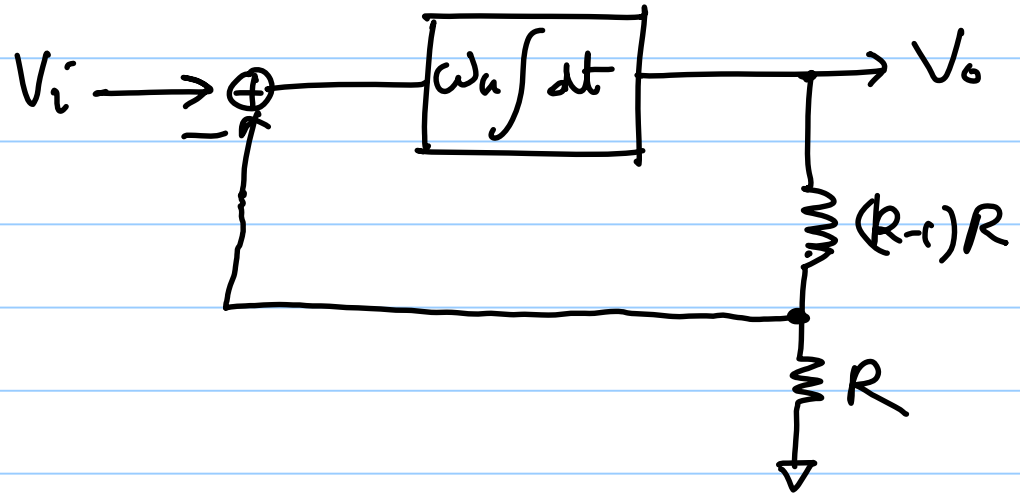
$\frac{V_o}{R} \to V_i$

$\Rightarrow V_o \to kV_i$

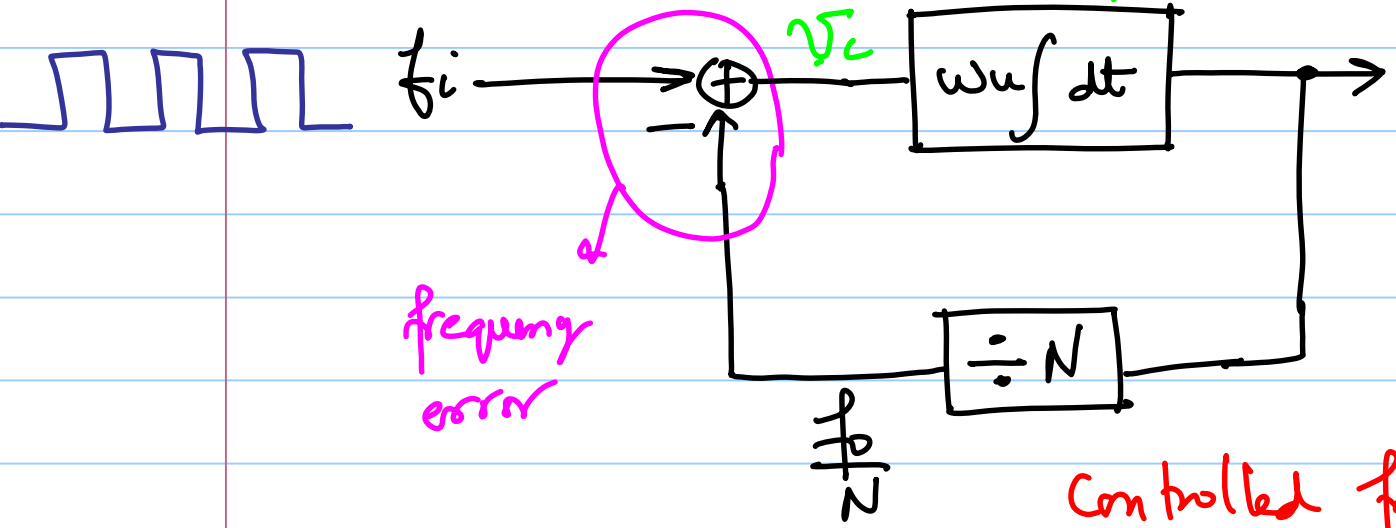


$\omega_u \to$ unity-gain frequency of the integrator

Gain = k

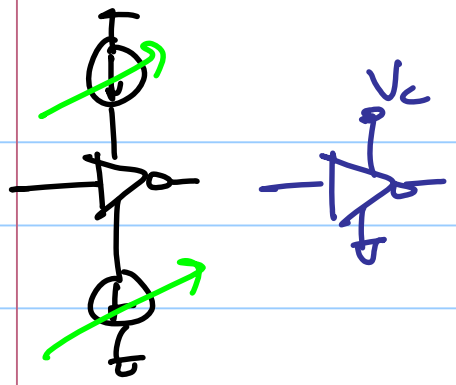


controlled frequency source



$f_o \rightarrow N f_i$

Controlled frequency source
↳ Vary output frequency using an electrical signal



↳ VCO

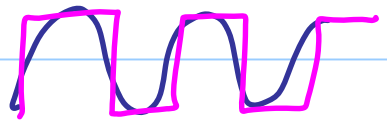
(voltage controlled oscillators)

Voltage Controlled oscillator

Bias point

small voltage

$V_{co} + v_c$



$f_0 + K_{vco} \cdot v_c$

f_0: free running frequency

K_{vco}: VCO gain $\left(\frac{Hz}{V}\right)$

output $\rightarrow$ $A \cos(2\pi f_0 t + 2\pi K_{vco} \cdot v_c \cdot t)$

ϕ

v_c

In reality, the phase is continuous

$$A \cos\left(2\pi f_0 t + 2\pi K_{vco} \int_0^t v_c(t)\, dt\right)$$

VCO phase

V_{ctrl} v_c