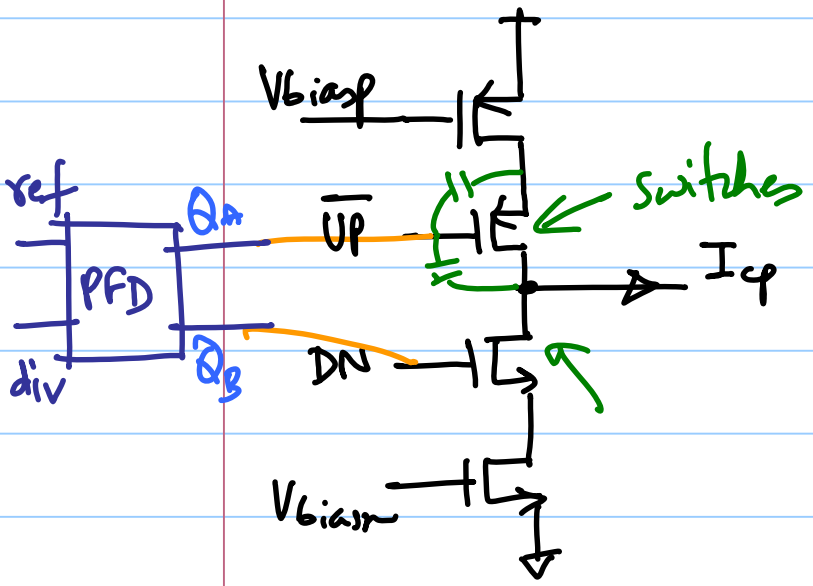
ECE 518 - Lecture 11

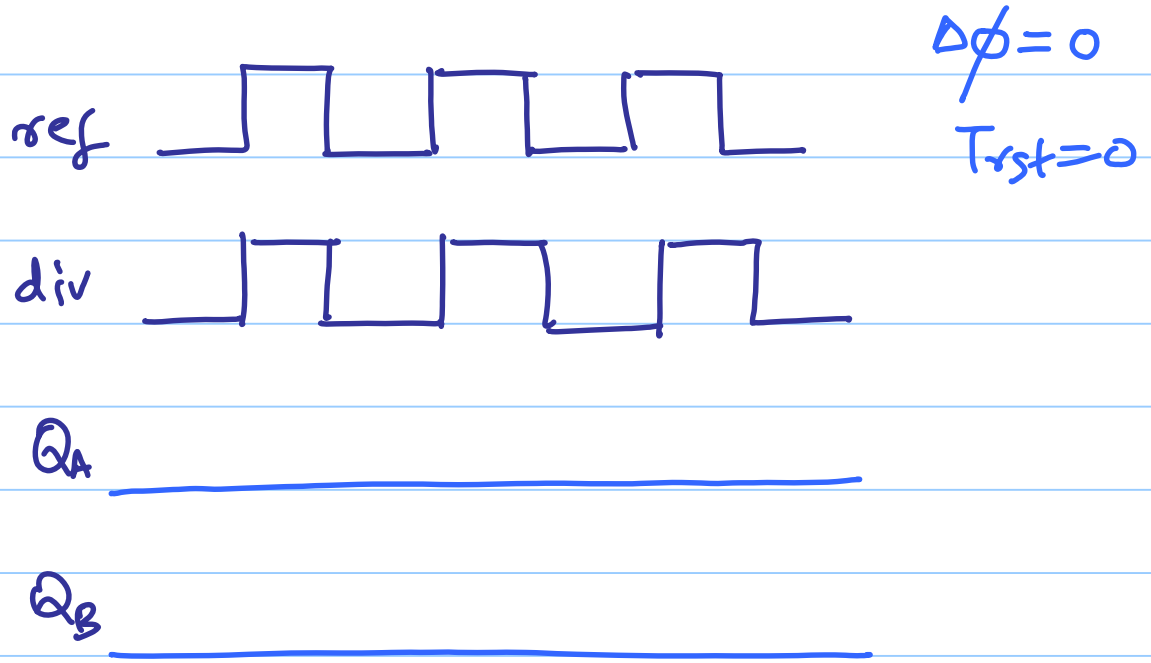
Note Title 2/19/2015

No lecture on Tuesday, 2/24

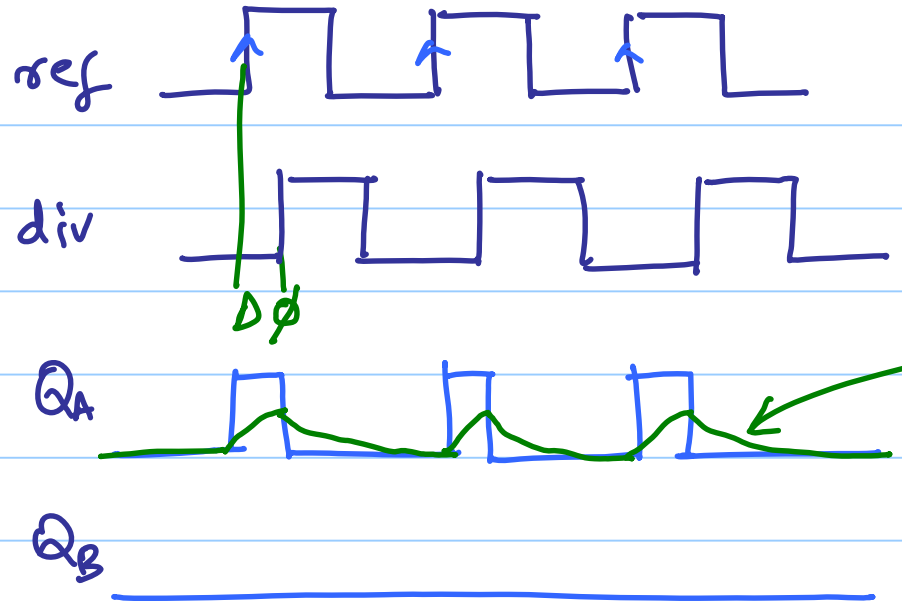
Watch online video instead

① PFD dead zone

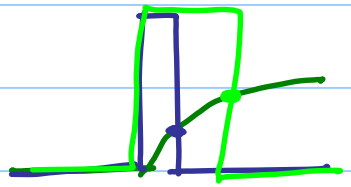




$\Delta\phi > 0$, $T_{rst} = 0$

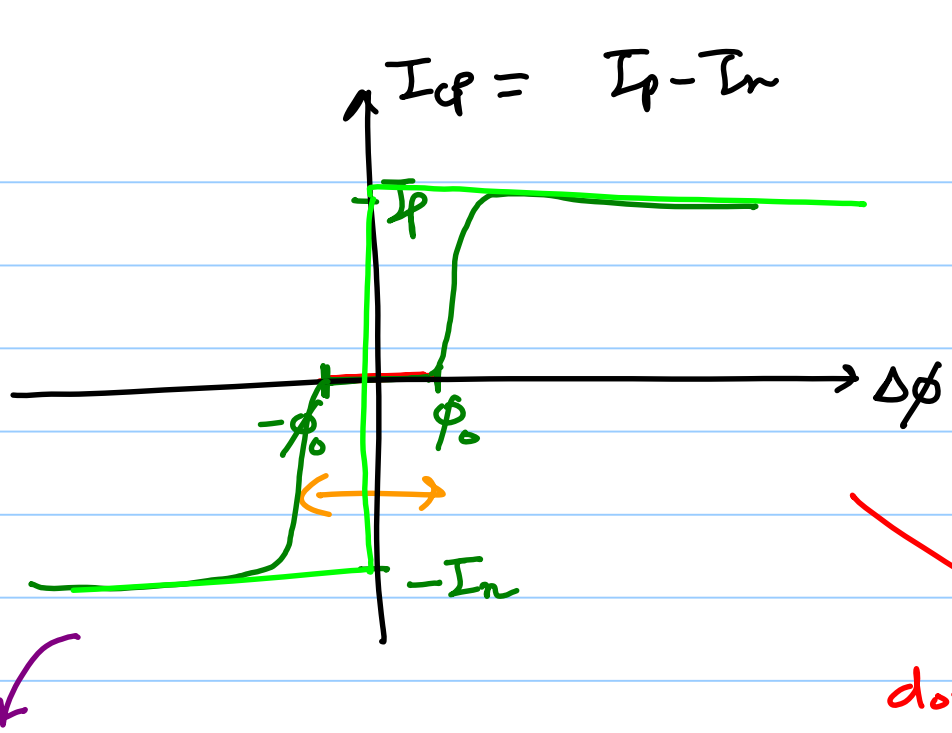


due to finite RC time constant in driving the switches

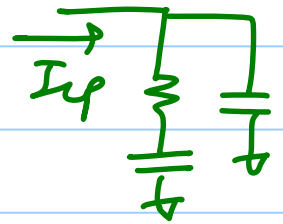


* for some small $|\Delta\phi| > 0$, the charge pump switches fail to turn on

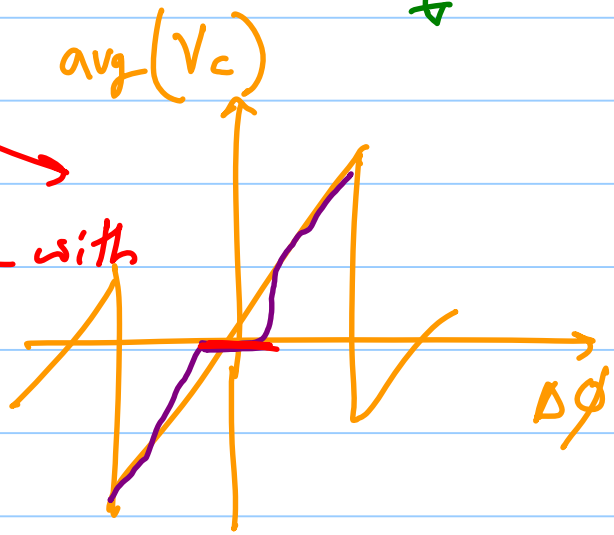
$\Rightarrow I_{cp} = I_p - I_n = 0$ for some $|\Delta\phi| < \phi_0$



I_{cp} is the current supplied to the loop-filter



don't confuse with this

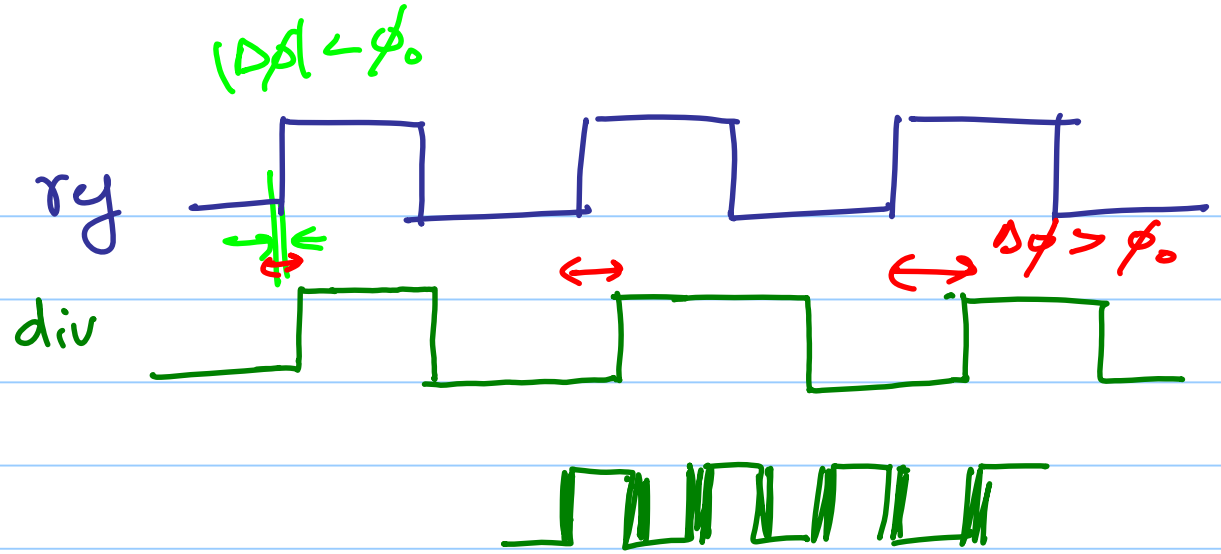


$\Rightarrow$ I_{cp} is no longer a function of $\Delta\phi$

$\Rightarrow$ loop gain drops to zero

$\hookrightarrow$ output phase is not locked

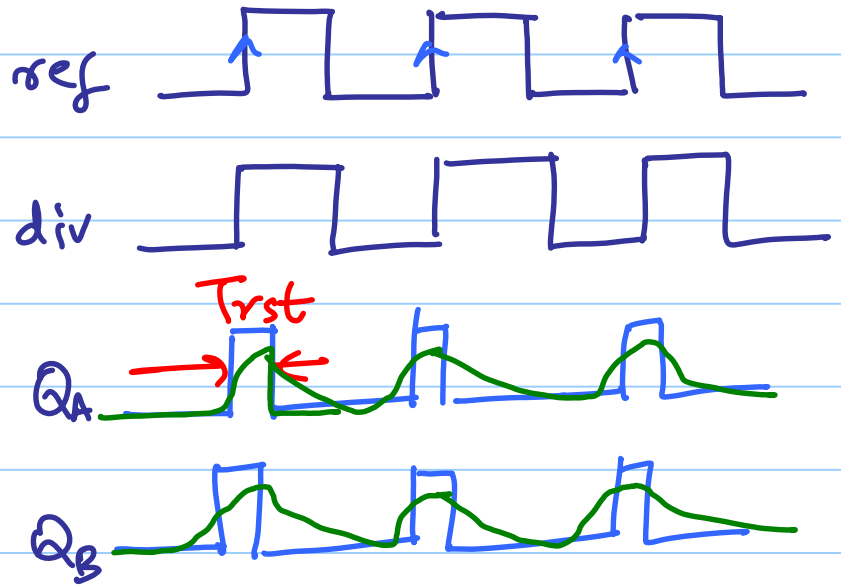
$\Rightarrow$ PFD/CP suffers from a "dead zone" around zero $\Delta\phi$ and is equal to $\pm\phi_0$



* dead zone allows the VCO to accumulate as much phase error as ϕ_0 as there is no corrective feedback
  - ↳ random phase accumulation ⇒ jitter

finite reset time in the PFD,

↳ coincident pulses on Q_A & Q_B to eliminate the dead zone

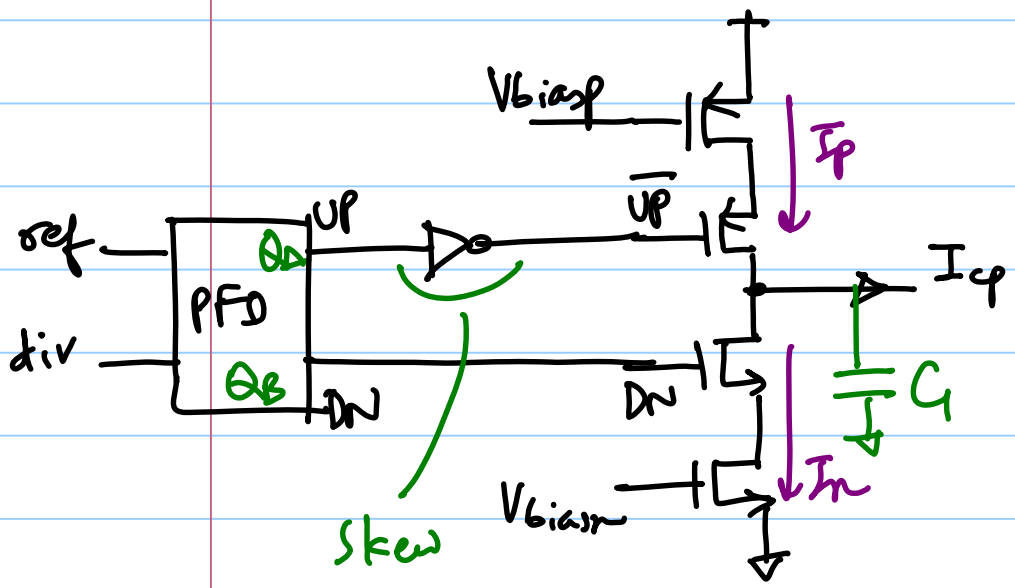


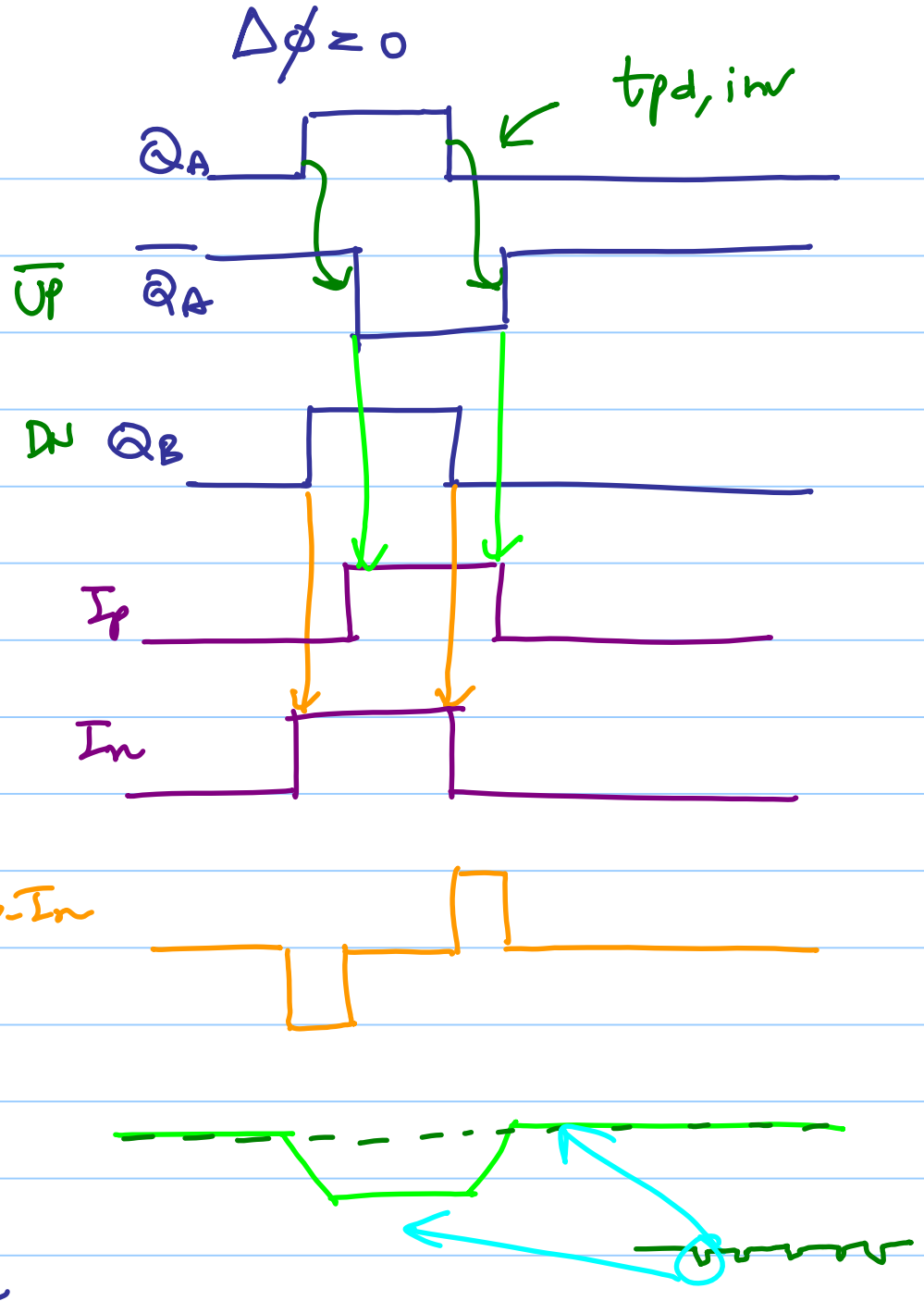
⇒ Trst must turn the CP switches ON

→ Q_A & Q_B pulses always turn the CP on if they are sufficiently wide ∈ Trst

↳ dead zone vanishes if Trst is long enough to allow Q_A & Q_B to reach a valid logic level and turn on the CP switches

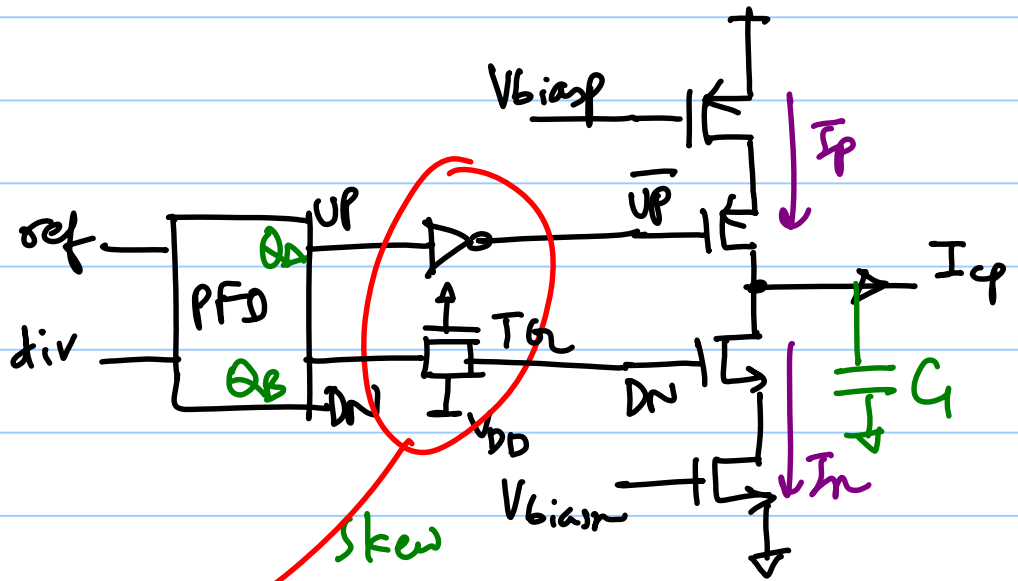
② UP/DN skew





⇒ more periodic disturbance

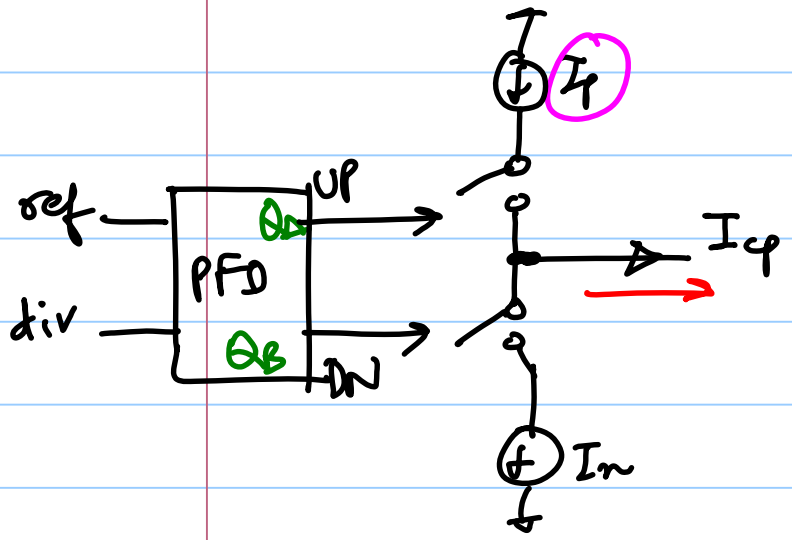
* match the UP & DN paths

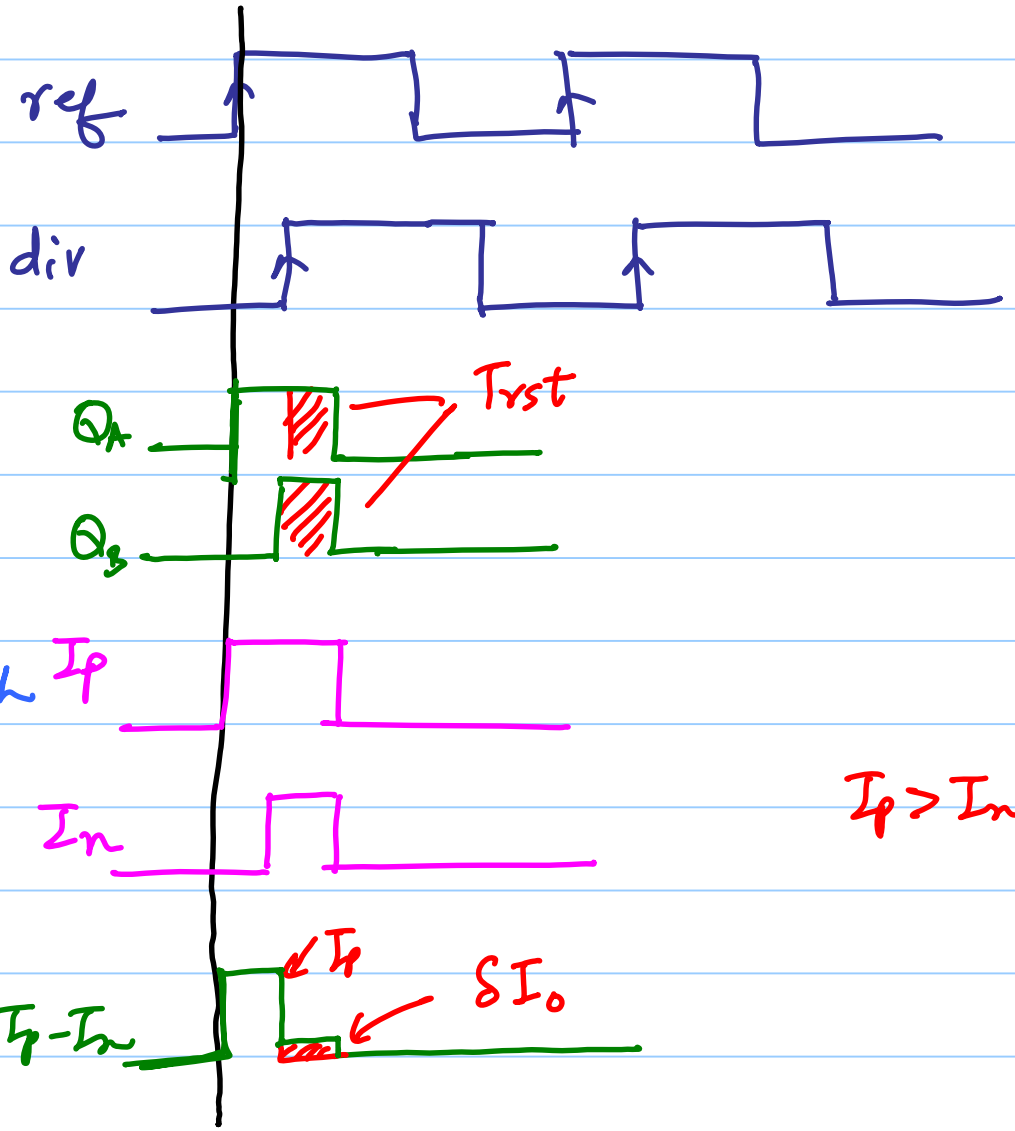


Equalize the delays

③ I_p & I_n mismatch

"Open-loop understanding"



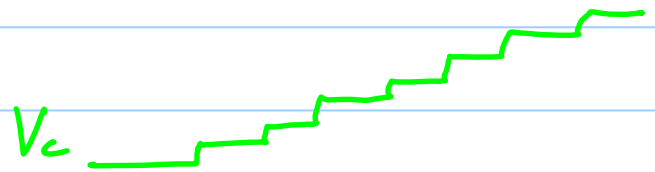


current flows into the LF due to the I_p & I_n mismatch during the reset time

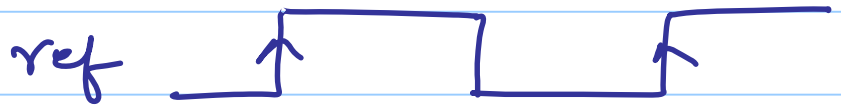
$T_{rst} > 0$

& $I_p - I_n = \delta I_o$

even if $\Delta\phi = 0$, δI_o will flow into the LF during Trst time

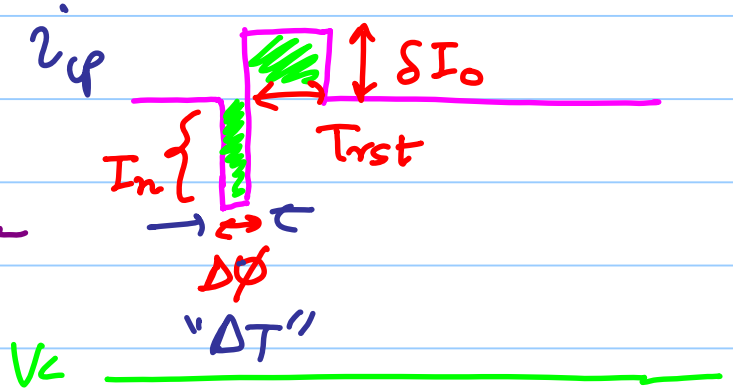


Now, in the steady-state (i.e. closed-loop)



$$\delta Q = T_{rst} \cdot \delta I_o = \Delta T \cdot I_{in}$$

steady-state fixed offset created to counterbalance the impact of δI_o



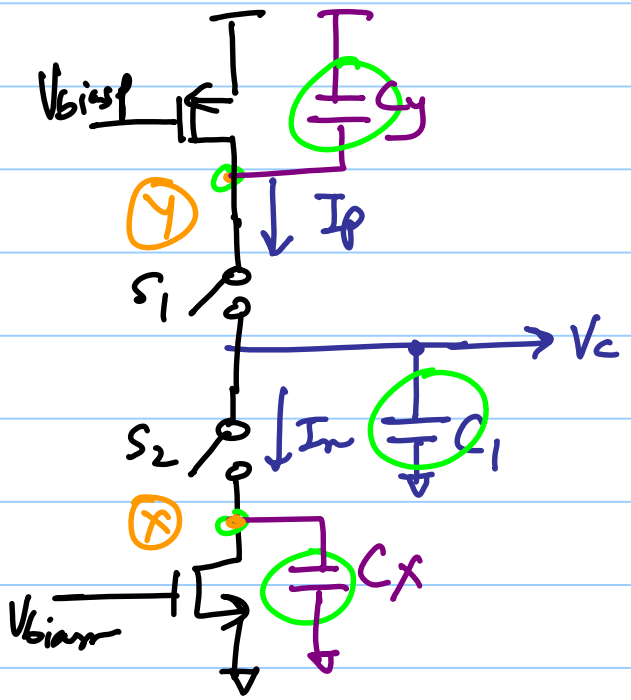
$$\Delta T = T_{rst} \cdot \left(\frac{\delta I_o}{I_{in}}\right)$$

$$\Delta T \triangleq T_{rst} \cdot \left(\frac{\Delta I_{cp}}{I_{cp}} \right)$$

Corresponding phase offset

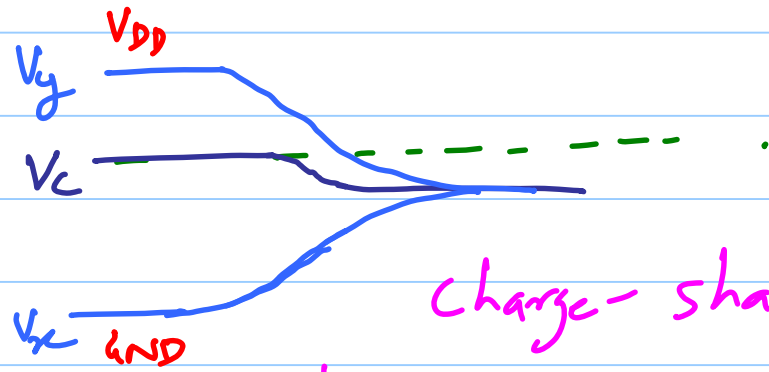
$$\Delta\phi = 2\pi \frac{\Delta T}{T} = \boxed{2\pi \cdot \frac{T_{rst}}{T} \left(\frac{\Delta I_{cp}}{I_{cp}} \right)}$$

④ Charge sharing in the CP



* initially S_1 & S_2 are off
  - ↳ node X → 0 (NMOS CM shuts off)
  - ↳ node Y → V_{DD}

* $\Delta\phi = 0$ ⇒ S_1 & S_2 turn on



Charge-sharing occurs b/w C_x, C_y & C_1

Let's say for $\Delta\phi = 0$ ⇒ V_c should be kept constant

$V_c \rightarrow f_{VCO}$

But b'coz of charge sharing

$$V_{y\,final} = \frac{C_x V_x + C_y V_y + C_l V_c}{C_x + C_y + C_l}$$

$$= \frac{C_y \cdot V_{DD} + C_l V_c}{C_x + C_y + C_l}$$

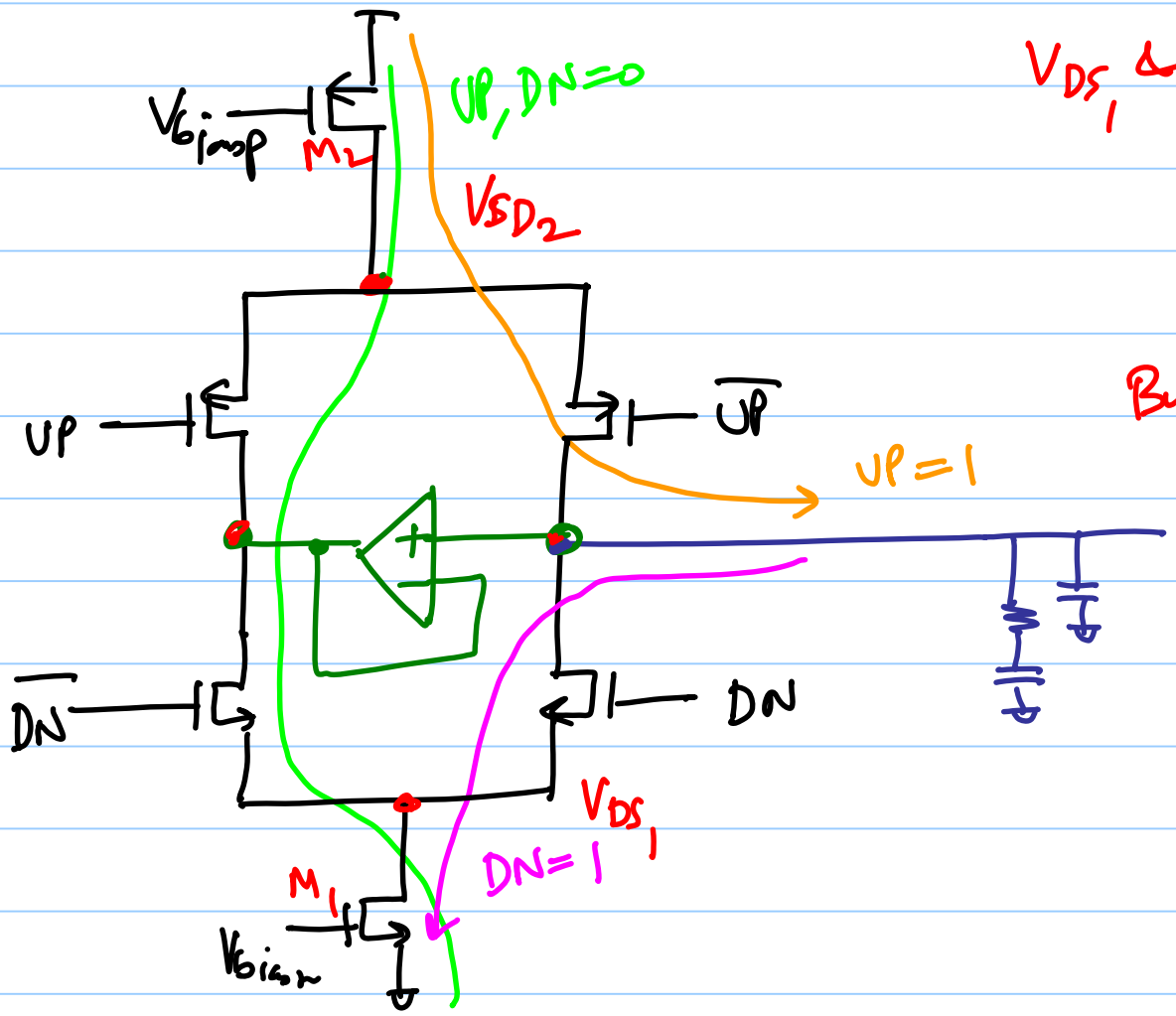
$\Rightarrow$ V_c 'jumps" $\Rightarrow$ VCO phase error $\Rightarrow$ jitter

$\Rightarrow$ This disturbance depends upon the value of V_c

$\Rightarrow$ % jitter depends upon Xtal of the PLL

$\Rightarrow$ charge sharing

Solution: keep the current sources turned ON and simply steer the current



V_{DS_1} & V_{SD_2} should not vary during Switching

Buffer Amp also ensures that Ip & In are always ON