Homework 3

ECE 5/418 – PLL and Memory IC Design

Note: Use Cadence schematic capture and Spectre simulation tools, available on the AMS servers for the homework problems. Use TSMC 180nm models with $V_{DD} = 1.8\,V$.

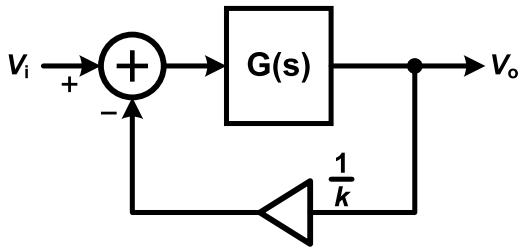
Problem 1- PFD Design

Design a transistor-level implementation of a PFD working at $f_{ref} = 100\,MHz$ with a minimum PFD output pulse width of at least $100\,ps$.

1. Show the transistor-level schematic and simulations showing the minimum PFD pulse width specification is satisfied.
2. Plot the phase transfer characteristic over a phase range of $\pm 4\pi$ (*Use your test-bench from the last HW*).

Problem 2- Feedback System Stability

A feedback system representative of a PLL is shown below, where $G(s)$ is the forward-path transfer function and the feedback gain is given by $H(s) = \frac{1}{k}$.



1. For each the following systems, plot- (i) loop-response (magnitude and phase), (ii) closed-loop response, and (iii) closed-loop transient step-response. Also, label the parameters $\omega_{u,loop}$, ω_{3dB}, phase and gain margins (PM and GM), closed-loop DC gain (A_{CL}).
   (a) $G(s) = \frac{10^3}{s}$, $k = 1,\ 10$ (*Type-I system*)
   (b) $G(s) = \frac{10^3}{\left(1+\frac{s}{10^3}\right)\left(1+\frac{s}{10^4}\right)}$, $k = 1,\ 10$ (*two close poles*)
   (c) $G(s) = \frac{10^3}{\left(1+\frac{s}{10^3}\right)\left(1+\frac{s}{10^6}\right)}$, $k = 1,\ 10$ (*two separated poles*)
   (d) $G(s) = \frac{5\times 10^8}{s^2}$, $k = 1,\ 10$ (Type-II system)
   (e) $G(s) = \frac{5\times 10^8\left(1+\frac{s}{10^3}\right)}{s^2}$, $k = 1,\ 10$ (Type-II system with a zero)
   (f) $G(s) = \frac{5\times 10^8\left(1+\frac{s}{10^3}\right)}{s^2\left(1+\frac{s}{10^6}\right)}$, $k = 1,\ 10$ (Type-II system with a zero and a pole)
2. Comment on the stability of the above systems in a closed loop. Do you observe any relation between the PM and the settling response?

PS: Make sure you spend some effort in arranging and illustrating the plots. Just throwing the plots around the document is not acceptable.