Revision History

Ver. #	Rev. Date	Rev. By	Comment
0.0	3/18/2012	Kehan Zhu	Initial draft
1.0	4/05/2012	Kehan Zhu	Add PLL phase noise
2.0	4/13/2012	Kehan Zhu	Re-design VCO
3.0	4/15/2012	Kehan Zhu	Freeze design and write report

Type-II 3rd-order Charge-Pump PLL Design

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1 Design Description

Type-II 3rd-order PLL is one of the most popular PLL topologies used nowadays due to the advantages over lower type or lower order PLL topologies for the following reasons:

- Type-I PLL has very limited tuning range, the PFD has to provide some phase difference at steady- state so that periodic spurs intrinsically modulates VCO.
- Type-II 2nd-order PLL is not good enough to immune reference clock feed-through due to the $-20\ dB/dec$ slope after loop bandwidth.

1.1 Spec. and Requirement

In this project, I am going to design a Type-II 3rd-order PLL according to the basic specifications listed in Table 1.

Table 1 PLL design specifications.

Parameter	Specified value
Technology	IBM 130-nm CMOS
Nominal Supply voltage	1.2V
Operating frequency (fout)	100 MHz - 500 MHz
Fixed feedback divider (N)	16
Reference clock	6.25 MHz – 31.25 MHz
Power consumption	Minimum
Absolute rms jitter	0.2% of the period

2 System Design Analysis

Bandwidth, zero and pole placement and loop filter parameters will be derived in this section. Noise transfer function is also studied.

2.1 System Parameters

As pervious mentioned Type-II 2nd-order PLL has not enough reference feed-through rejection, so by adding C_2, we introduce another pole after $\omega_{u,loop}$ to reduce reference feedthrough and decrease the spurious sidebands at harmonics of the reference frequency. Actually, Type-II 2nd-order PLL is not existing in reality due to the parasitic capacitance seen at the input of the VCO even without placing the explicit capacitor C_2.

The loop transfer function ($L(s)$) of Type-II 3rd-order PLL is

$$L(s) = \frac{I_{CP}}{2\pi} \cdot \left[\left(R_1 + \frac{1}{sC_1}\right) || \frac{1}{sC_2}\right] \cdot \frac{2\pi K_{VCO}}{s} \cdot \frac{1}{N} = \frac{I_{CP} K_{VCO}}{(C_1 + C_2)N} \cdot \frac{1 + \frac{s}{\omega_z}}{s^2\left(1 + \frac{s}{\omega_p}\right)}$$

$$\omega_z = \frac{1}{R_1 C_1} \quad \text{and} \quad \omega_p = \frac{C_1 + C_2}{R_1 C_1 C_2}$$

The unit of K_{VCO} is defined as Hz/V instead of rad/V in this work. Let $b = \frac{C_1}{C_2}$, $\omega_p = \frac{b+1}{R_1 C_1} =$

$(b+1)\omega_z$. As illustrated in Figure 1, $\omega_z < \omega_{u,loop} < \omega_p < \omega_{ref}$.

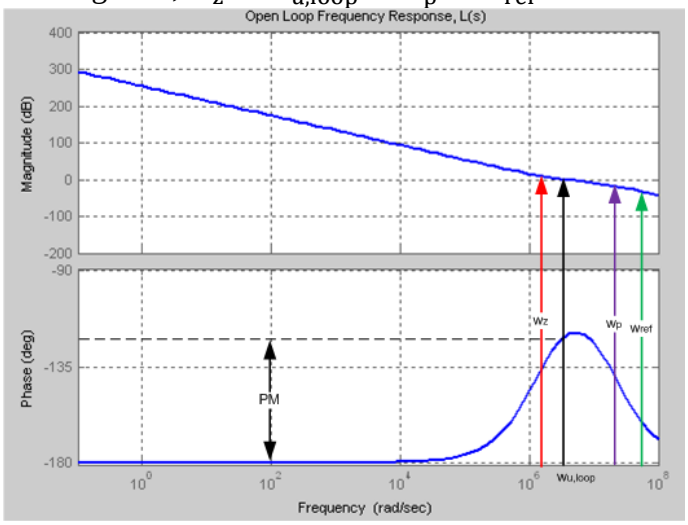


Figure 1 PLL loop transfer function bode plot characteristic.

Let $\frac{\omega_{u,loop}}{\omega_z} = c$, so that

$$PM = \varphi = \tan^{-1}\left(\frac{\omega_{u,loop}}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_{u,loop}}{\omega_p}\right) = \tan^{-1} c - \tan^{-1}\frac{c}{b+1} = \tan^{-1}\frac{bc}{1+b+c^2}$$

By using the trigonometric identity

$$\tan^{-1} A - \tan^{-1} B = \tan^{-1}\frac{A-B}{1+AB}$$

We get

$$\tan\varphi = \frac{bc}{1+b+c^2}$$

Use Matlab to plot the c versus b when PM is 60° as shown in Figure 2. We can see that in order to achieve 60° phase margin, C_1 has to be more than 10 times larger than C_2. Typically, the value of c is set in the range of 6 to 10 [1]. The larger the c value, the better the reference feed-though suppression will be as shown in Table 2. Another reason to set c larger is better to process variation.

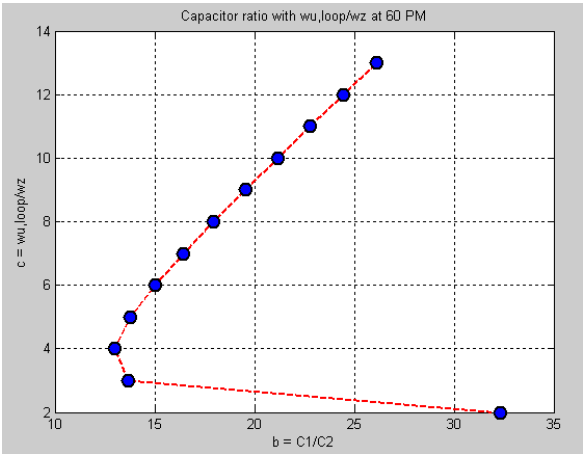


Figure 2 Plot of c versus b when the PM is at 60°.

Table 2 Different c value leads to different reference feed-through suppression.

$c = \frac{\omega_{u,loop}}{\omega_z}$	$b = \frac{C_1}{C_2}$	$\frac{\omega_{ref}}{\omega_p}$
4	13	2.9
8	18	4.2

Next, Let's define $\omega_{ref} = a \cdot \omega_{u,loop}$, we have to make sure loop unity bandwidth less than one tenth of the reference frequency for the following reasons (Figure 3):

- Linearize the model so that Vctrl can be approximated as continuous time rather than discrete time.
- Filter out periodic reference disturbance due to reference clock feed-through.

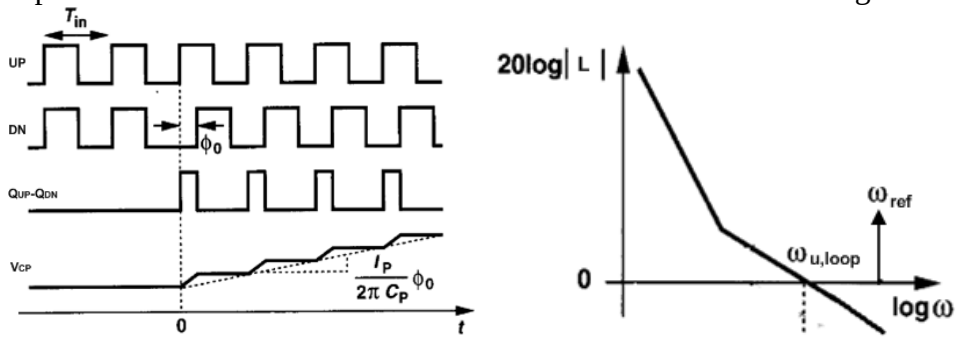


Figure 3 Graphical illustration of $\omega_{u,loop}$ and ω_{ref} relationship.

Once we have all the information, we can solve for C_2 by substituting $\omega_{u,loop}$ into the loop magnitude function.

$$\frac{I_{CP}K_{VCO}}{(b+1)C_2N} \cdot \frac{\sqrt{1+c^2}}{\left(\frac{\omega_{ref}}{a}\right)^2 \sqrt{1+\left(\frac{c}{b+1}\right)^2}} = 1$$

So we have C_2 as

$$C_2 = \frac{I_{CP}K_{VCO}}{N} \cdot \frac{a^2\sqrt{1+c^2}}{(\omega_{ref})^2\sqrt{(b+1)^2+c^2}}$$

Once C_2 is solved, we can get C_1 based on the coefficient b, and R_1 from zero. The system parameters can be solved by using Excel with above equations. One possible parameters are listed in Table 3. But, we have to know K_{VCO} first to determine the system parameters of the loop filter. Once the parameters are set, loop transfer function can be plotted using Matlab (Figure 4).

Table 3 Type-II 3rd-order PLL component parameter specifications.

K_{VCO}	I_{CP}	R_1	C_1	C_2	PM	ζ
$1.2\ GH/V$	$20\ \mu A$	$2.98\ K\Omega$	$684\ pF$	$38.1\ pF$	60°	0.74

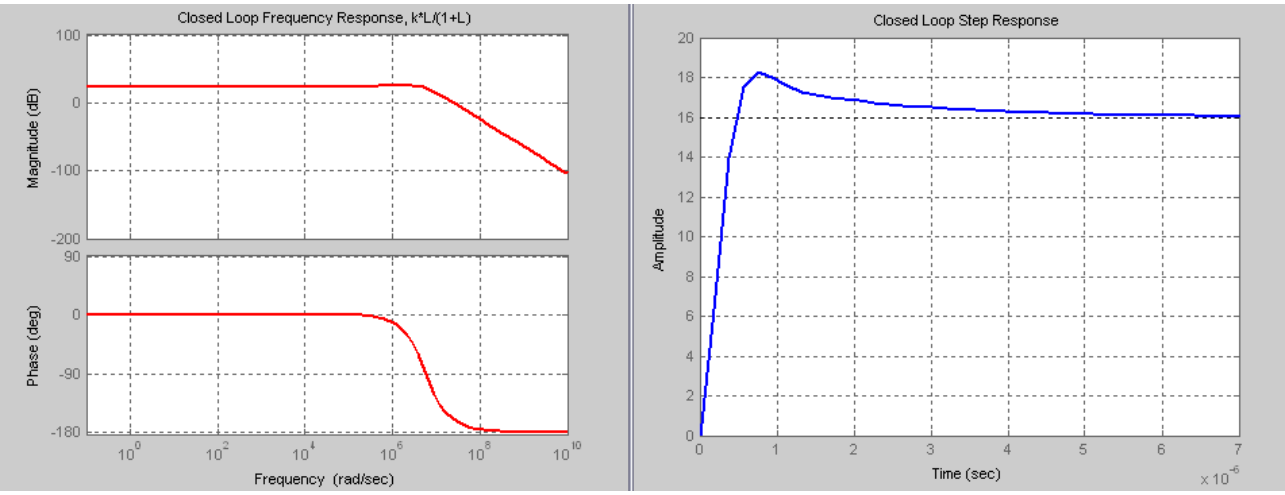


Figure 4 Bode plot and step response of the closed-loop transfer function.

2.2 Closed-loop Noise Transfer Functions

Everything add noise in the PLL system include reference clock, PFD, charge pump, supply voltage, etc. In order to find out actual cause of the noise (jitter), we have to look at jitter transfer function for each block in the system. The closed-loop transfer function (Figure 6) of the PLL model as shown in Figure 5 is studied for noise introduced in the system with Simulink linear analysis function.

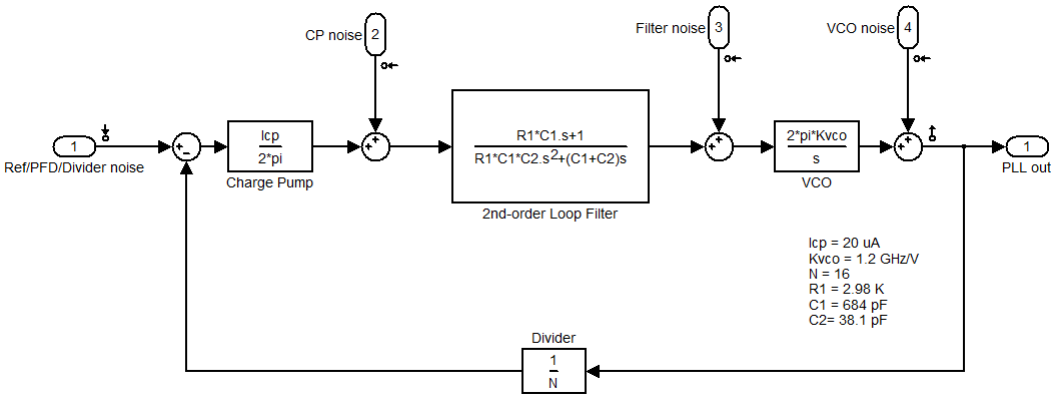


Figure 5 Simulink PLL model for noise transfer function.

The reference, PFD and divider noise transfer function are the same the system closed-loop transfer function $H(s)$.

$$H(s) = \frac{N \cdot L(s)}{1 + L(s)}$$

The DC gain is N, in this case N is 16 which is 24.1 dB.

The charge pump noise transfer function ($H_{CP}(s)$) has the same effect as is introduced from the reference, but scaled by $2\pi/I_{cp}$.

$$H_{CP}(s) = \frac{2\pi}{I_{cp}} H(s)$$

Which means lowest-power change pump will contribute more noise.

Continue down to the loop filter, its noise transfer function ($H_{LF}(s)$) is further scaled by the loop

filter impedance $Z(s)$.

$$H_{LF}(s) = \frac{1}{Z(s)} H_{CP}(s) = \frac{2\pi K_{vco}}{s} \frac{1}{1 + L(s)}$$

This is a band-pass TF.

VCO noise accumulates due to its integral characteristic of VCO transfer function. The transfer function ($H_{VCO}(s)$) for noise introduced after the VCO is a high-pass shape.

$$H_{VCO}(s) = \frac{s}{2\pi K_{vco}} H_{LF}(s) = \frac{1}{1 + L(s)}$$

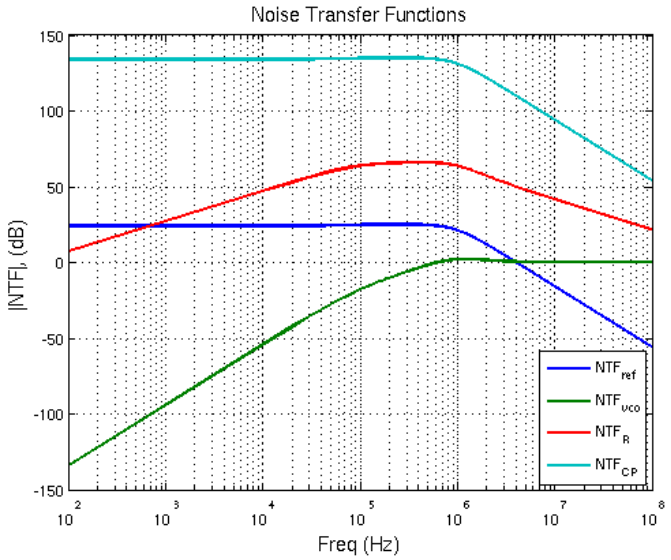


Figure 6 PLL noise transfer functions.

As can be seen, all of the added noise for the PLL system can be attributed to two primary noise sources – detector noise and VCO noise [1]. Detector noise is considered to be the addition of white and spurious noise, and is composed of noise due to the reference, PFD and divider jitter, charge pump noise, and spurious noise from the reference clock. VCO noise is assumed to roll of at – 20 dB/dec, and is caused primarily by thermal noise sources in the VCO structure. But in practice, VCO noise rolls off at a higher rate than – 20 dB/dec at low frequencies due to the influence of the flicker noise.

Detector noise can be reduced by setting the bandwidth as low as possible. By reducing the bandwidth, the VCO noise TF will not only shifts to the low frequency side, but also the magnitude will go up. So in order to minimize VCO noise, we have to raise the bandwidth of the loop. The peak point of the band-pass (refer to Figure 6) is the bandwidth of the loop. Optimizing loop bandwidth is basically balancing between the noise due to the reference and VCO.

3 Circuit Design

3.1 VCO Design and Simulation

The traditional current starved VCO topology doesn't work well at wide frequency range when the operating voltage drops to 1.2 V. The reason is that when the VCO oscillation amplitude is so large that makes the current source in the delay cell in triode region most of the time. VCO self-modulation takes over the control of current control. So, in order to meet frequency range from 100 MHz to 500 MHz, we have to modify the traditional current-starved cell.
Maneatis cell [2] shown in Figure 7, NMOS cross-coupled pair are used to increase speed at higher frequency operation. Symmetric load I-V characteristics are simulated at different bias condition and plotted in Figure 8. If the VCO is oscillating at the center of symmetric curve, the load resistance seen at differentially will be equal due to the same slope. In small-signal sense, it features better PSRR. The disadvantage of this cell is the swing is limited.

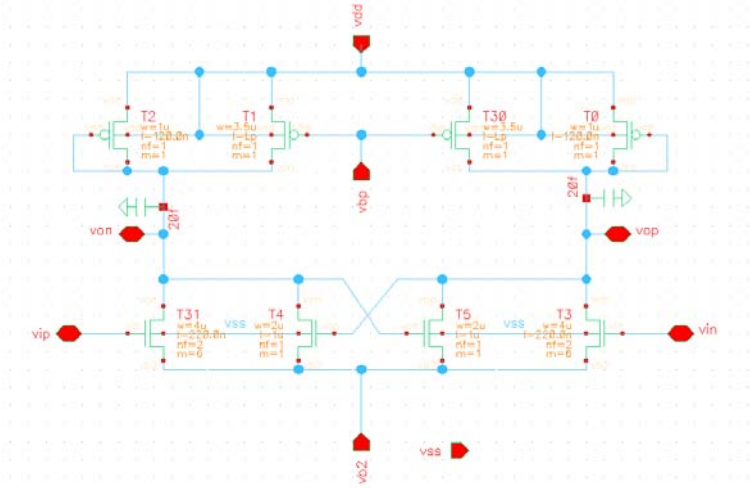


Figure 7 Maneatis cell.

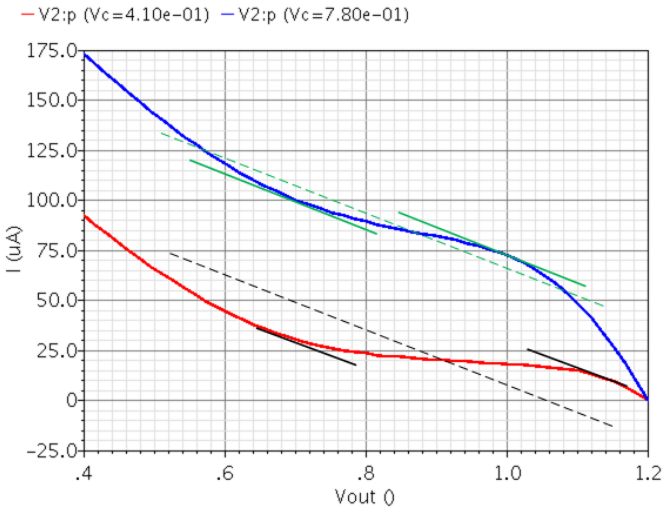


Figure 8 Symmetric load I-V curves.

The complete VCO is shown in Figure 9. Source degenerated common-source is adopted to linearly convert control voltage to current if the $g_m R_s$ is large. Bootstrapped replica-bias sets the common-mode voltage of the Maneatis cell to be the DC bias of the PMOS. By connecting the CS nodes of

all delay cells together, the oscillations present on the unconnected CS nodes add together out of phase, reducing the Vds modulation of the combined current source [3].

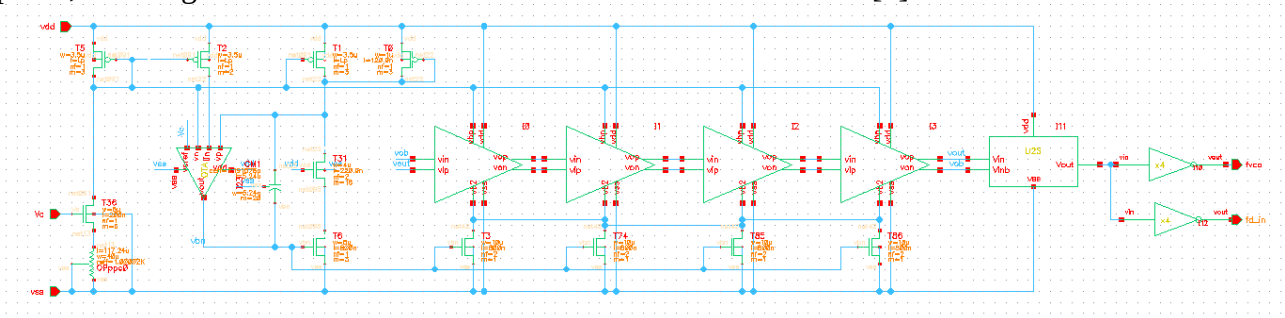


Figure 9 Complete VCO schematic.

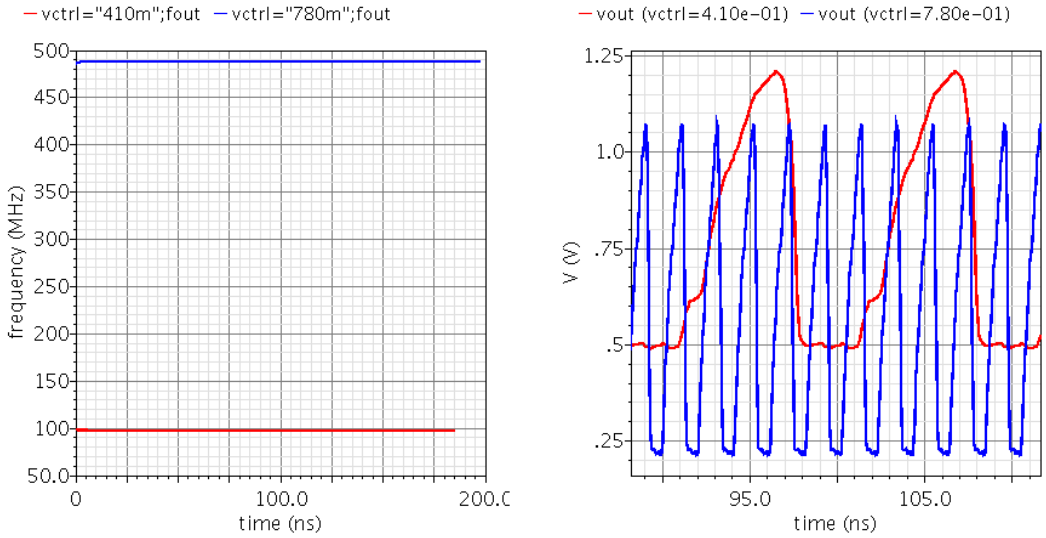


Figure 10 VCO waveforms at different V_{ctrl} voltages.

3.1.1 VCO voltage tuning range

Frequency and VCO gain with varying control voltage are plotted in Figure 11. The linear range is only from 550-650 mV.

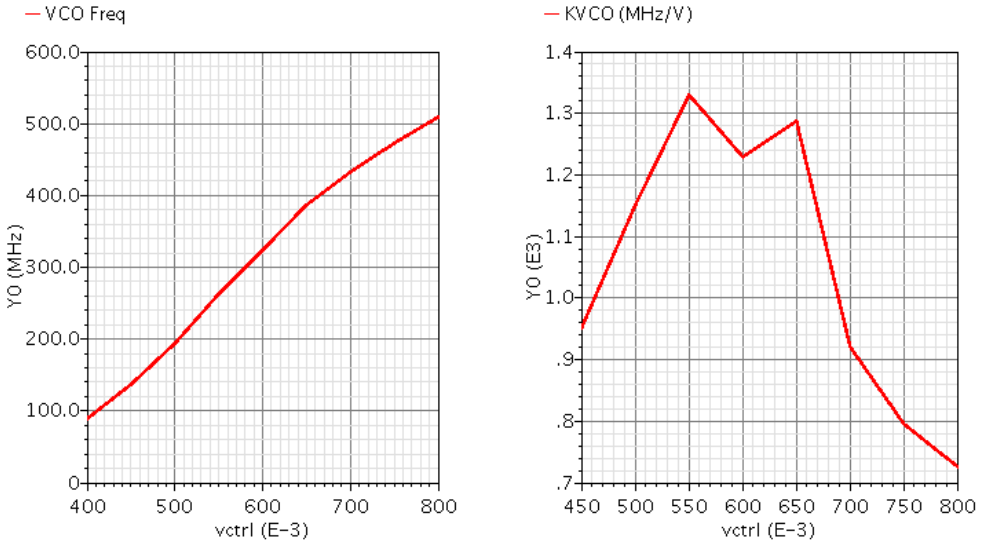


Figure 11 Control voltage tuning with PSS analysis.

3.1.2 Frequency pushing

Frequency changes with varying power supply voltage.

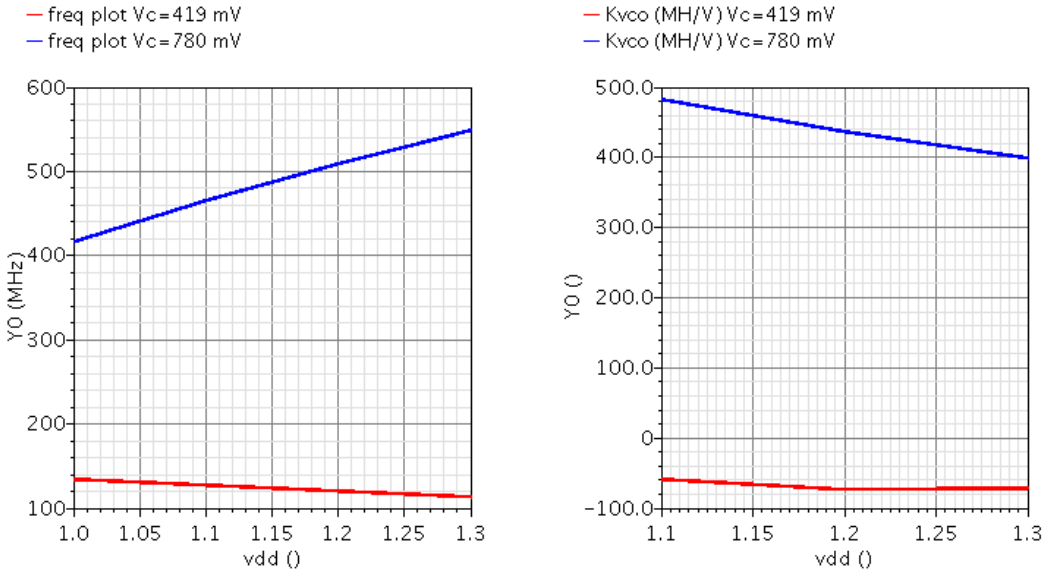


Figure 12 Frequency pushing with PSS analysis.

3.1.3 Phase noise

Phase noise a frequency domain version of viewing clock jitter. In general corner frequency is where the flicker noise and thermal noise intersects. As shown in Figure 13, the phase noise is larger than 0 dBc/Hz when the offset frequency is 100 Hz, this phenomenon seems unreasonable. But, it won't contribute much to the total PLL phase noise if the bandwidth of the PLL not too small. Higher side offset frequency phase noise need to be optimized due to high-pass VCO noise transfer function. We have to try to suppress phase noise below -100 dBc/Hz at 500 KHz for good VCO.

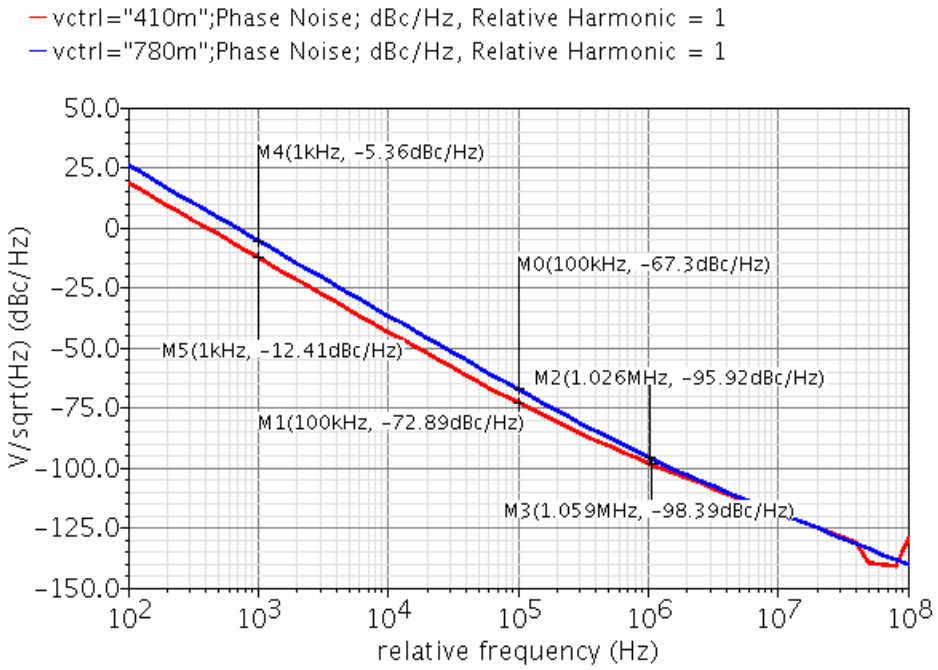


Figure 13 VCO phase noise plot.

3.2 Phase Frequency Detector

Pass-transistor DFF PFD [4] is used as shown in Figure 14. Small latches are added to optimize the crossing point. UPB and DN clock skew should be minimized by using TG. In order to avoid PFD+CP+LF dead zone, minimum reset pulse width by inserting delay in the reset path must be able to turn on the switches in the charge pump [5]. Otherwise, when the phase error is less than a certain value, the PLL will lose lock.

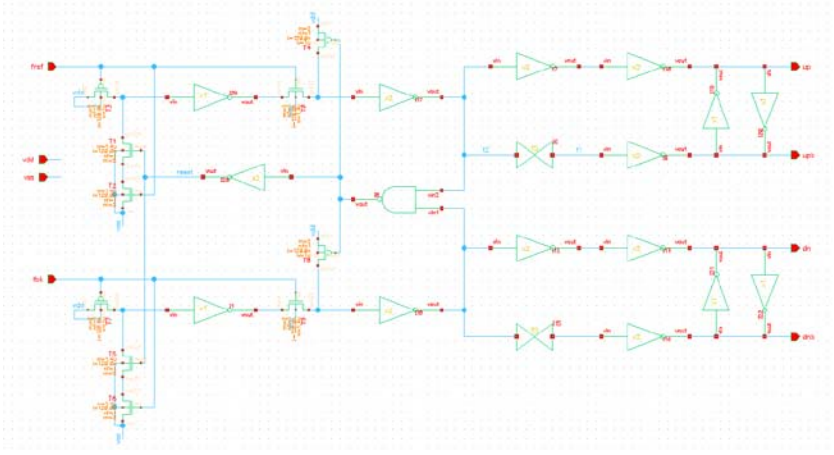


Figure 14 Pass-Transistor DFF based PFD.

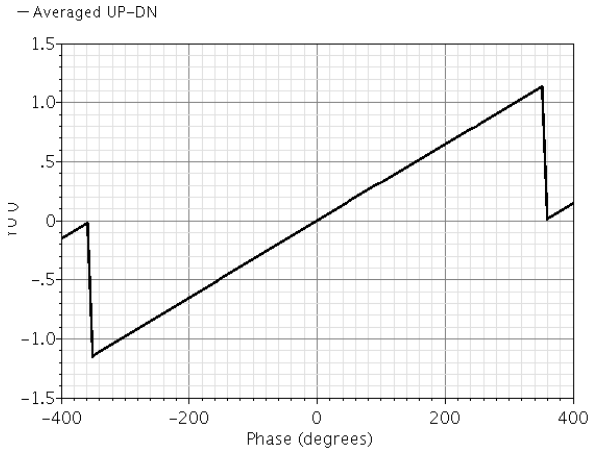


Figure 15 Transfer curve of Pass-Transistor FF PFD at 6.25MHz.

3.3 Charge Pump & Passive Loop Filter

On the one hand, the smaller the charge pump current, the larger the noise will contribute to the PLL output phase noise. On the other hand, the larger the current, the larger the capacitors are required in the loop filter. That is noise and area tradeoff.

3.3.1 Charge Pump Design Issues

Several design issues relate to charge pump design that must be addressed:

- Dead zone

As previously discussed in the PFD, we have to make sure enough wide pulse width to avoid issue of the small phase offset fail to turn-on the CP switches.

- UP and DN skew

This has been taken care in the PFD design.

- Current mismatch

Current mismatch can be translated into static phase offset (shown in Figure 16), in turn modulates

Vc at steady-state (shown in Figure 17), so that cause spurious tones at the PLL output. The phase offset due to charge pump current mismatch can be derived as shown in Eq. 1 [6]. Where the T_{rst} is the reset pulse width, T_{ref} is reference clock period.

$$\Delta\emptyset = 2\pi \frac{T_{rst}}{T_{ref}} \cdot \frac{\delta I_{cp}}{I_{cp}} \qquad \text{Eq 1}$$

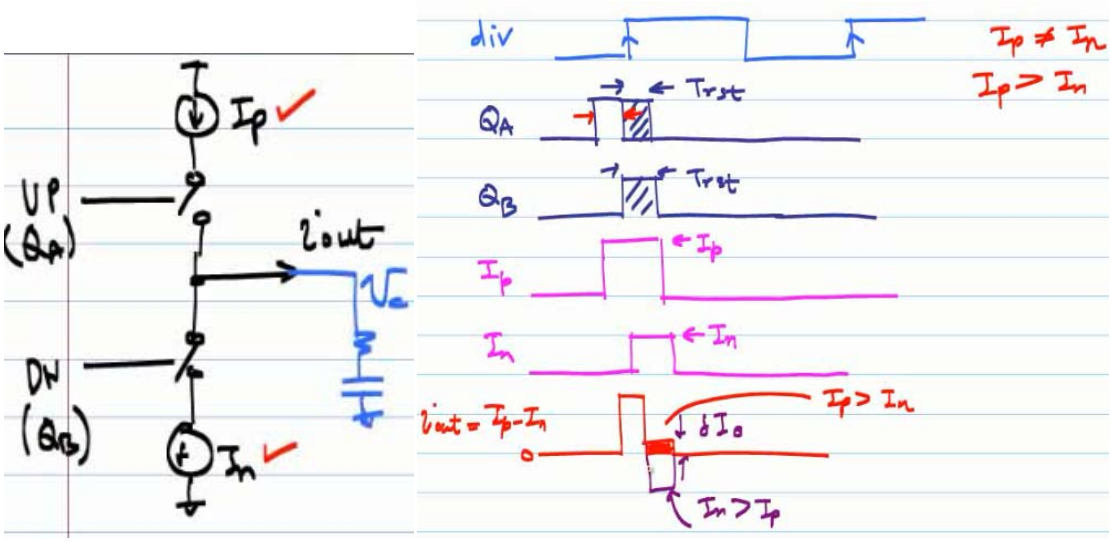


Figure 16 Charge pump current mismatch leads to static phase offset.

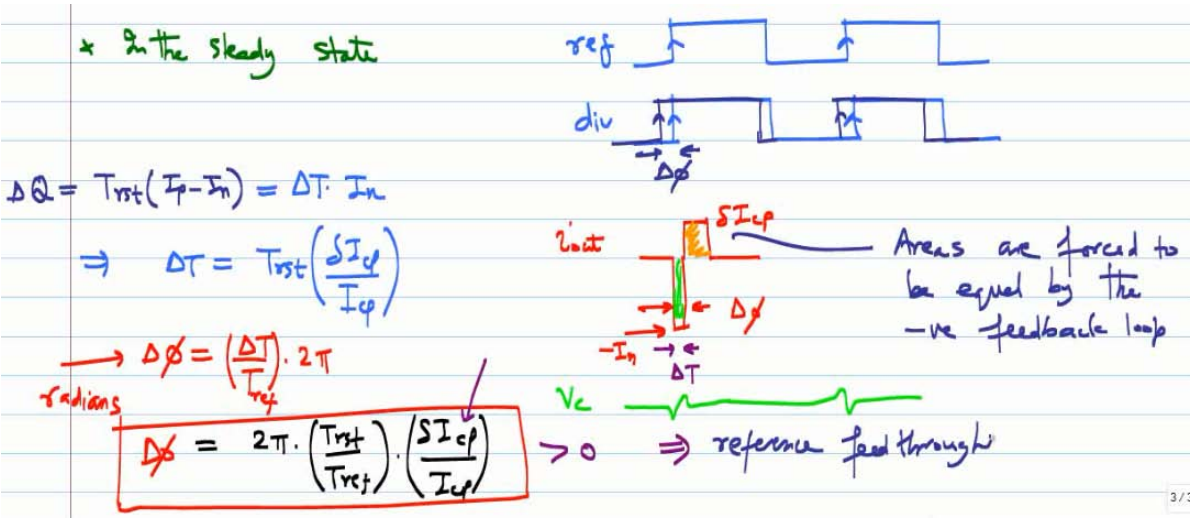


Figure 17 Charge pump current mismatch lead to spur on Vc in the steady-state.

- Charge-sharing

When the switches S_1 and S_2 turn on, V_X and V_Y rises and falls, respectively. And eventually, $V_X = V_Y = V_C$, charge-sharing between C_X, C_Y and C_1.

$$V_{C,final} = \frac{C_X V_X + C_Y V_Y + C_1 V_C}{C_X + C_Y + C_1} = \frac{C_Y V_{DD} + C_1 V_C}{C_X + C_Y + C_1}$$

If the parasitic capacitors C_X and C_Y are large, $V_{C,final}$ will droop periodically, that will lead to the VCO phase error, and jittery PLL output.

For example, if $C_X = C_Y = 100\ fF$, $C_1 = 10\ pF$, $V_{DD} = 1.2\ V$, $V_C = 0.45\ V$, so given enough time

$V_{C,final} = 0.453\ V$. This may not be a big issue if the parasitic capacitor values are kept small.

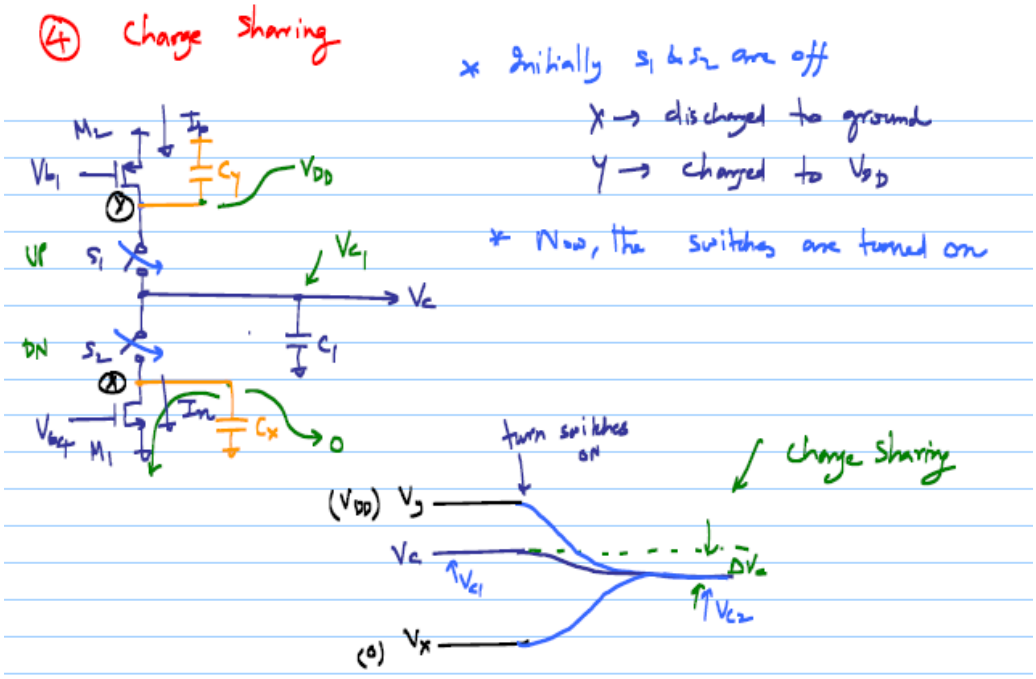
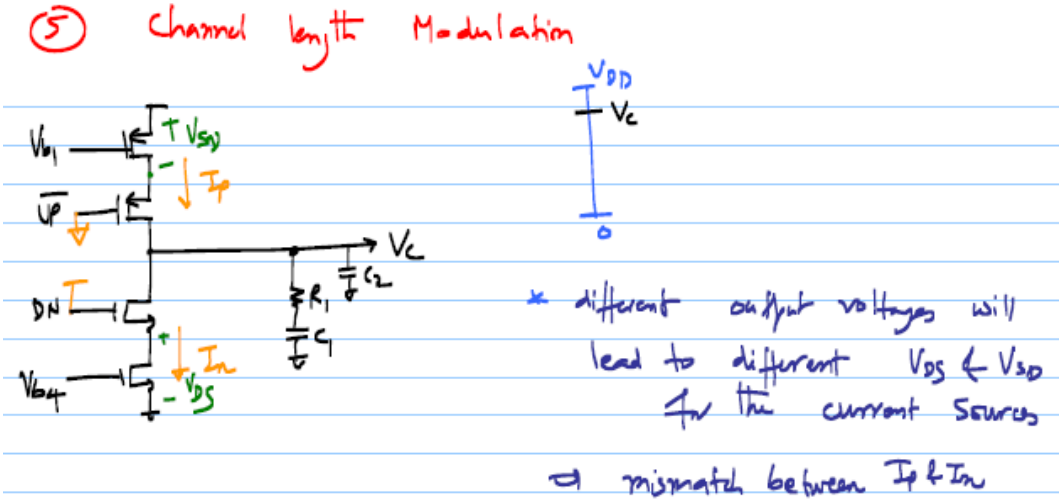


Figure 18 Charge-sharing.

- Channel length modulation

V_C may not be always settled at the $V_{DD}/2$ when at the steady-state, so that leads to different V_{ds} for upper PMOS and lower NMOS current sources. Even though I_{cp} for up and down current are depend up on each other, channel length modulation effect still bothers at the effective branch.



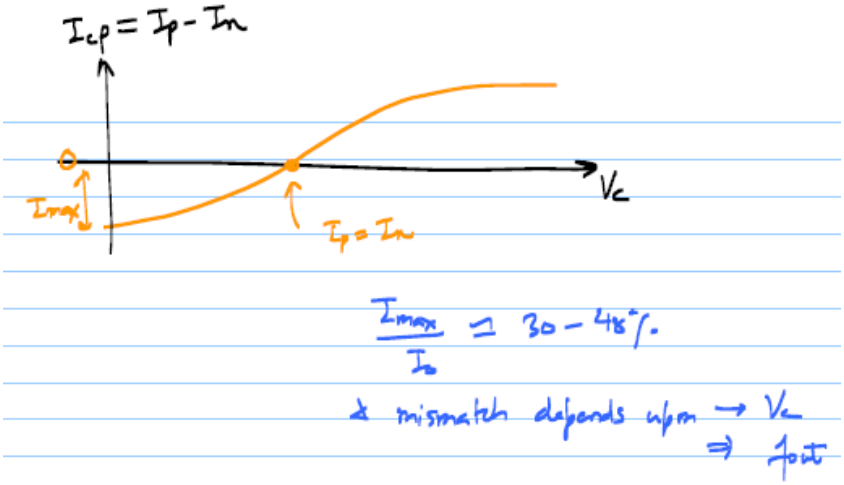


Figure 19 Channel length modulation effect.

- Clock feed-through

UP and DN signal feed through from the C_{gd} will cause spurs, so that minimum size of the switches are preferred. But the smaller the size, the larger the mismatch, so dummy devices need to be added.

3.3.2 Charge Pump Circuit Design

The improved charge pump schematic is shown in Figure 20. By using differential switches steering the current, the up and down current sources are always kept on, eliminates charge sharing issue and current source devices are always in saturation. The complementary node V_l of V_C is well fixed by an analog buffer OTA2 to reduce transient current mismatch. Replica bias scheme is used with OTA1 to make sure up and down current are the same, systematic mismatch is reduced. The long term average integration node, V_{cref}, is chosen instead of proportional node (V_C) as the reference for both OTAs.

The gain and bandwidth of both the OTA loops have to be large and at least as wide as reference clock frequency. The input range of the OTAs should meet both high and low steady-state V_C values so that wide common-mode range opamp is desired. So that the OTA used both NMOS and PMOS input pair, but not necessarily need to be constant-g_m in this application.

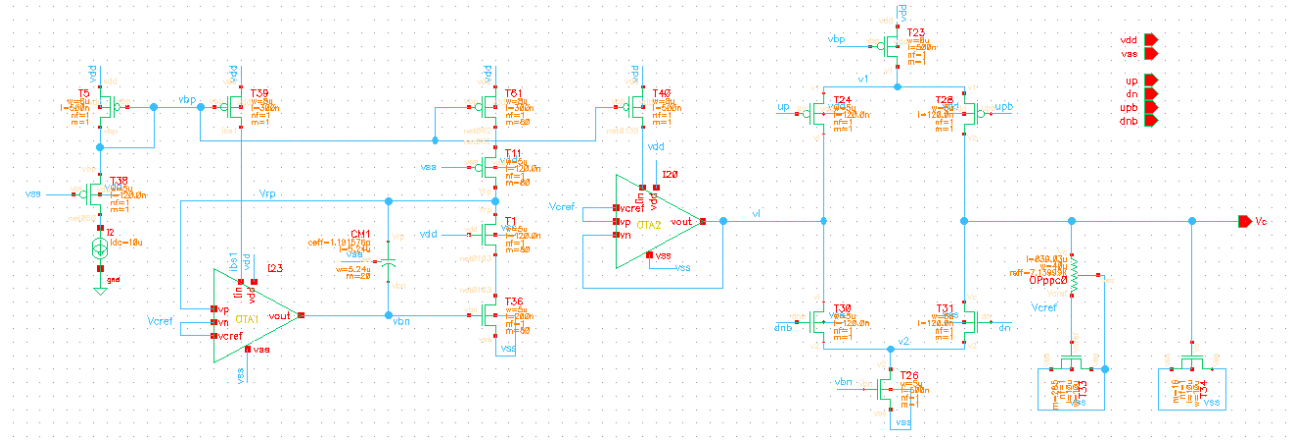


Figure 20 Charge pump and loop filter schematic.

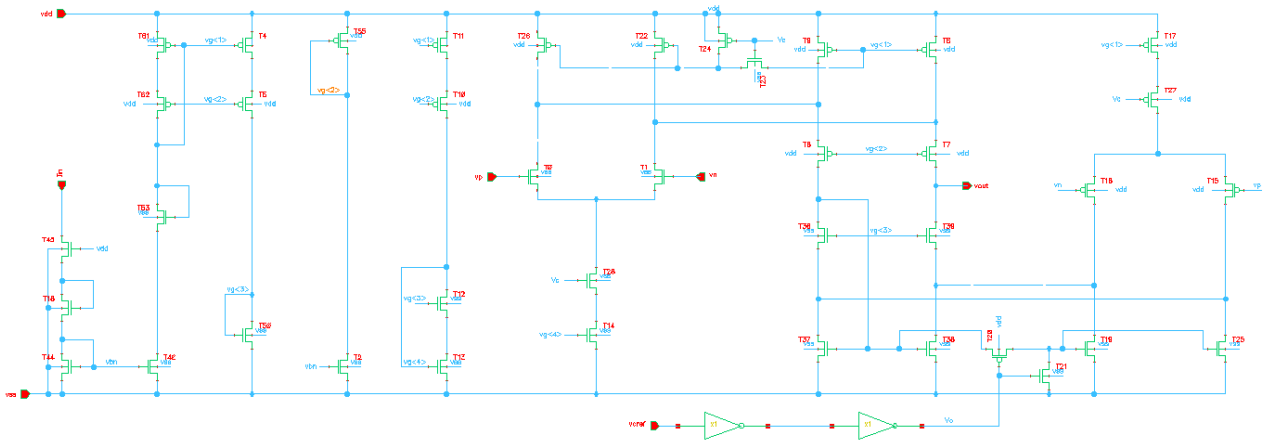


Figure 21 OTA1 for replica biasing in charge pump.

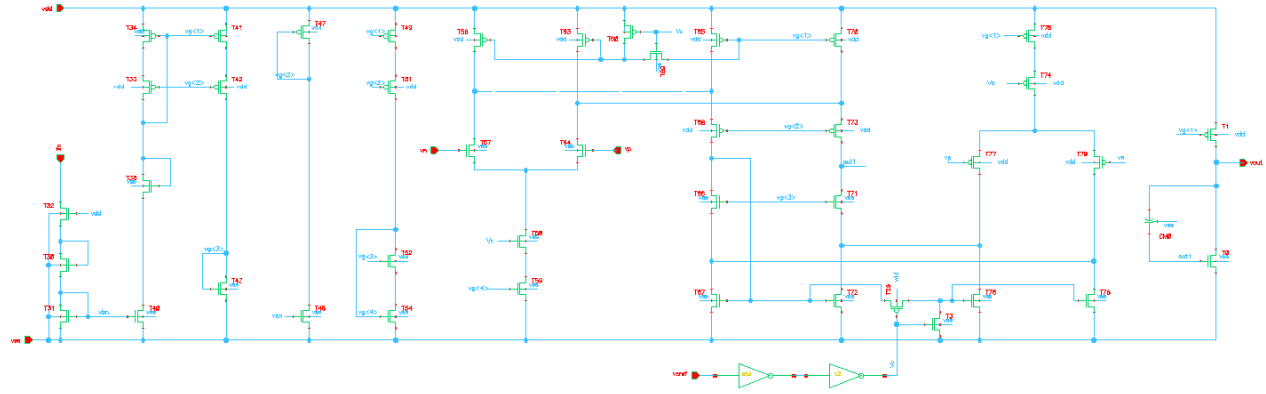


Figure 22 OTA2 in charge pump.

3.3.3 CP Simulation Results

Stability of both OTA loops is verified. UPB and DN signals and current sources at zero phase offset are plotted in Figure 25. We can see that the up and down current sources can track well within the valid pulse width except at the pulse transition. Mismatch of the up and down currents during pulse transition will cause spur on V_C as can be seen in Figure 25. V_C versus phase is plotted in Figure 26 to check for charge pump linearity and dead zone issue.

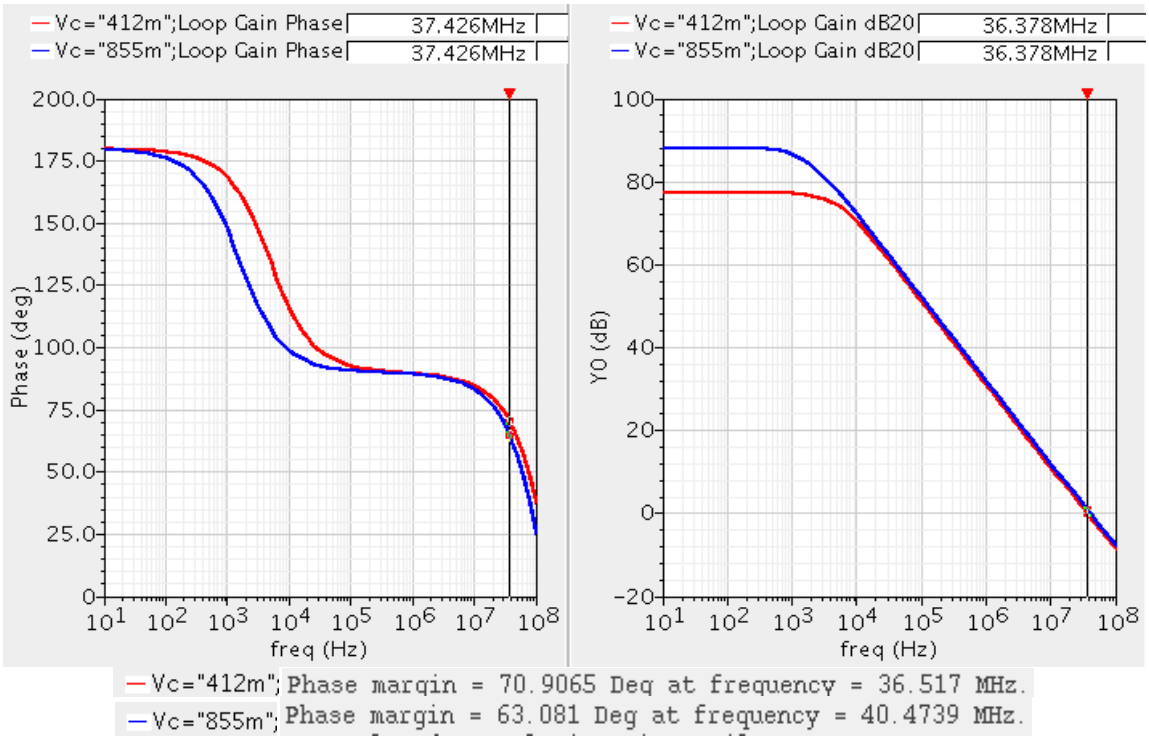


Figure 23 .stb analysis of OTA1.

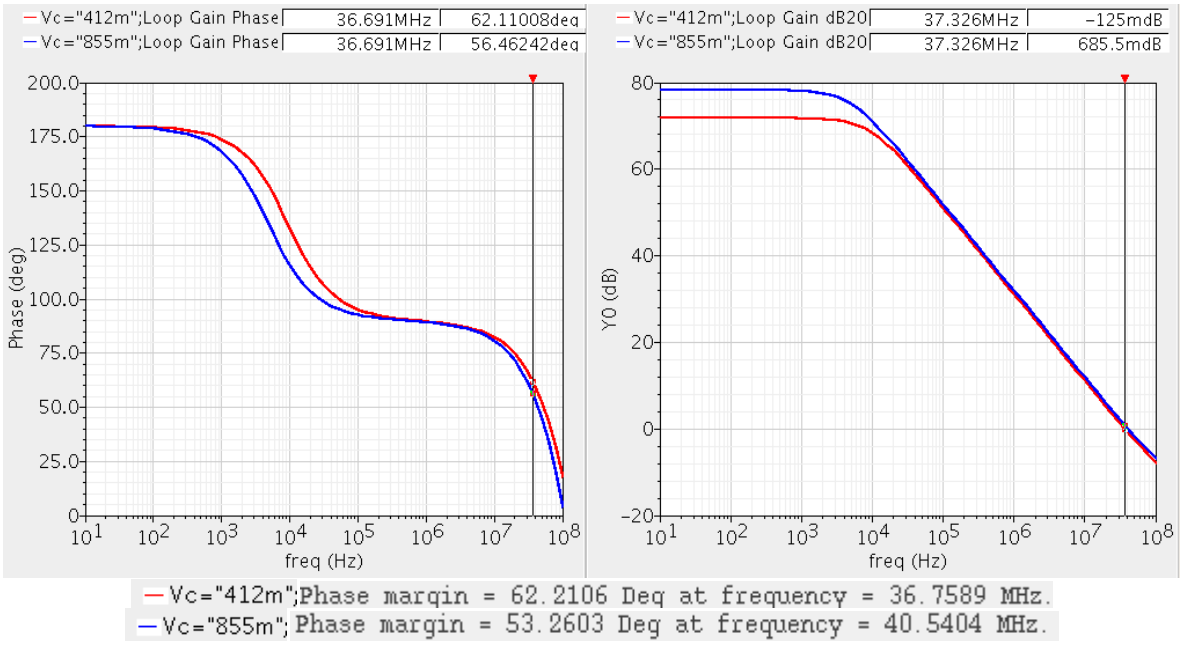


Figure 24 .stb analysis of OTA2.

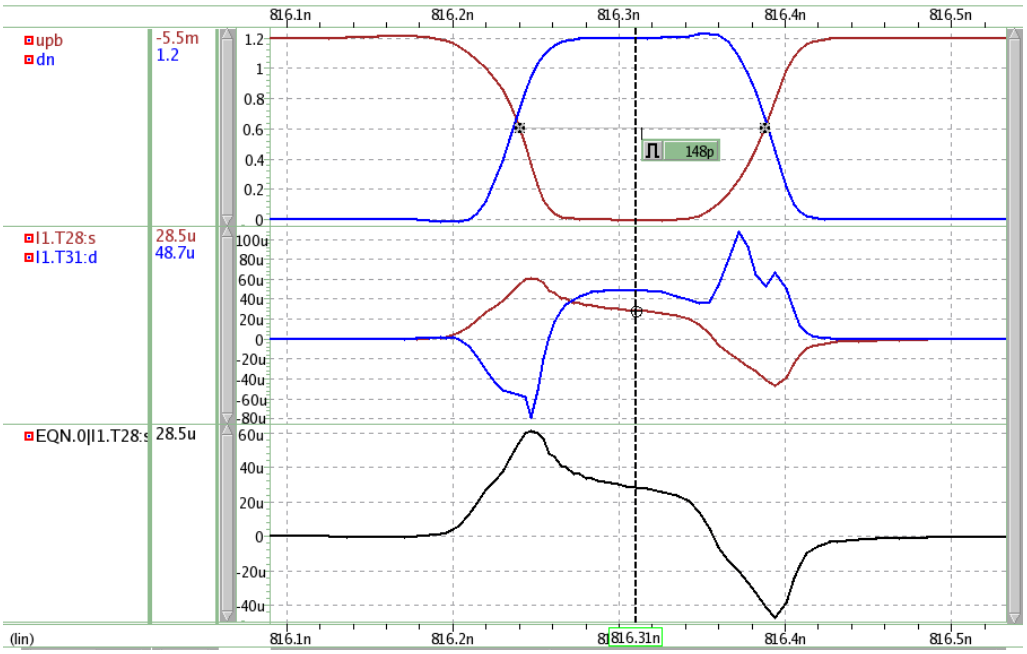


Figure 25 Transient UP/DN and current waveforms at zero phase error.

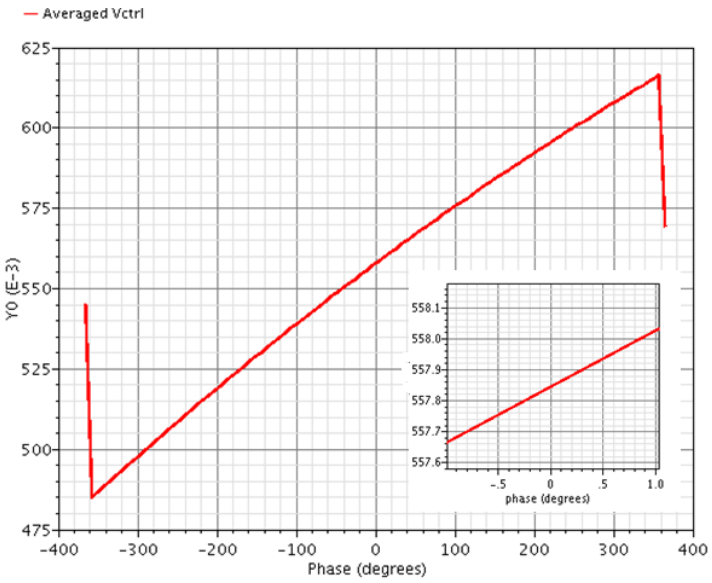


Figure 26 Vctrl-phase plot with phase difference from -365° to 365°.

3.4 Frequency Divider

True Single-Phase-Clock (TSPC) dynamic flip-flop [7] is used as the building block of dividers.

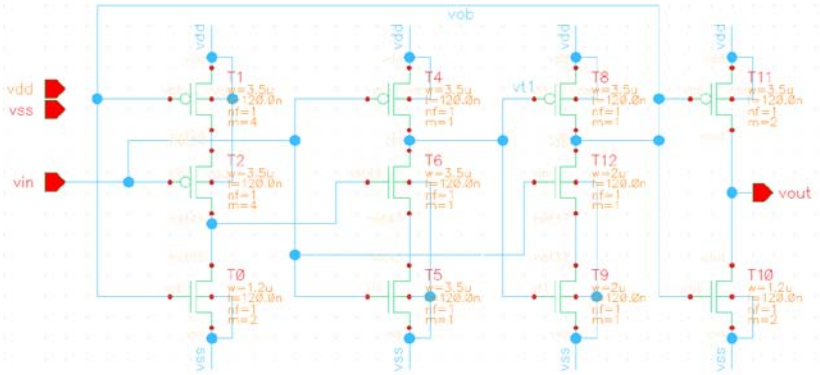


Figure 27 TSPC divider-by-2 schematic.

4 Top-Level Simulation Results

PLL locking is simulated, eye diagram is plotted to measure the peak-to-peak jitter. PLL output PSD is also plotted in Figure 32. Individual block phase noise and total PLL phase noise are extracted and processed by Matlab shown in Figure 33.

4.1 PLL Locking

In order to observe more practical peak-to-peak jitter, transient noise option must be enabled in the transient analysis. Figure 28 shows the transient noise setup for both cases.
From BDA documents we have following recommendations:
Noise Fmax ≥ 50*VCOfreq, Noise Fmin=10/tstop.

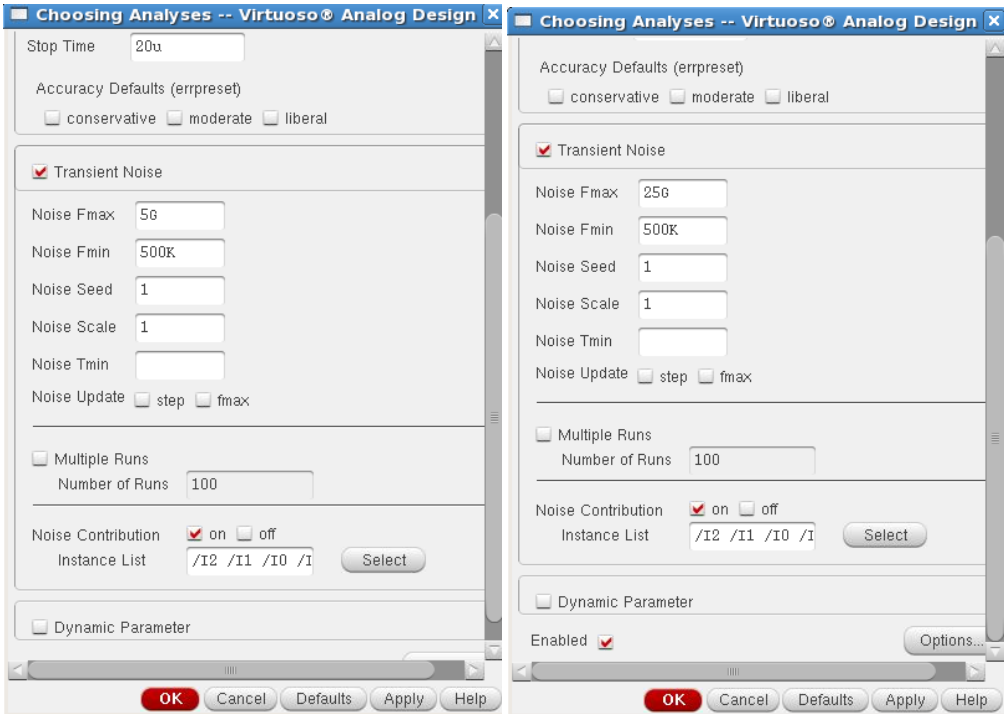


Figure 28 Transient noise setting for 100MHz and 500MHz.

Control voltage at the loop filter is checked for PLL locking at both cases are plotted in Figure 29

and Figure 30. The locking time is too long, it may due to the Opamp settling. The PSD plots (Figure 32) of the PLL output shows it oscillating at the desired frequencies.

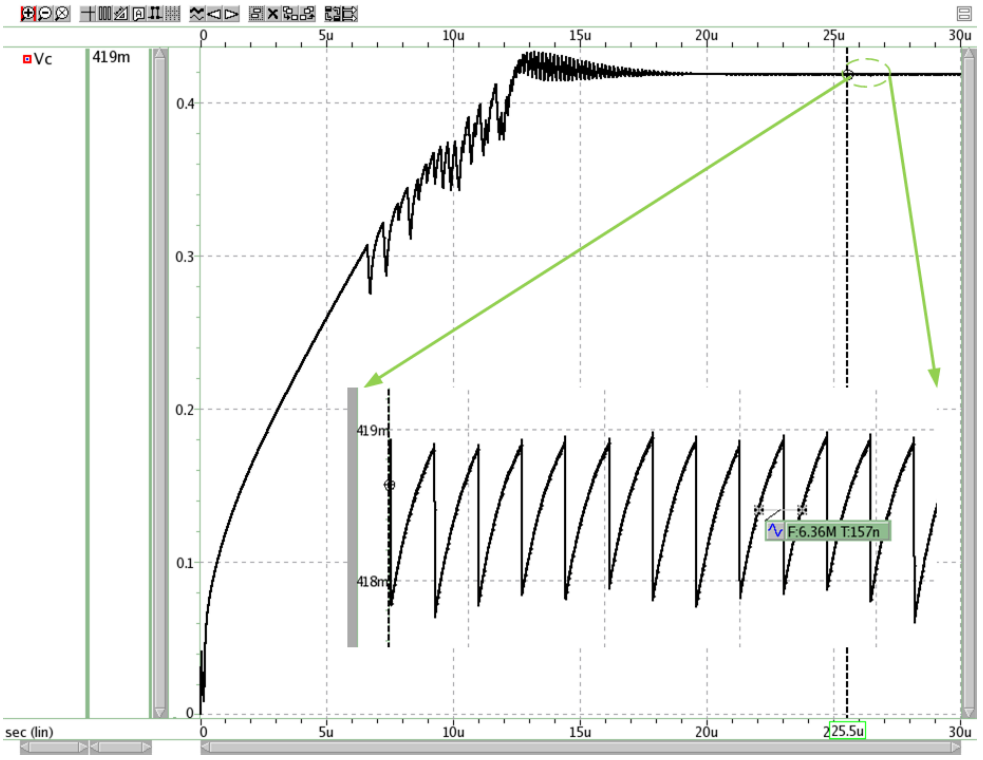


Figure 29 Vc plot at 100 MHz PLL locking with transient noise enabled.

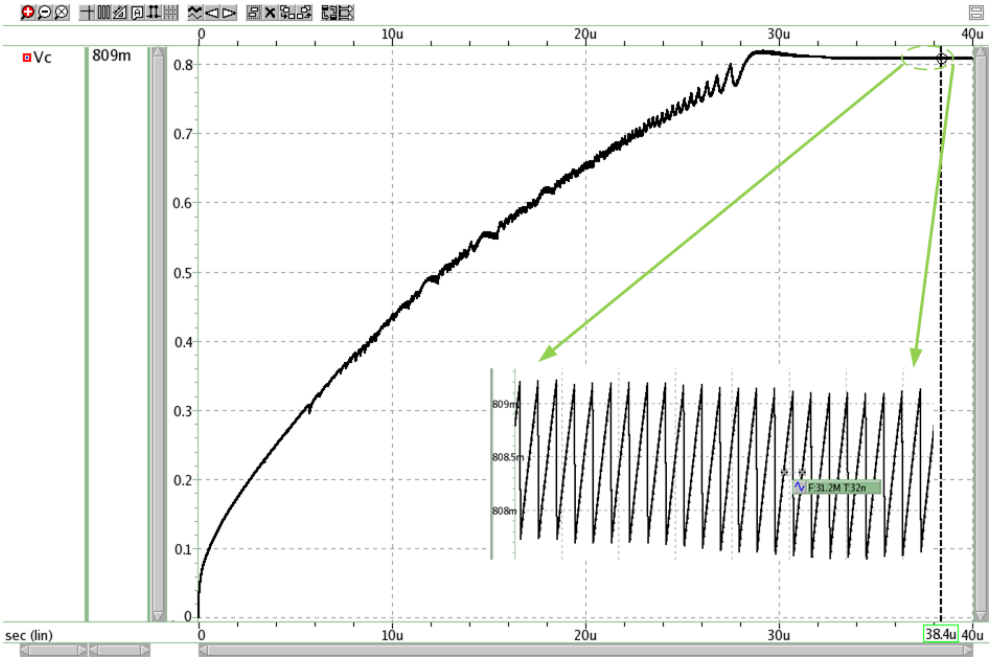


Figure 30 Vc plot at 500 MHz PLL locking with transient noise enabled.

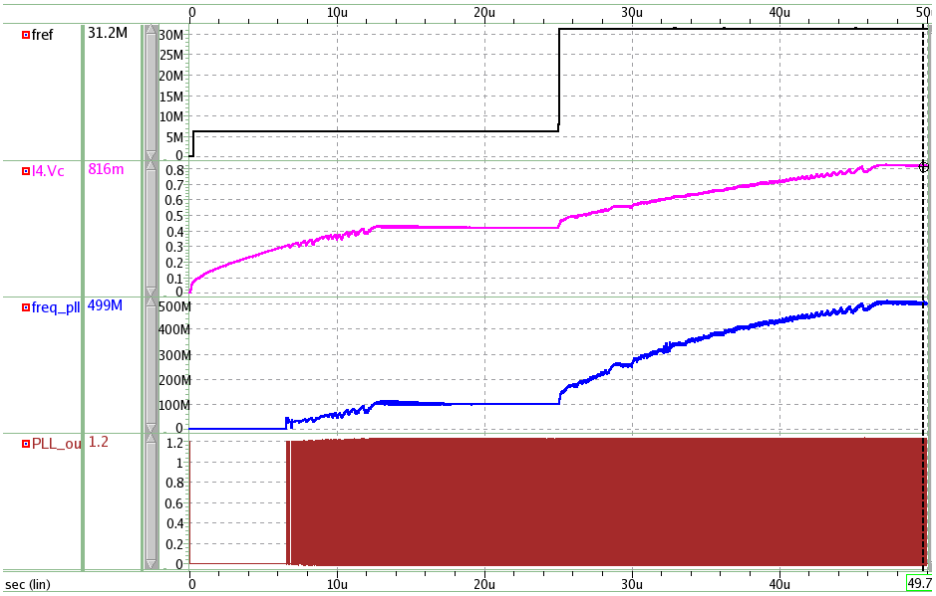


Figure 31 Reference frequency hopping.

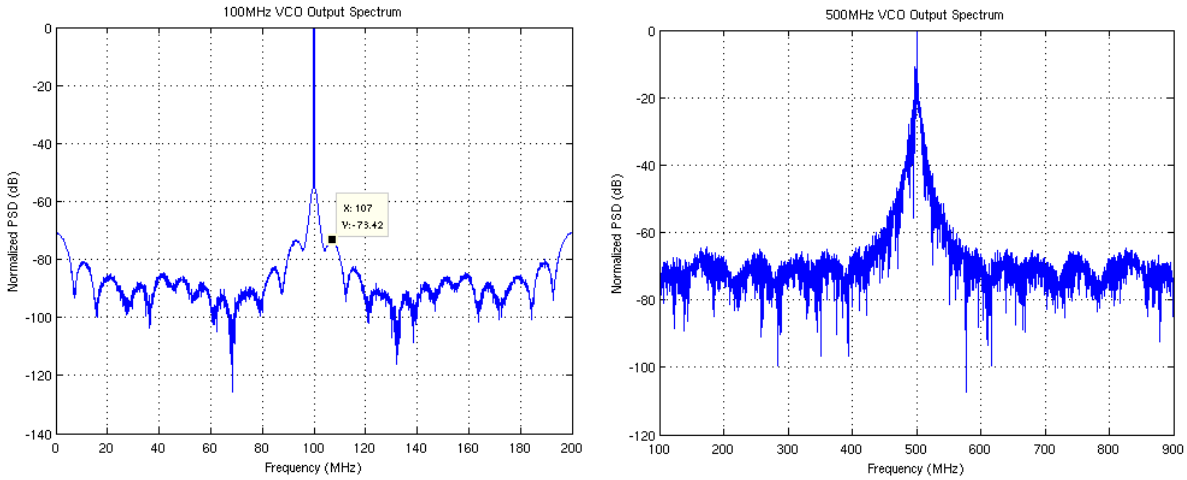


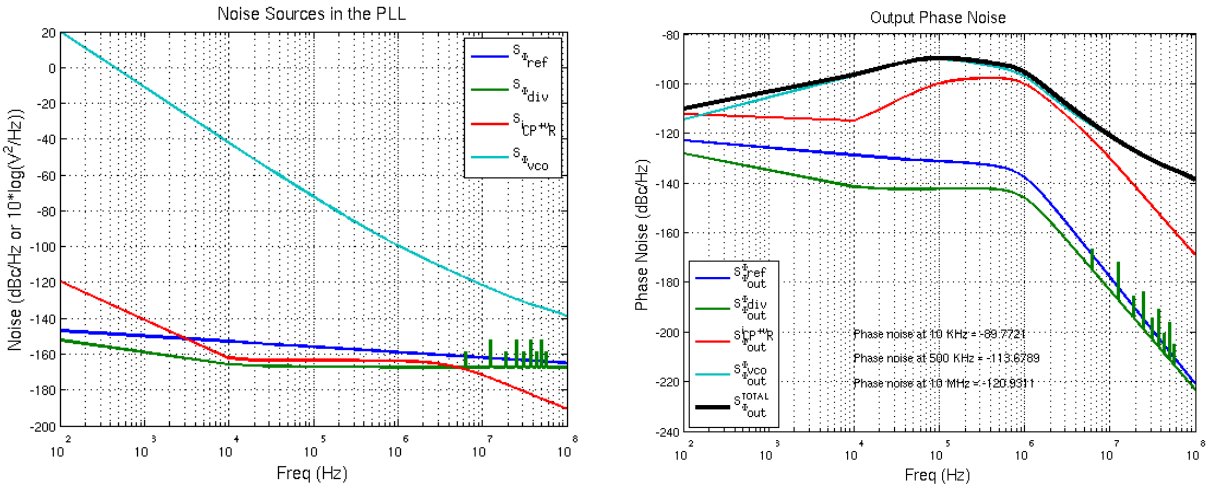
Figure 32 VCO Spectrum at 100MHz and 500MHz with transient noise enabled.

4.2 PLL Phase Noise and rms Jitter

Noise sources in the PLL and PLL output phase noise are plotted in Figure 33 and Figure 34, for 100 MHz and 500 MHz, respectively. We can use Eq 2 to calculate the variance of PLL phase noise PSD in the time domain to get the rms jitter:

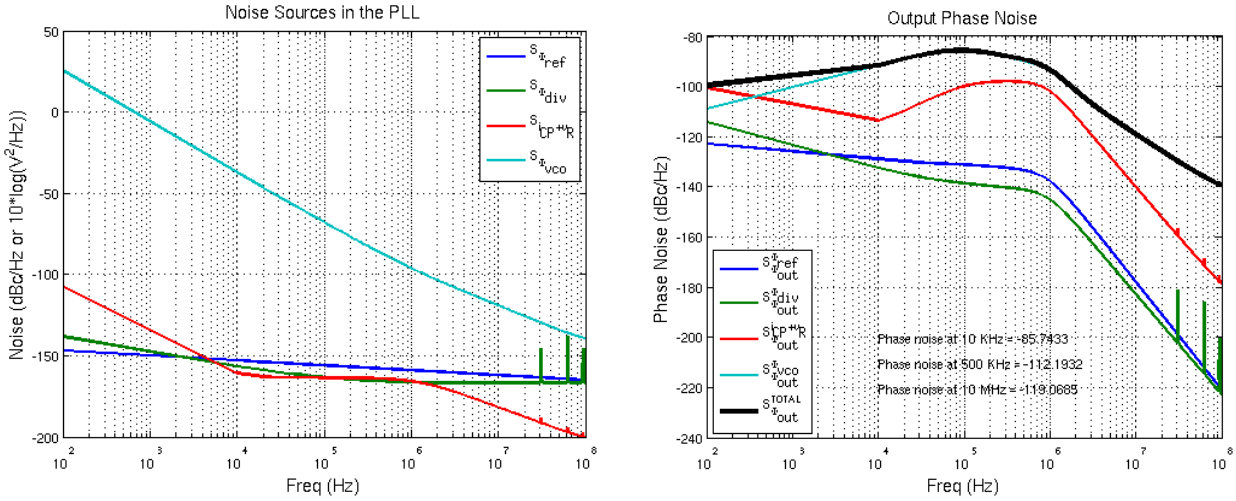
$$\sigma_{\Delta T} = \sqrt{\int_0^{\infty} S_{\phi_{out}}^{Total}(f)df} \cdot \frac{T_{VCO}}{2\pi} \qquad \text{Eq 2}$$

Due to high VCO phase noise, the rms jitter derived from the PLL total phase noise can't meet the 0.2% rms jitter specification.




```
jitter_rms =  4.5217e-11
```

Figure 33 PLL output phase noise at 100MHz.




```
jitter_rms =  1.2631e-11
```

Figure 34 PLL output phase noise at 500MHz.

4.3 Peak-to-peak Jitter

We also can map the desired rms jitter to the peak-to-peak jitter according to Eq 3 [8]. Let's say if we want a BER of 10^{-12}, then α is 14.069, so the peak-to-peak jitter for 100MHz PLL should be less than 281.4 ps. As shown in Figure 35 and Figure 36, it is obviously can't meet the 0.2 % rms jitter spec. Jitter results are summarized in Table 4.

$$\boldsymbol{Jitter_{P-P} = \alpha \cdot Jitter_{RMS}} \quad \text{Eq 3}$$

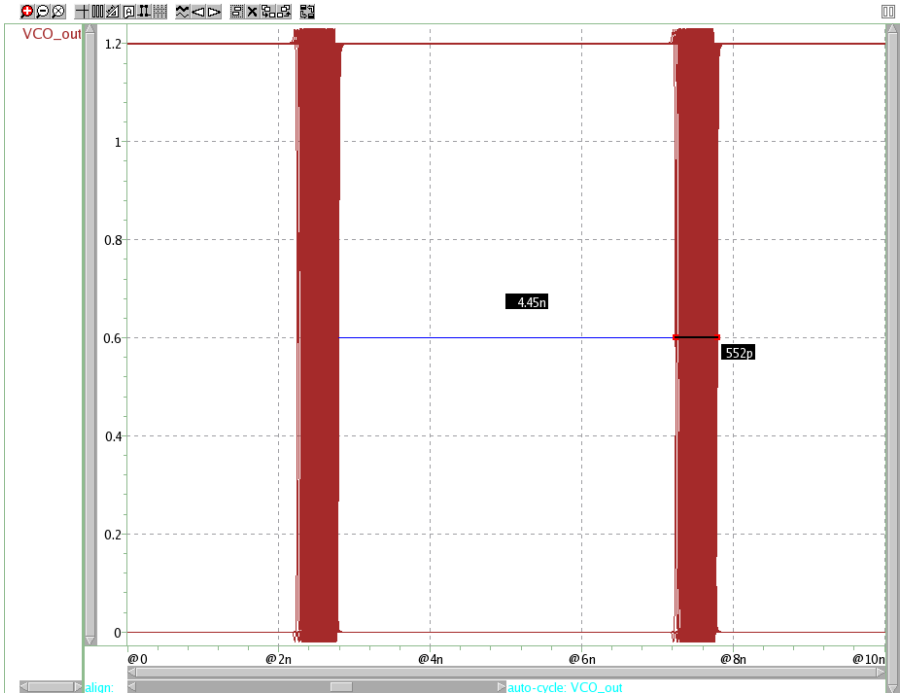


Figure 35 Eye diagram with transient noise enabled VCO oscillating at 100MHz.

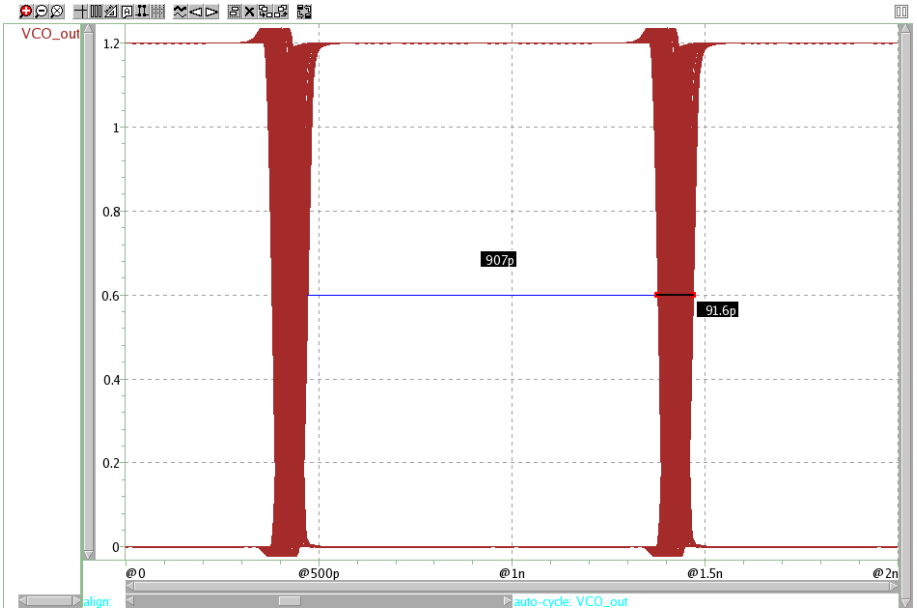


Figure 36 Eye diagram with transient noise enabled VCO oscillating at 500MHz.

Table 4 Jitter summary.

$VCO\ freq$	$Jitter_{rms}\ spec.$	$Jitter_{p-p}\ spec.$	$Calculated\ Jitter_{rms}$	$Simulated\ Jitter_{p-p}$
$100\ MHz$	$20\ ps$	$281.4\ ps$	$45.2\ ps$	$553\ ps$
$500\ MHz$	$4\ ps$	$56.3\ ps$	$12.6\ ps$	$91.6\ ps$

4.4 Power Consumption

RMS current for each circuit blocks at steady-state are calculated and plotted in pie chart. Total current consumption for the PLL operating at 100 MHz and 500 MHz are 4.45 mA and 6.46 mA, respectively.

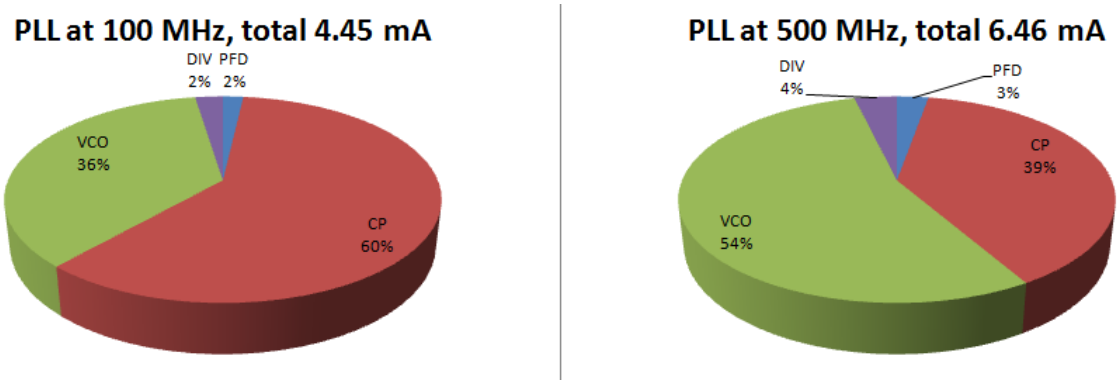


Figure 37 PLL current consumption at 100 MHz and 500 MHz.

5 Conclusions

A type-II 3rd-order charge-pump PLL is systematically studied and simulated in this work. It's easy to make a PLL lock, but fast-locking, low-noise, low-power, wide-range PLL is not easy to design, especially at lower operating supply voltages.

6 References

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