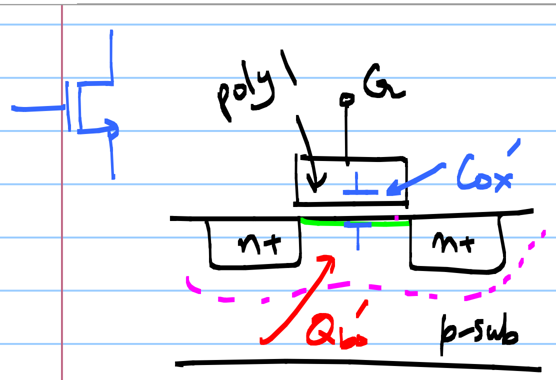
ECE 518 - Lecture 7

Note Title 2/12/2013

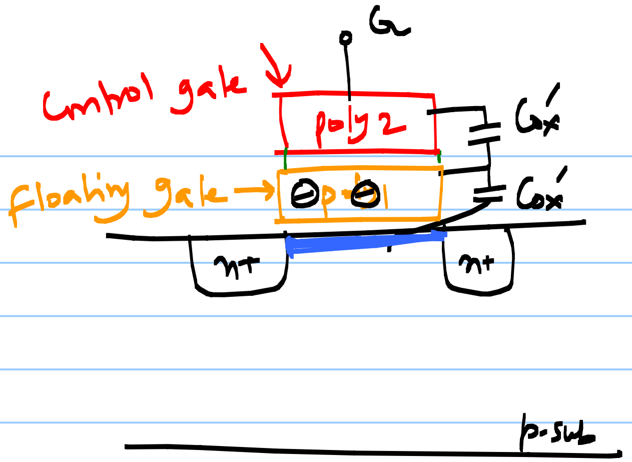


$$V_{THN} = \underset{\substack{\uparrow \\ \text{work function} \\ \text{difference}}}{-V_{ms}} \underset{\substack{\uparrow \\ f(N_A)}}{-2V_{fp}} + \frac{Q'_{bo}}{C'_{ox}} - \cancel{\frac{Q'_{ss}}{C'_{ox}}} + \cancel{\frac{Q'_{c}}{C'_{ox}}}$$

$$\phi = -V_{fp}$$

$$Q'_{bo} = \sqrt{2qN_A\varepsilon_{si}\underbrace{|-2V_{fp}|}_{\phi}}$$

$$V_{THN} = -V_{ms} - 2V_{fp} + \frac{Q'_{bo}}{C'_{ox}}$$



$\frac{C'_{ox}}{2}$

Erased device

$$\Rightarrow V_{THN,\,erased} = -V_{ms} - 2V_{fp} + \frac{2\,Q'_{bo}}{C'_{ox}}$$

$$= \left(-V_{ms} - 2V_{fp} + \frac{Q'_{bo}}{C'_{ox}}\right) + \underbrace{\frac{Q'_{bo}}{C'_{ox}}}_{50\,mV}$$

$t_{ox} = 100\ \text{Å}$

$*$ trap e^{-}s in poly 1 FG

$$V_{THN,\,prog} = -V_{ms} - 2V_{fp} + 2\left[\frac{Q'_{bo}}{C'_{ox}} + \underbrace{\frac{|Q'_{poly1}|}{C'_{ox}}}\right]$$

EPROM → Electrically programmable ROM

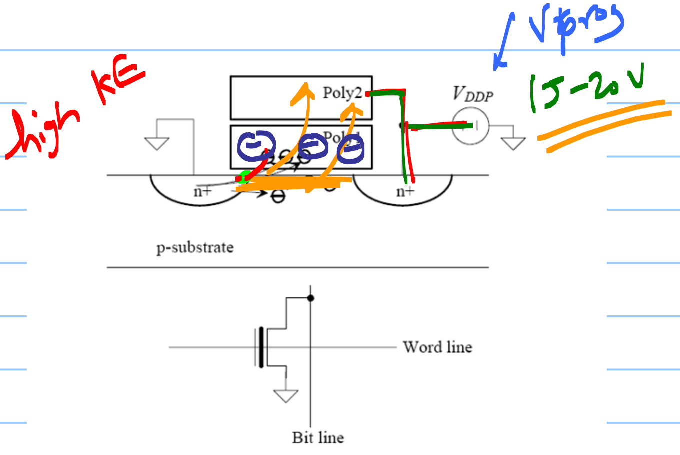


Figure 16.56 How charge is trapped on the floating gate using channel hot electron (CHE) injection.

CHEI

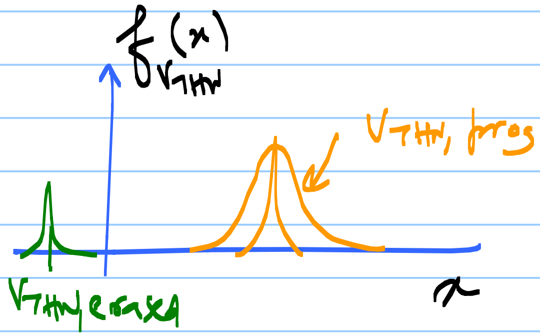
channel hot electron injection

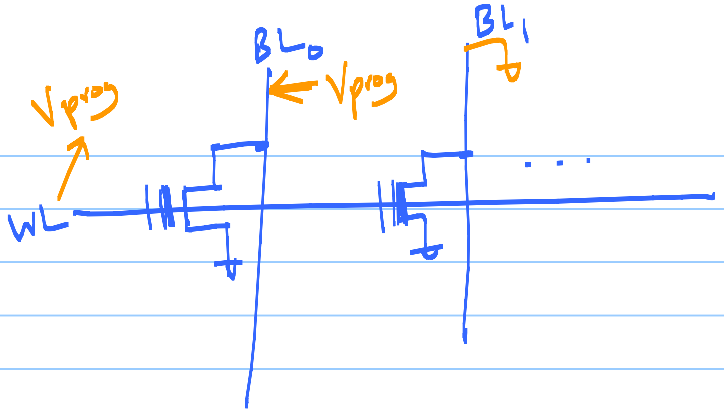
* lucky electron model

CHEI $V_{prog} \Rightarrow V_{THN} \uparrow$

$I_D \downarrow$

* self-limiting programming





* In a CHE, both drain and gate terminals need to be at a high voltage during programming.

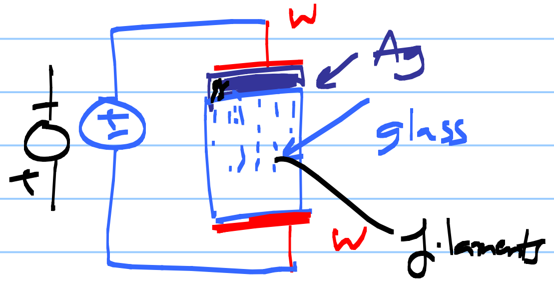
E^2PROM → FNT

↳ Flash

- → NOR ← code / data
- → NAND (SSD) → FNT prog & erase
- → erase large amount of data as an "array" block.

Fowler Nordheim Tunneling (FNT)

Aside



ion-conducting chalcogenide memories

Programming

* triple-well process

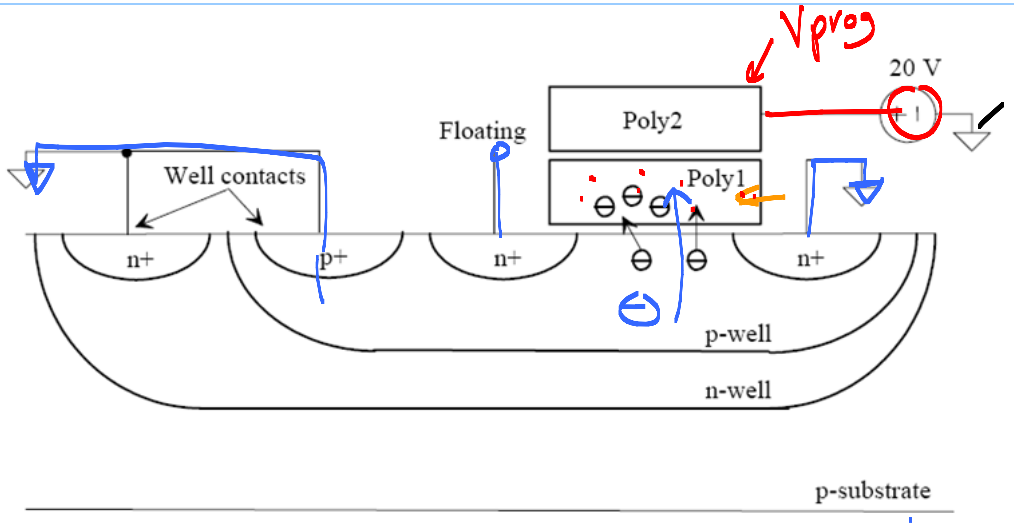


Figure 16.58 FNT of electrons from the p-well to a floating gate to increase threshold voltage (showing programming).

Erase

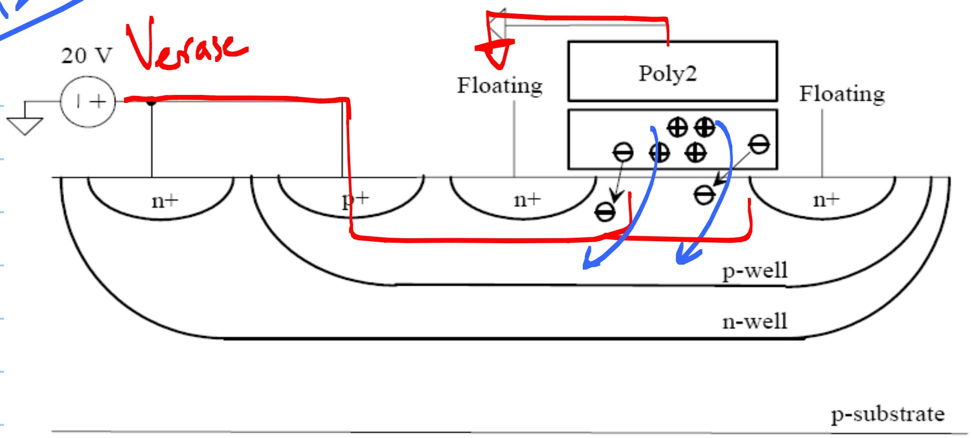


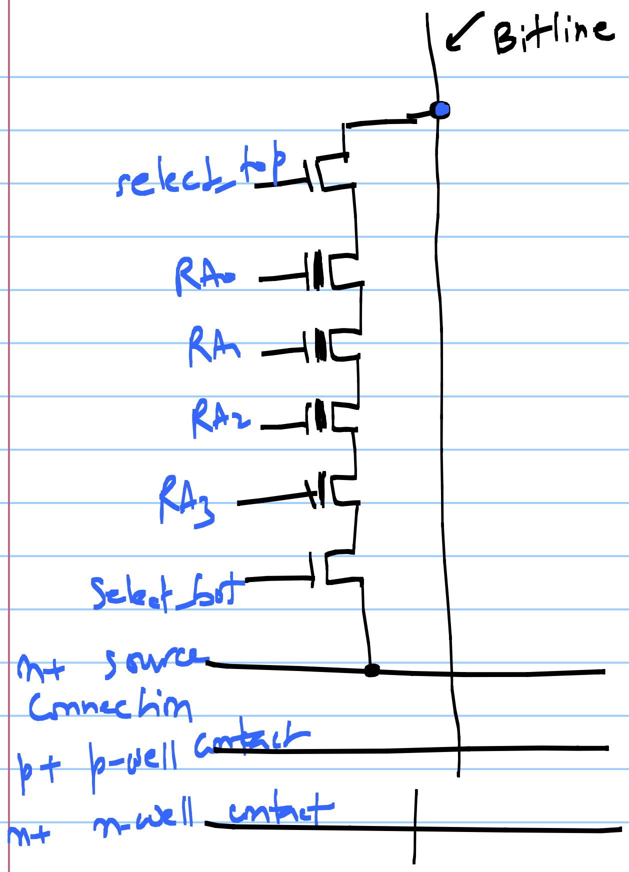
Figure 16.59 FNT of electrons from the floating gate to p-well to decrease threshold voltage (showing erasing).

FNT

⇒ Over erase

4-bit NAND

"higher density"



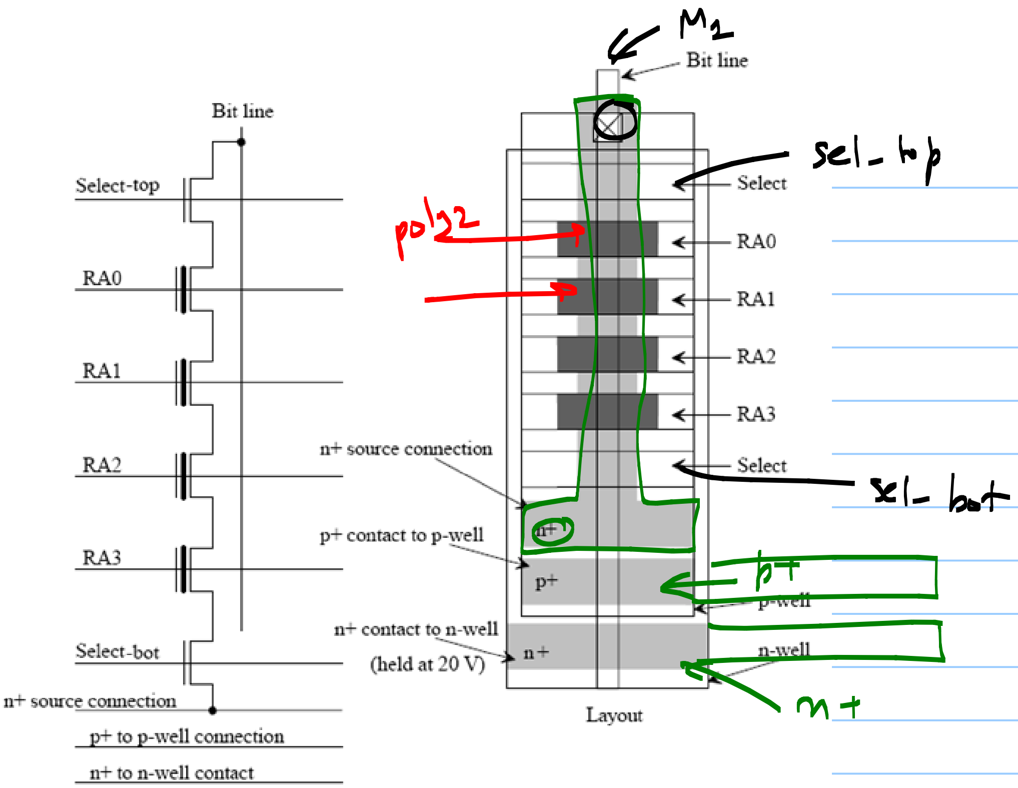
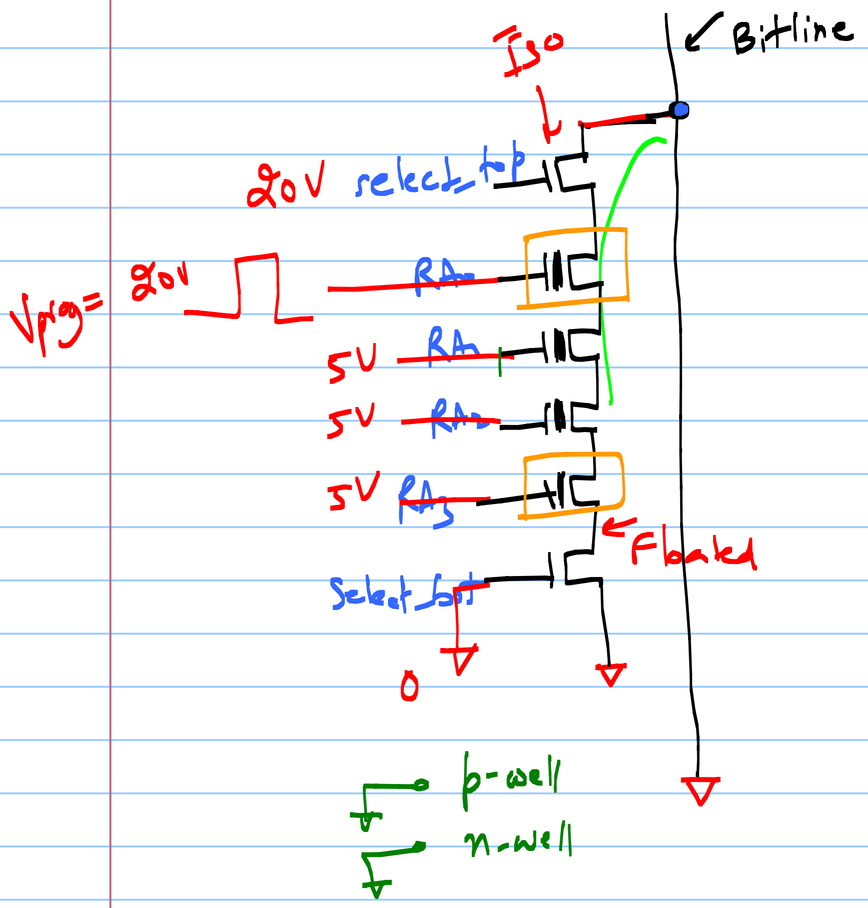


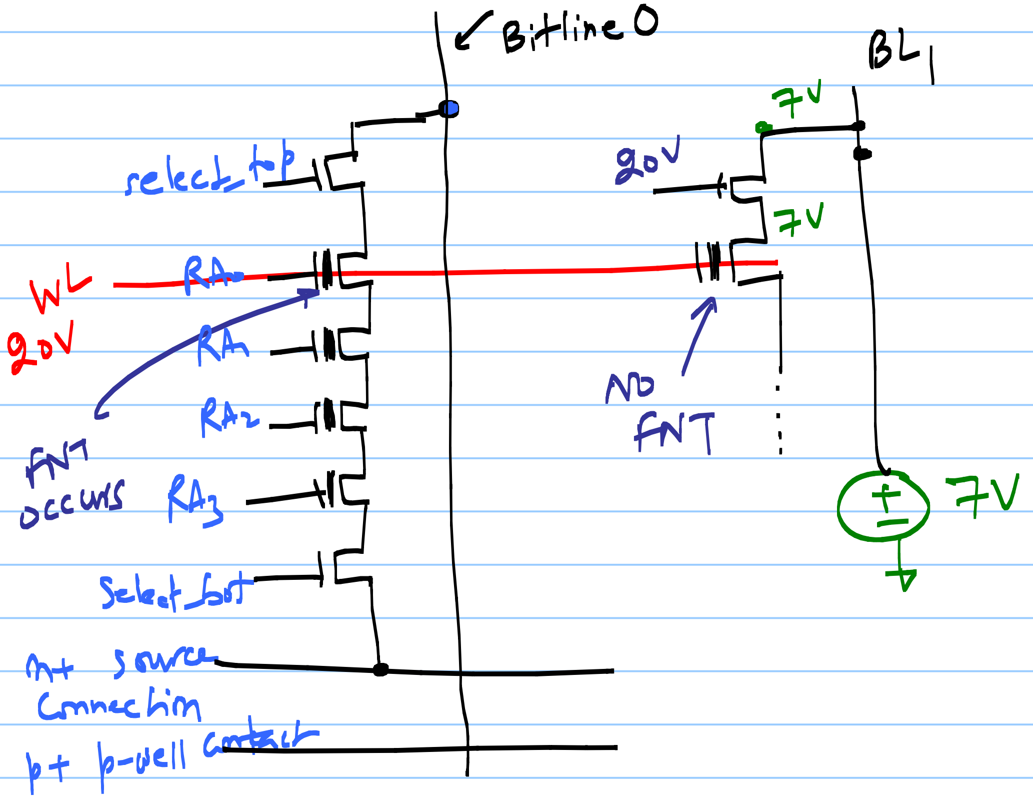
Figure 16.61 A 4-bit NAND Flash memory cell.

Program

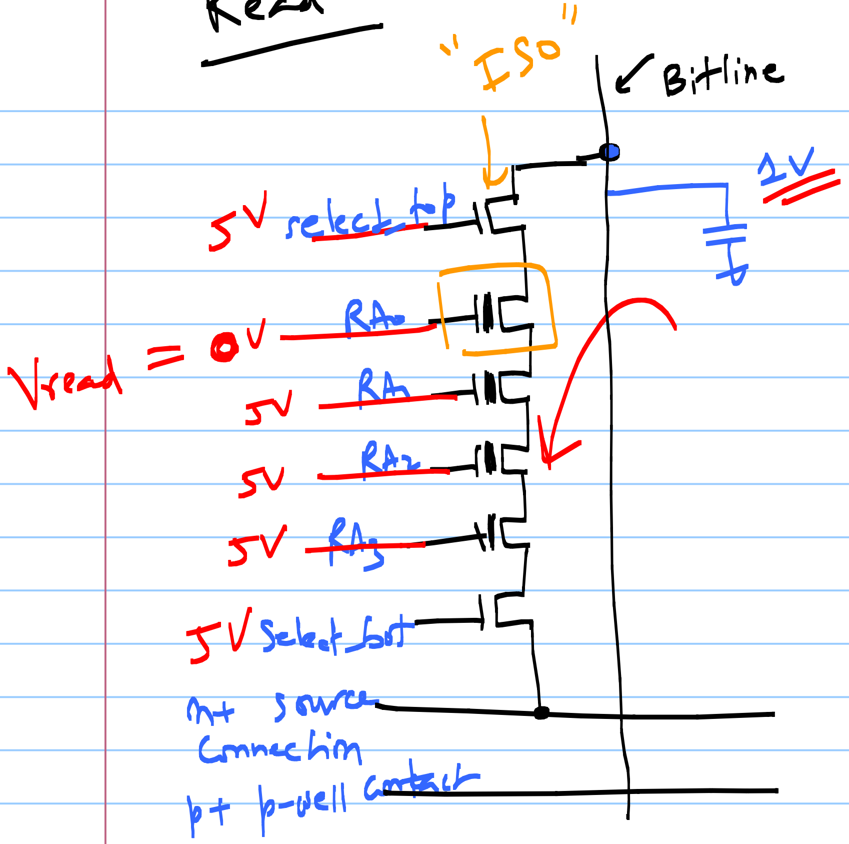


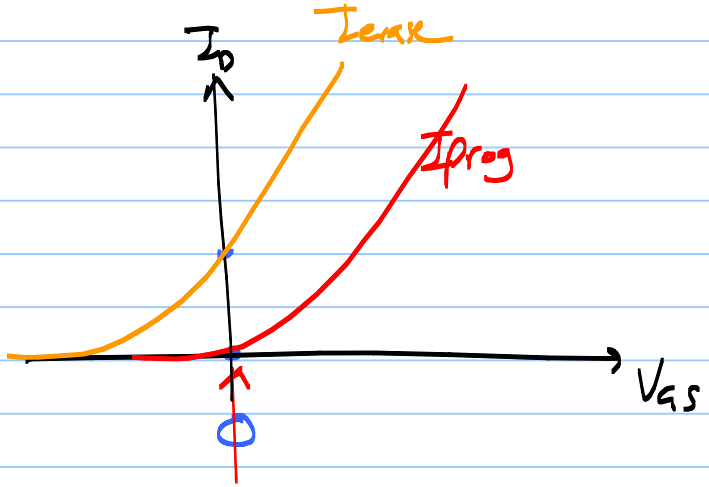
"64 – 128
NAND String"

"Disturb"

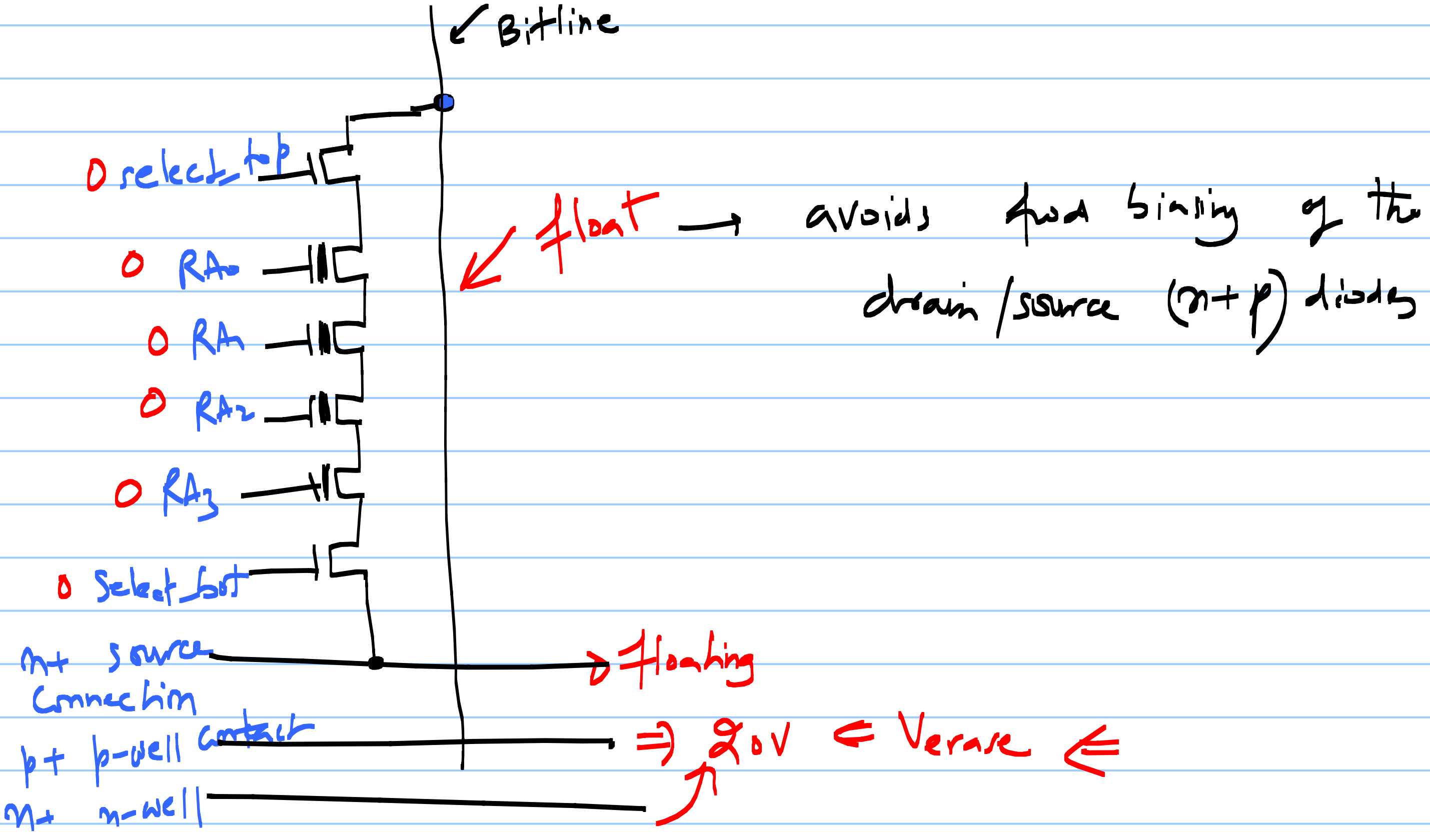

Bitline 0
BL1
7V
20V
7V
select_top
WL
20V
RA0
RA1
RA2
FNT occurs
RA3
Select_bot
NO FNT
7V
n+ source Connection
p+ p-well contact

Read


"ISO"
Bitline
1V
5V select top
RA0
Vread = 0V
5V RA1
5V RA2
5V RA3
5V Select bot
n+ source connection
p+ p-well contact


I_D
Ierase
Iprog
V_{GS}
0

Erase



float → avoids fwd biasing of the drain/source (n+p) diodes