ECE 518 – Lecture 6

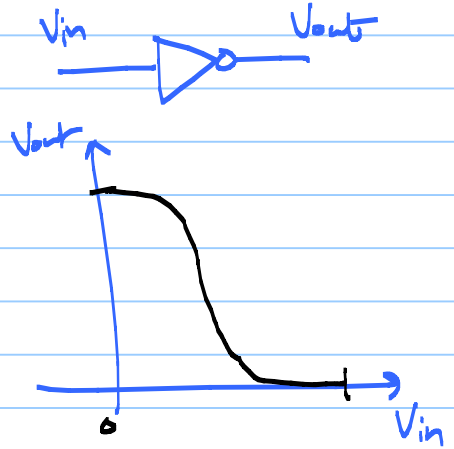
Note Title 2/7/2013

NMOS PMOS

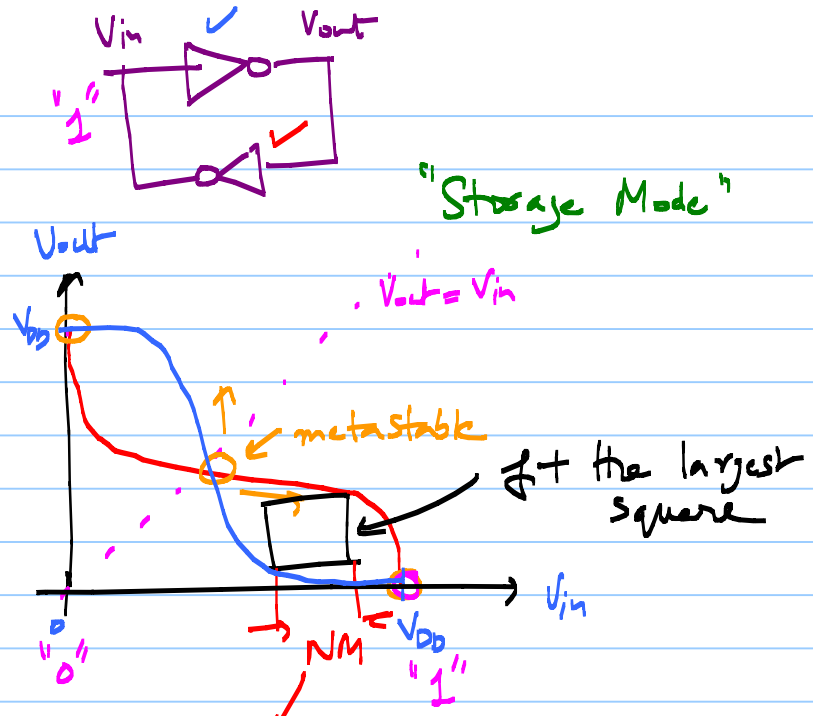
$\beta_{pull\text{-}down} > \beta_{access} > \beta_{pull\text{-}up}$

readable writable

SRAM Cell Noise Margin



"Butterfly curves"

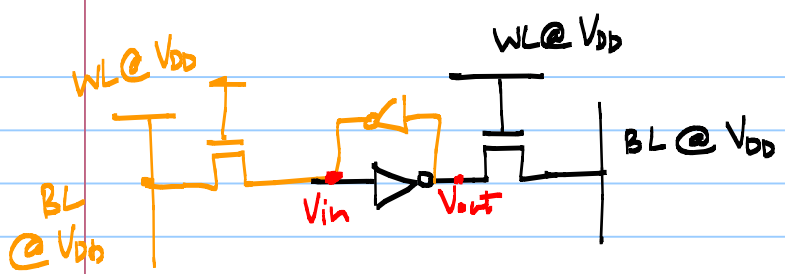


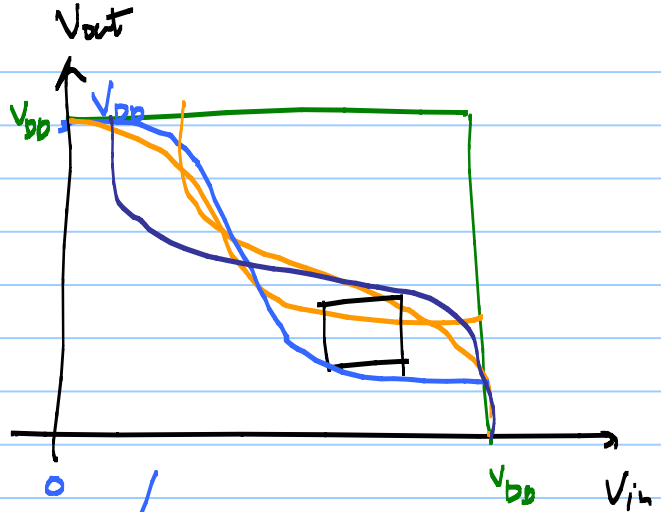
"Static noise margin"

↳ the larger the better

"Read Mode"

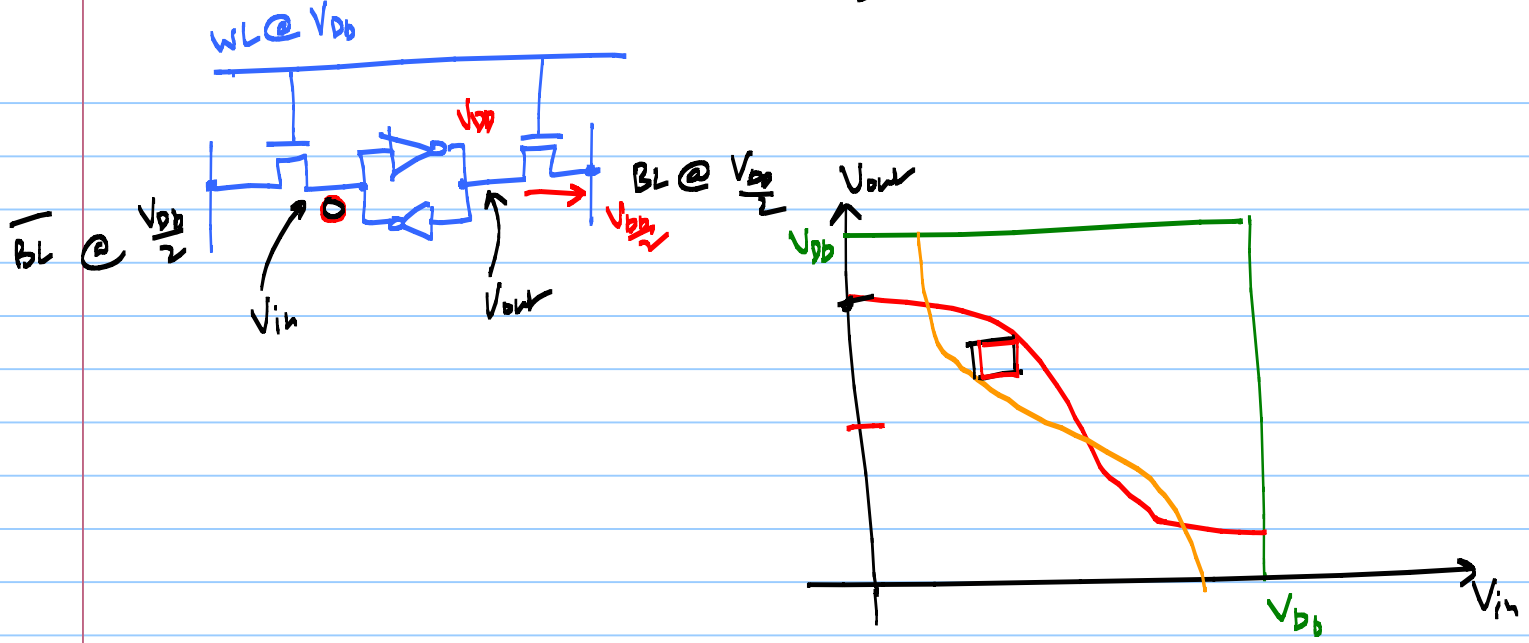
"Monte Carlo"



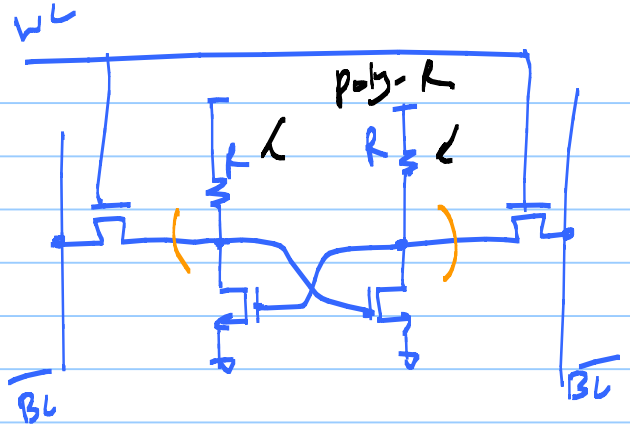


Read Butterfly curve

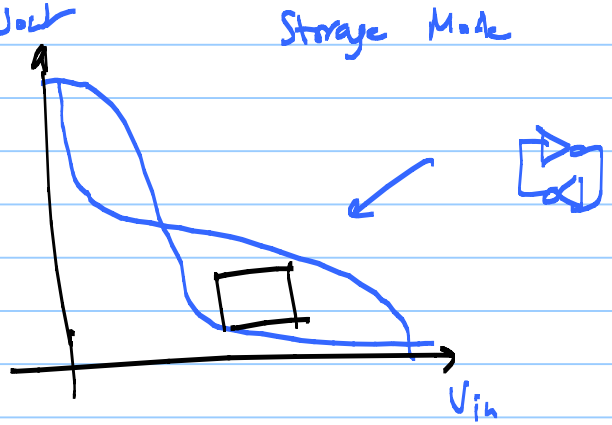
BL's are precharged at $\frac{V_{DD}}{2}$, Read



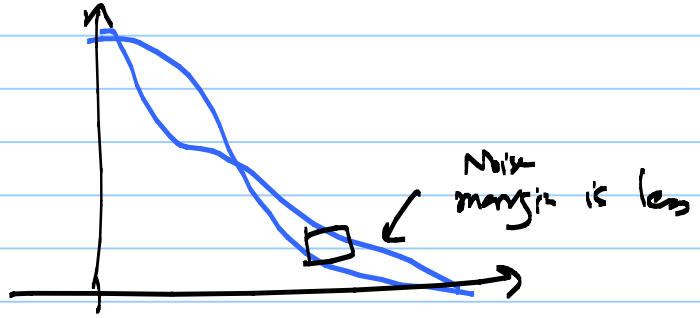
4T Cell SRAM



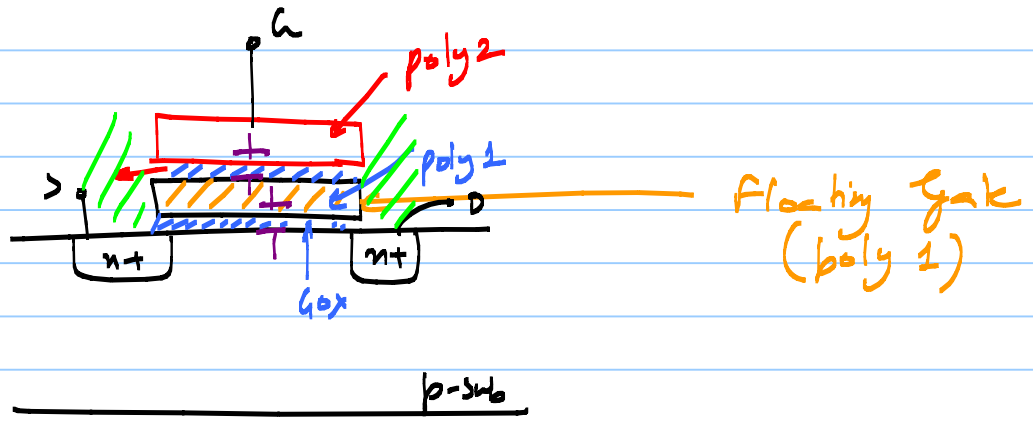
(-) leakage current



"Read mode"



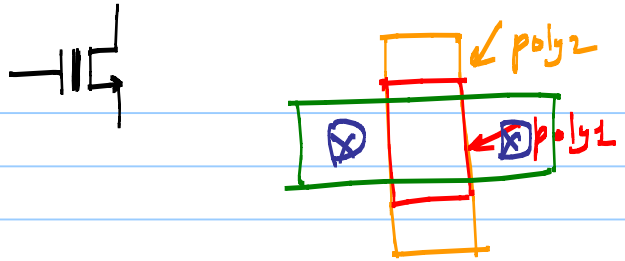
Floating Gate Memory :

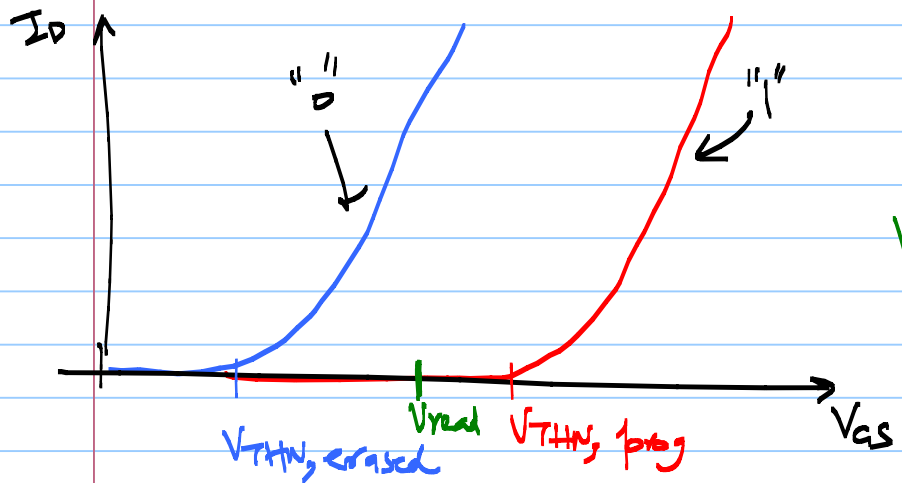


* poly 1 is floating → not electrically connected

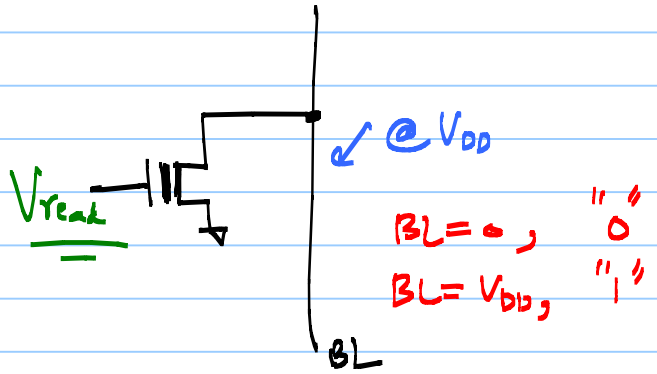
* poly 2 ⇒ Controlling gate of this transistor

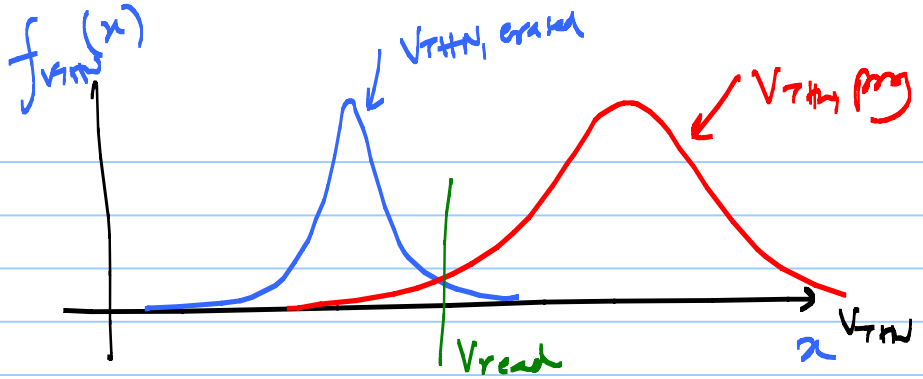
↳ we can store information (memory) by changing, adding or removing charge stored in the floating gate


poly2
poly1


I_D
"0"
"1"
$V_{THN,\ erased}$
V_{read}
$V_{THN,\ prog}$
V_{GS}

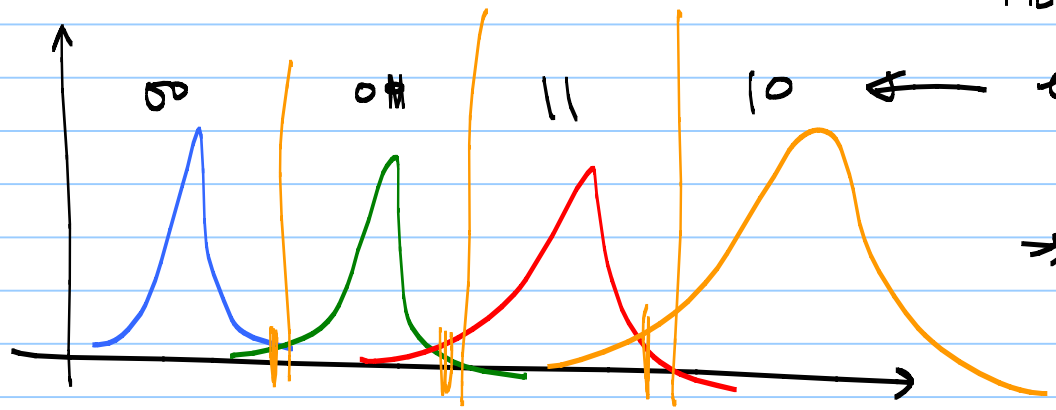
"SPA"


V_{read}
@ V_{DD}
BL = 0, "0"
BL = V_{DD}, "1"
BL



1bit

"MLC"



← Gray Coding

⇒ 2-bit MLC