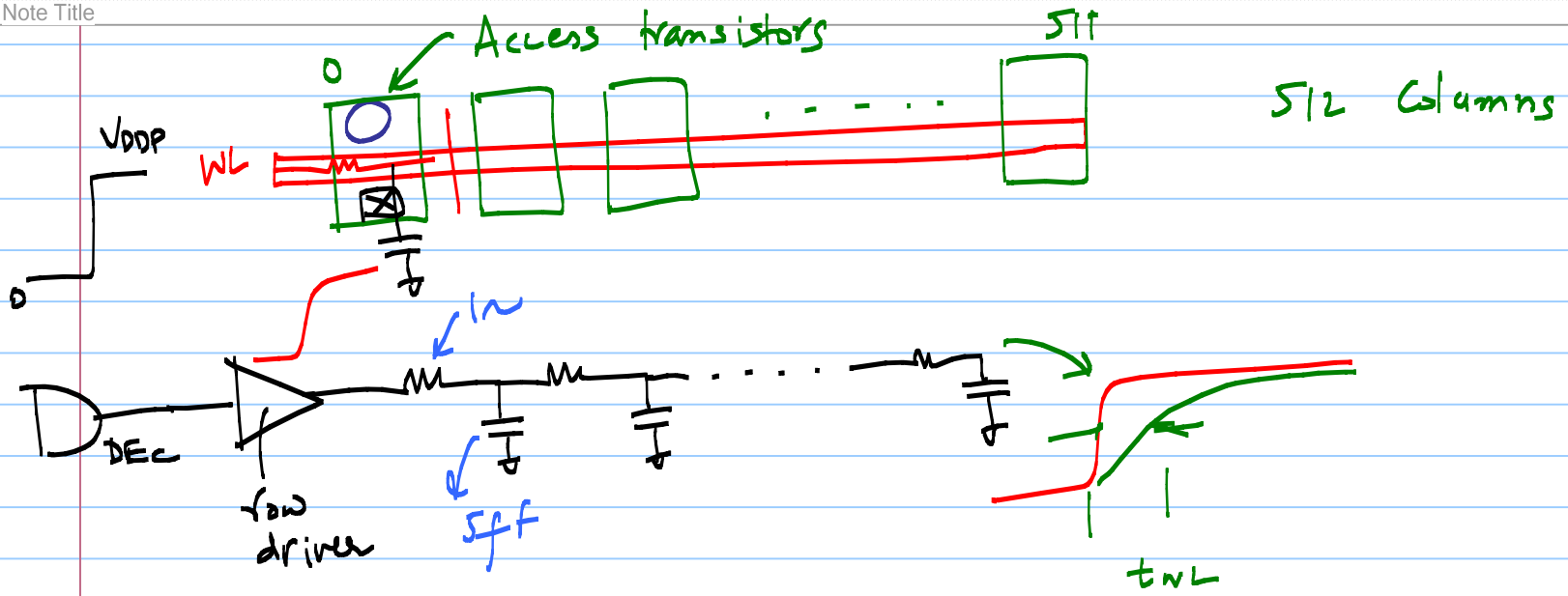
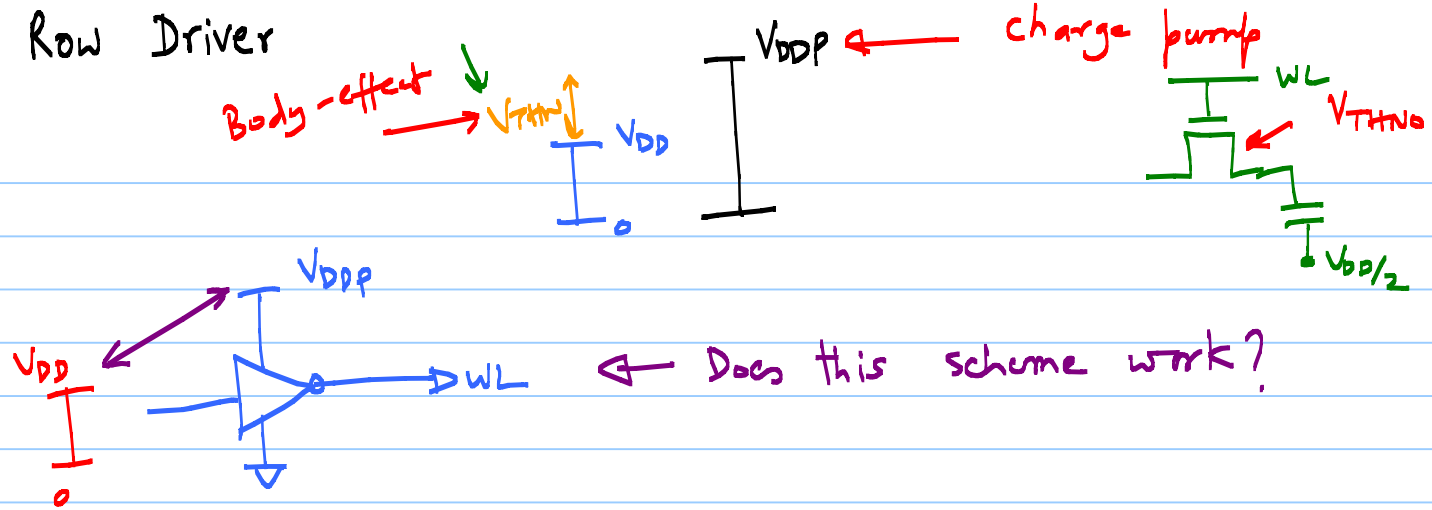
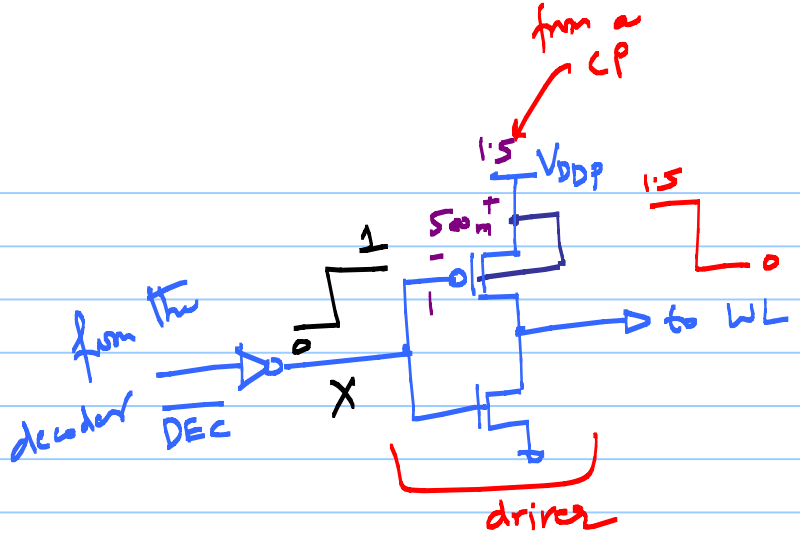
ECE 518 – Lecture 5

Note Title 2/5/2013



Row Driver


Body-effect
V_{THN}
V_{DD}
0
V_{DDP}
charge pump
WL
V_{THNo}
$V_{DD/2}$
V_{DDP}
V_{DD}
WL
0
Does this scheme work?



Example:

Let $V_{DD} = 1V$

$V_{THP} = V_{THN} = 280mV$

$V_{DDP} = 1.5V$ (from a charge pump)

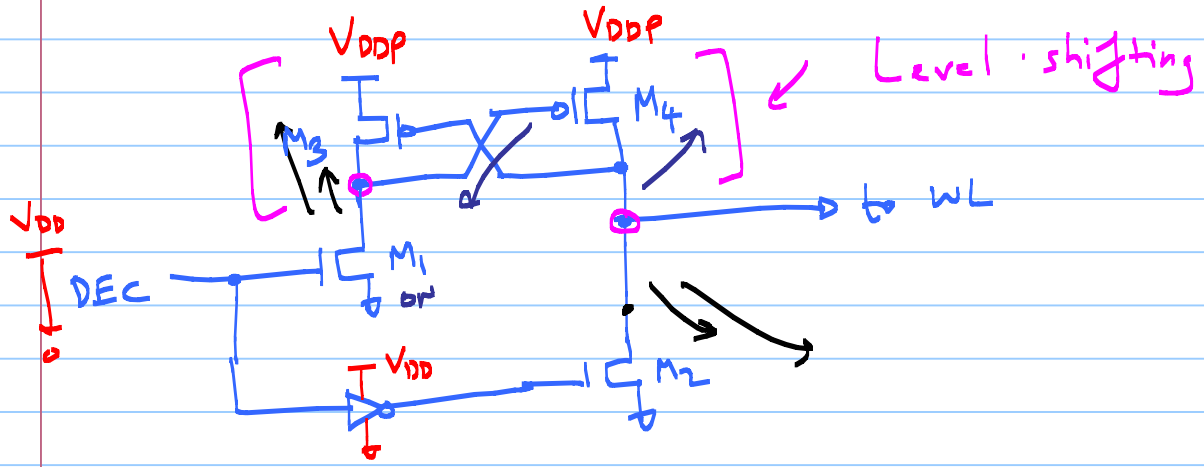
$X=0 \Rightarrow$ WL is driven to V_{DDP} ✓

$X=1 \Rightarrow$ NMOS $\Rightarrow$ ON, PMOS $\Rightarrow$ Can't shut off

$V_{SG} = 0.5V > |V_{THP}|$

Problem!

CMOS drivers :



when DEC = 0 ⇒ M_1 ⇒ OFF, M_2 ⇒ ON (+ve feedback)

⇒ M_3 ⇒ ON

↳ M_4 shuts off ✓

when DEC = 1 ⇒ M_1 = ON, M_2 = OFF

⇒ gate of M_4 is pulled to 0 ⇒ M_4 turns ON

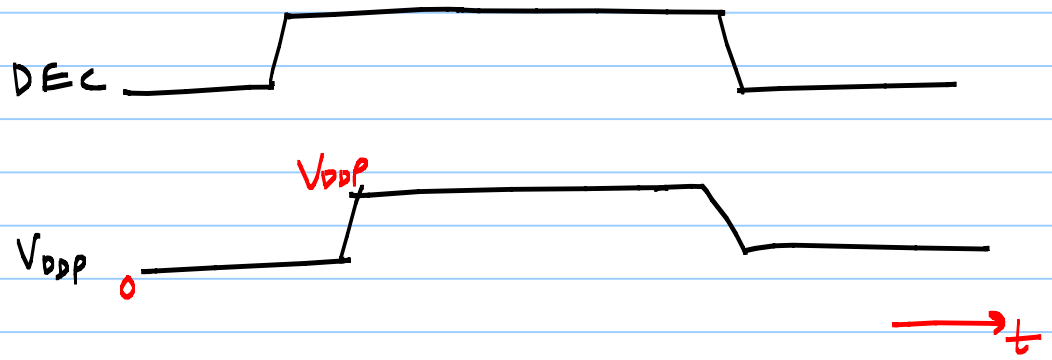
⇒ M_3 shuts off ! ✓

⇒ This circuit works well

↳ ⇔ significant contention current flows when M_3 / M_4 are turning ON

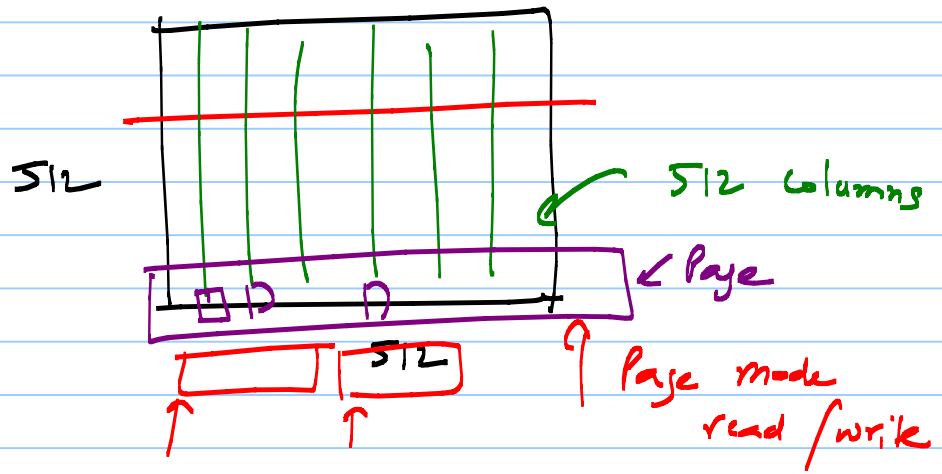
⇒ To avoid this, V_{DDP} can be clocked supply

↳ goes high after the decoder output has transitioned



Page in a DRAM array?

256 kb subarray $\sqrt{2^{18}} = 2^9$



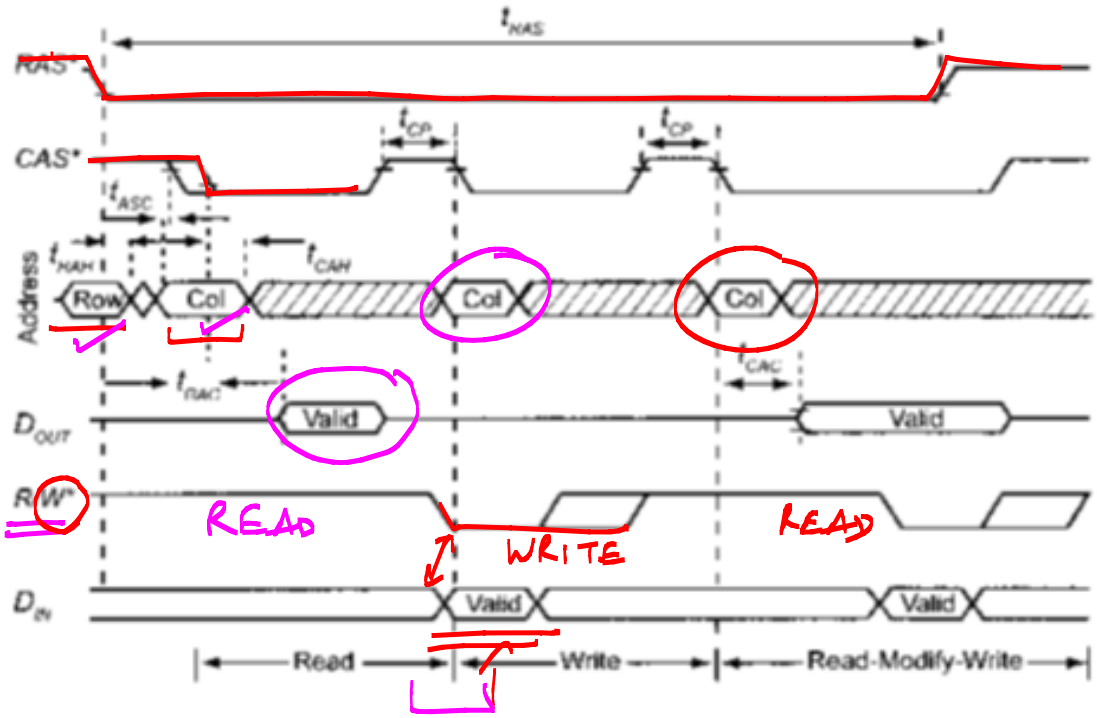
1-bit

RA

CA

4-bit word

⇒ open the WL only once



RAS

CAS

"Page Mode"

SRAM :

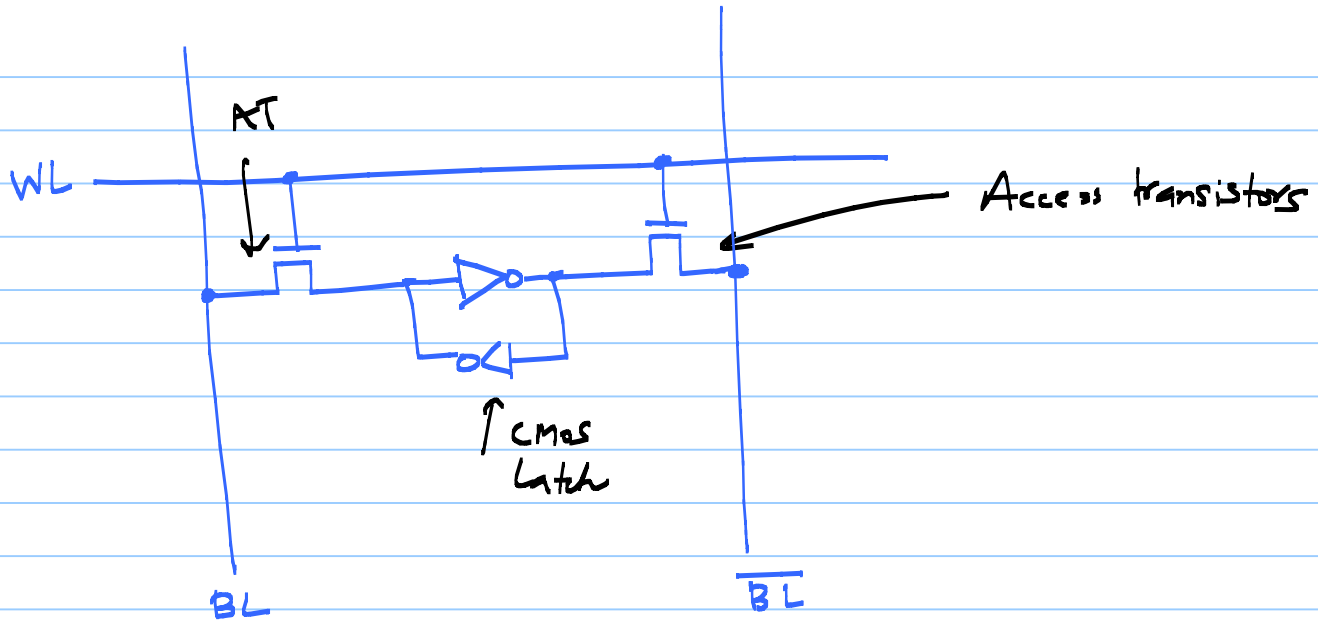
[Processors / Asic → cache

↳ Volatile memory
retains information as long as power is applied
↳ No refreshing needed

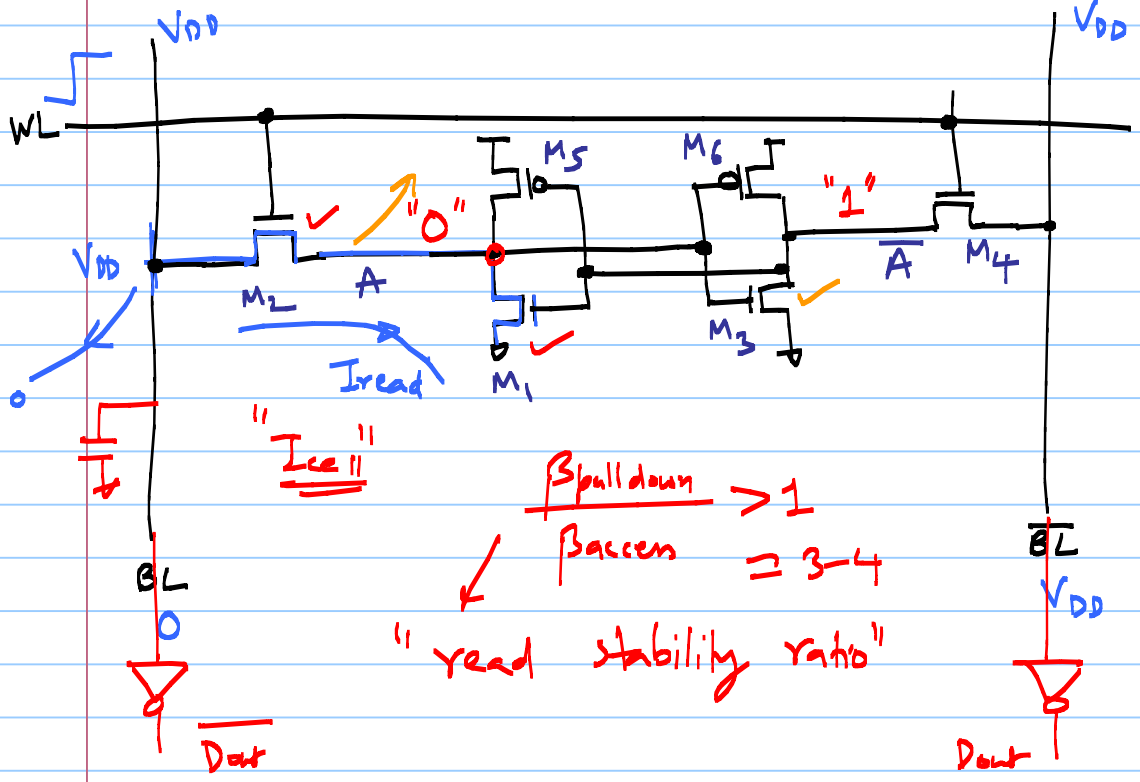
ASIC → Application Specific ICs

6T SRAM Cell

6T SRAM Cell



6T SRAM Read :



* precharge BL, $\overline{BL}$ to VDD and float

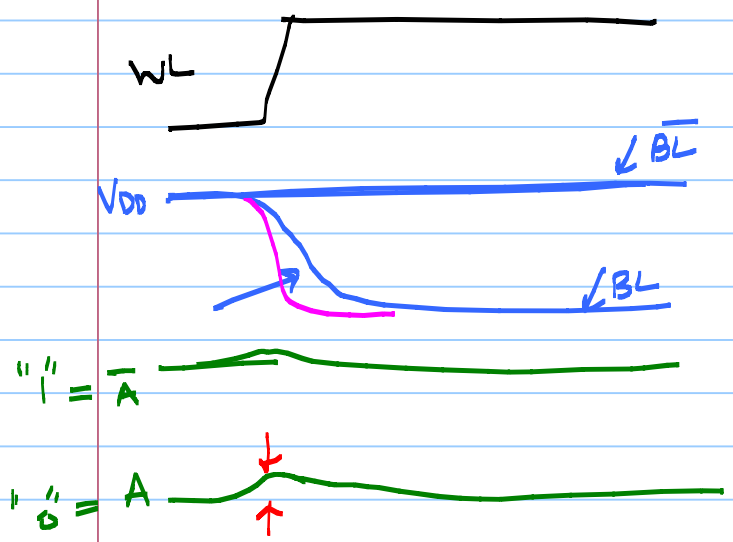
* open the WL

$\frac{\beta_{pulldown}}{\beta_{access}} > 1$ $= 3-4$

↓

"read stability ratio"

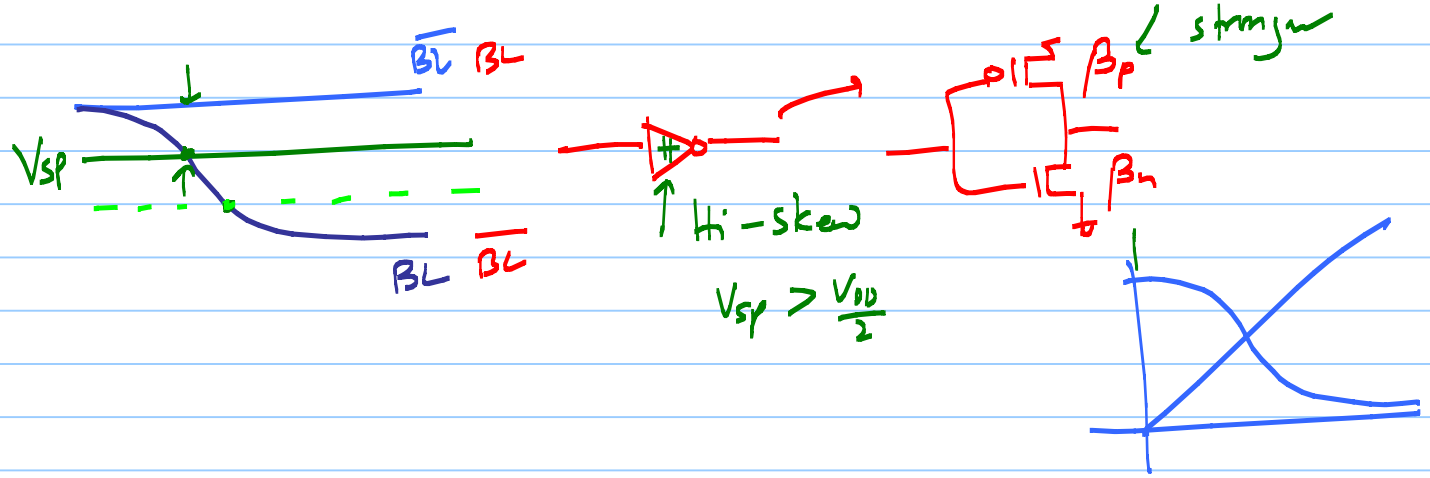
M_1 must be stronger than M_2
↳ node A doesn't trip the second inverter
↳ stable read

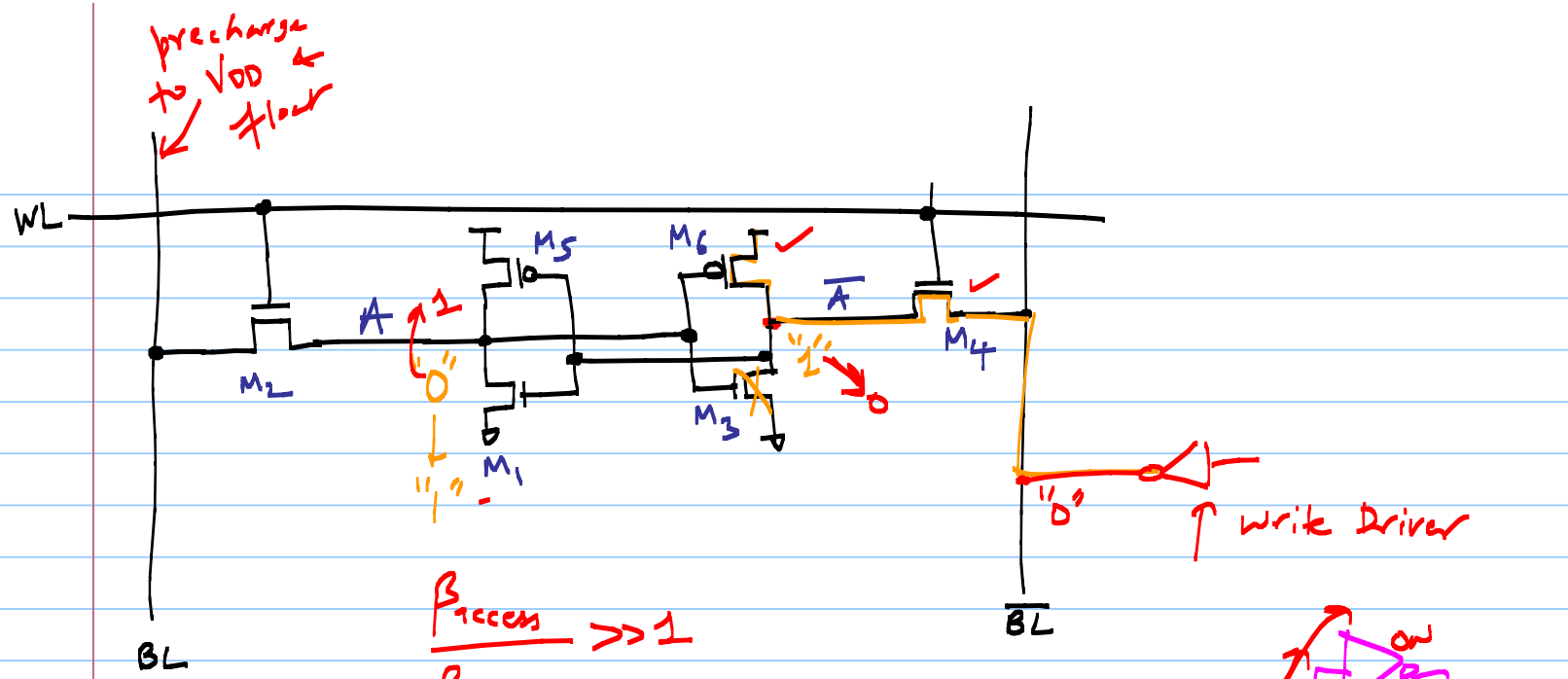


* Can use S/A to speed up the reads

"cell must not be flipped while reading".

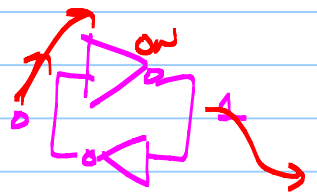
* C_{BL} discharged through the access transitor and pulled by M_2.





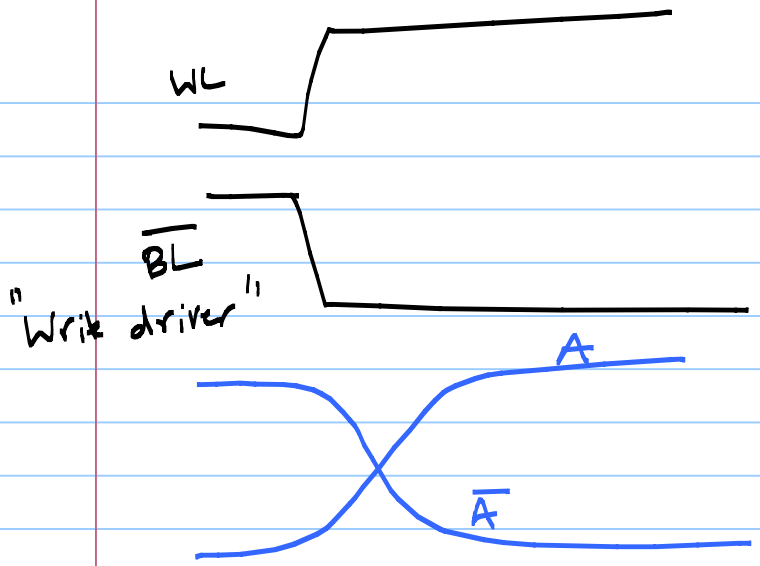
$$\frac{\beta_{access}}{\beta_{pull\text{-}up}} >> 1$$

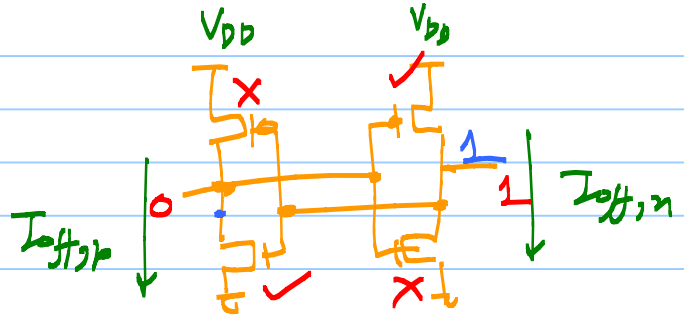
"writeability constraint"



$$\beta_{pull\text{-}down} > \beta_{access} > \beta_{pull\text{-}up}$$

"Write"





$$P_{static} = V_{DD}\left(I_{off,p} + I_{off,n}\right)$$