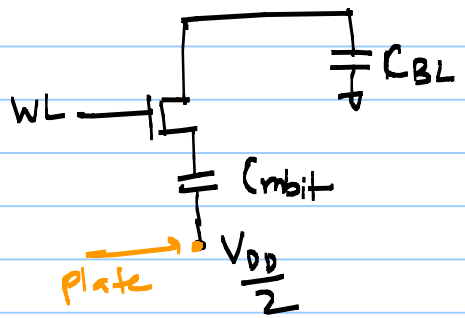
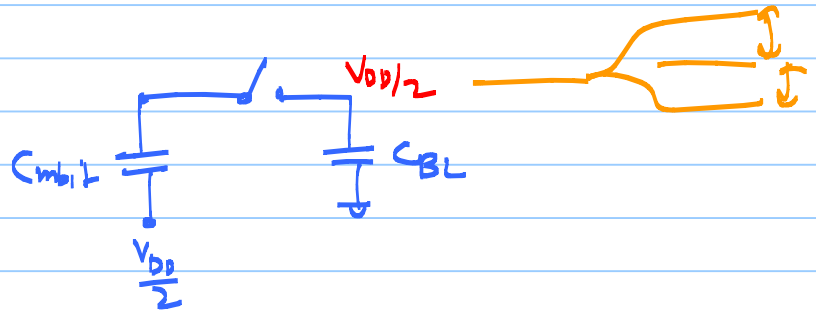
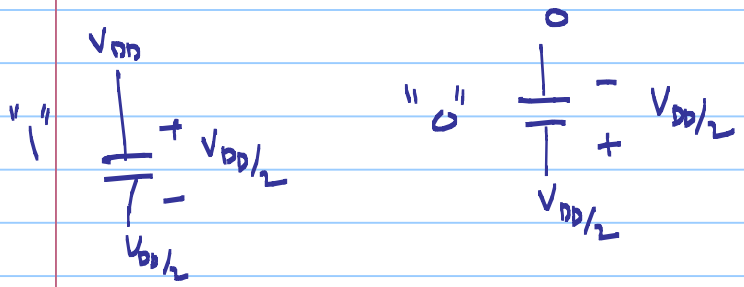
ECE 518 – Lecture 4

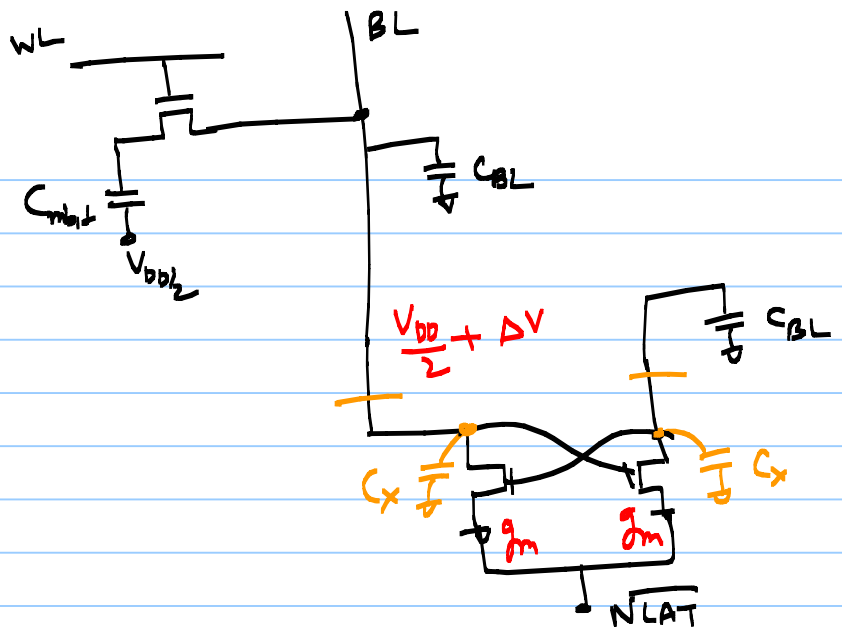
Note Title 1/31/2013





$$\Delta V_{bit} = \pm \frac{C_{mbit}}{C_{mbit} + C_{BL}} \cdot \frac{V_{DD}}{2}$$

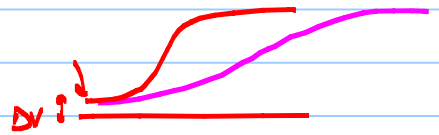


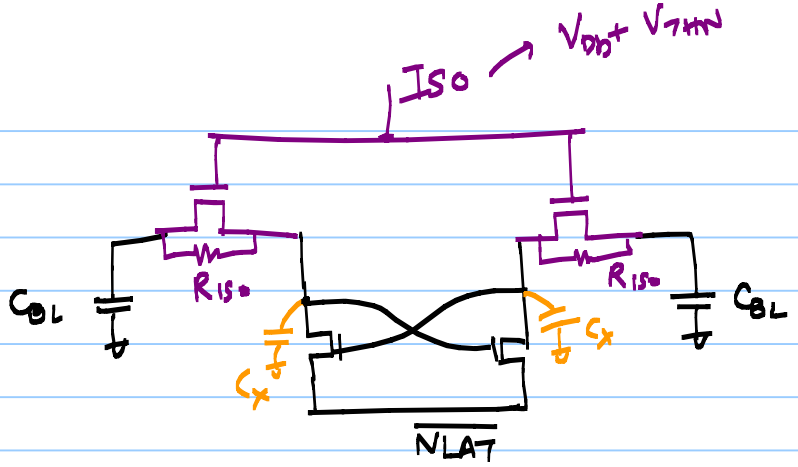


Time-Constant

$\tau = RC$

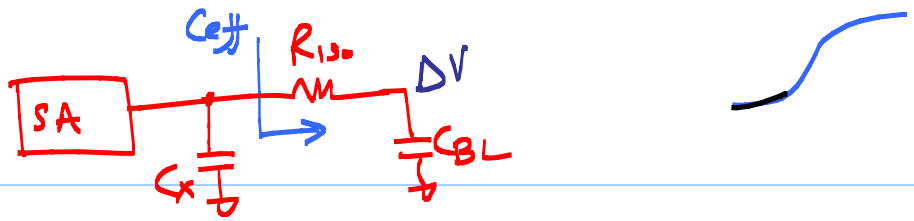
$\tau = \frac{C_x}{g_m}$

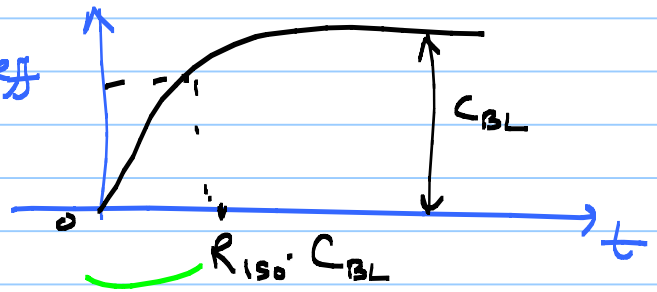




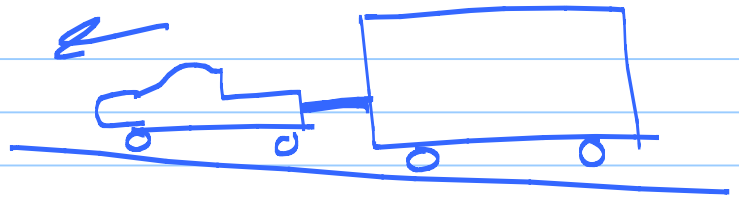
(1) R_{ISO} somewhat isolates the BL from the SA while sensing initially.

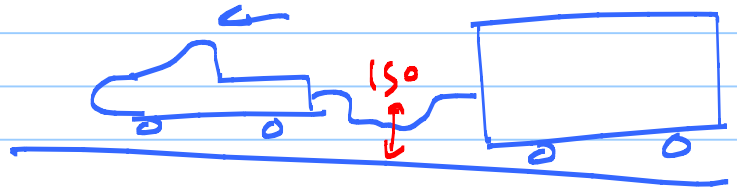
(2) ISO can be used to isolate the S/A from the array.





$$\tau = \frac{C_{SA}}{g_m}$$

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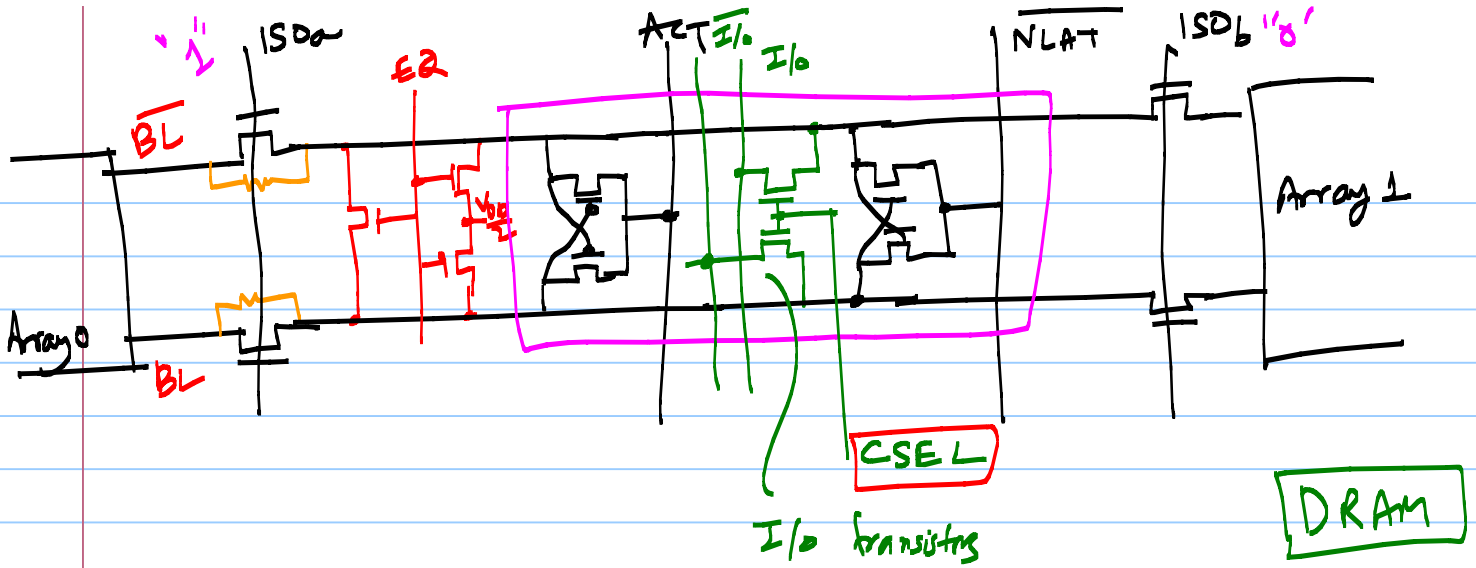
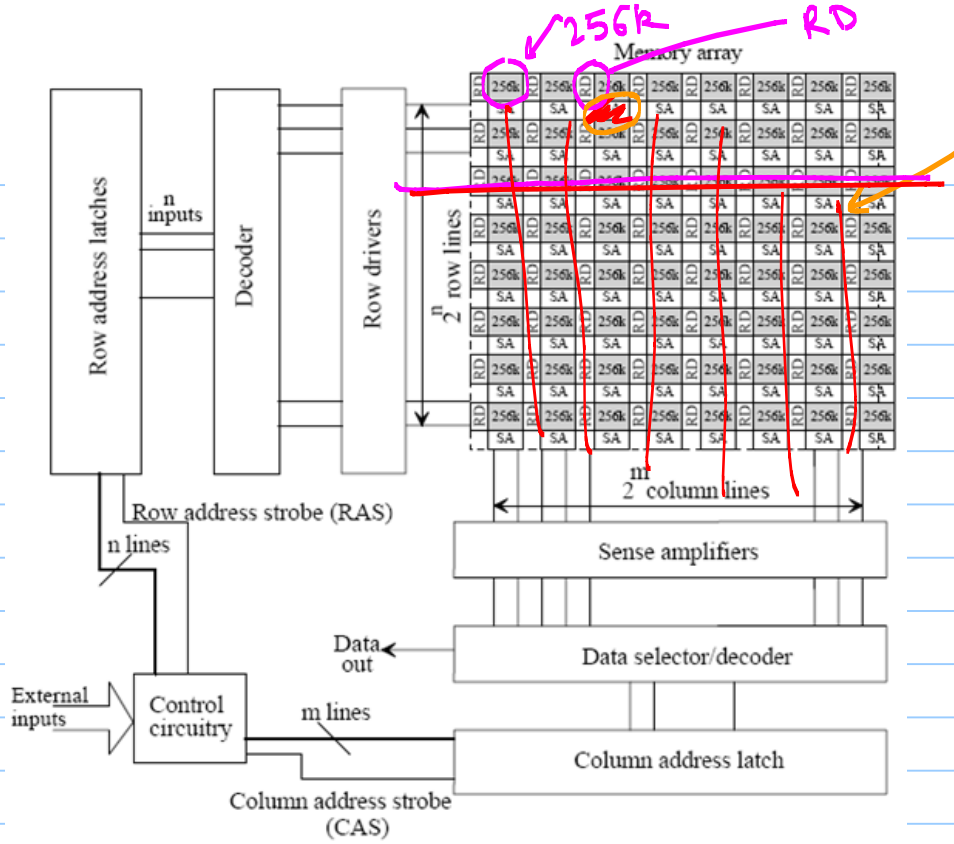

"1"
ISDa
BL
E2
ACT
I/o
I/o
NLAT
ISDb
"0"
Array 1
Array 0
BL
CSEL
I/o transistors
DRAM

256 k bit Sub Array

↳ 2 x 512 WL

512 BL



16 Mb Array block

$2^4 \cdot 2^{20} = 2^{24}$

2^{24}

Figure 16.39 Detailed block diagram of a RAM.

256k x 64 =

$2^8 \cdot 2^{10} \cdot 2^6 = 2^{24} = 2^4 \cdot 2^{20} =$ 16 M

1Gb ⇒ 8 banks of 128 Mb Arrays

$$\text{Area efficiency} = \frac{\text{Area of Memory blocks}}{\text{Total Chip Area}} \Rightarrow 50-60\%$$

Peripheral circuitry → SAs, Row & Col decoders, Row drivers

$1Gb = 2^{30} = 2^{15} \cdot 2^{15}$

15 bit RA, CA

⇒ Row & Column address pin MUXing

$\overline{RAS}$, $\overline{CAS}$

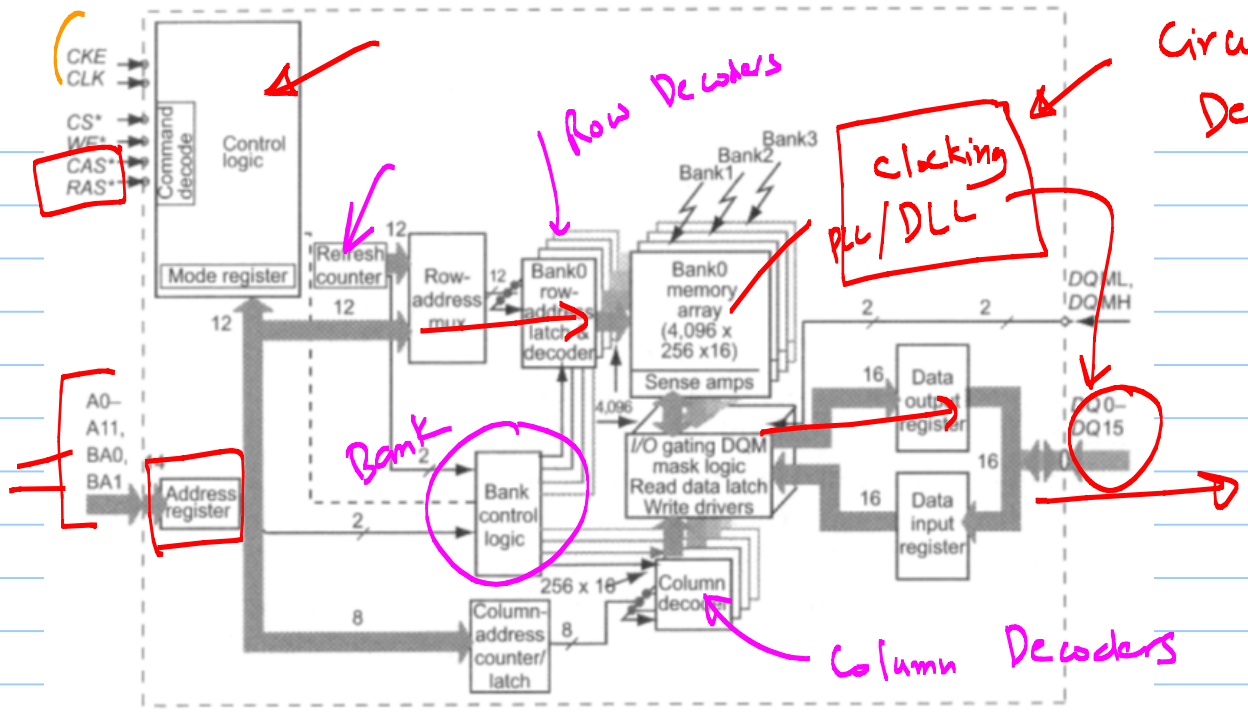


Figure 1.18 Block diagram of a 64Mb SDRAM with 16-bit *I/O*.

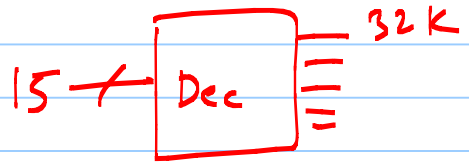
Synchronous DRAM

Global Decoding

$2^{15} \Rightarrow$ 32,768 row wires

* Need another metal layer for routing
  - ↳ process challenges

(+) area efficient



32K ↘ 1 row turns on

↳ drives WL in 64 memory arrays

↳ 32K columns have data sitting on bitline

→ Wastage of power while trying to read a 1bit
↳ 32K columns have data

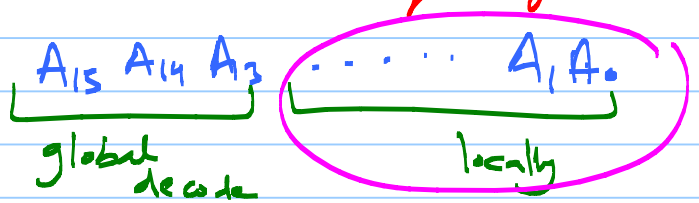
Local decoding

route the address across all the subarrays
↳ locally decode the WL

⇒ every subarray needs a decoder
↳ area inefficient

⇒ doesn't require process complexity

* In practice
↳ Combination of global & local decode



Locally decode 10 bit address

$a[9:0]$

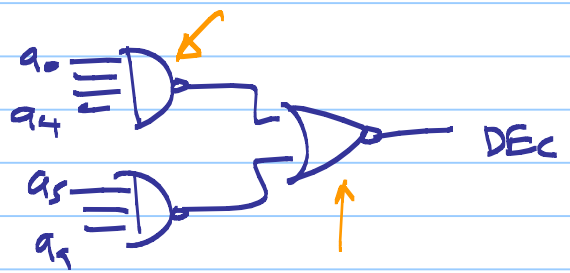
Select

CMOS Static Decoder

$$DEC = \overline{a_0} \cdot \overline{a_1} \cdots \overline{a_9}$$

$$= \overline{a_0 + a_1 \cdots + a_9}$$ NOR

$$= \overline{\overline{a_0 \cdot a_1 \cdots a_4} + \overline{a_5 \cdot a_6 \cdots a_9}}$$



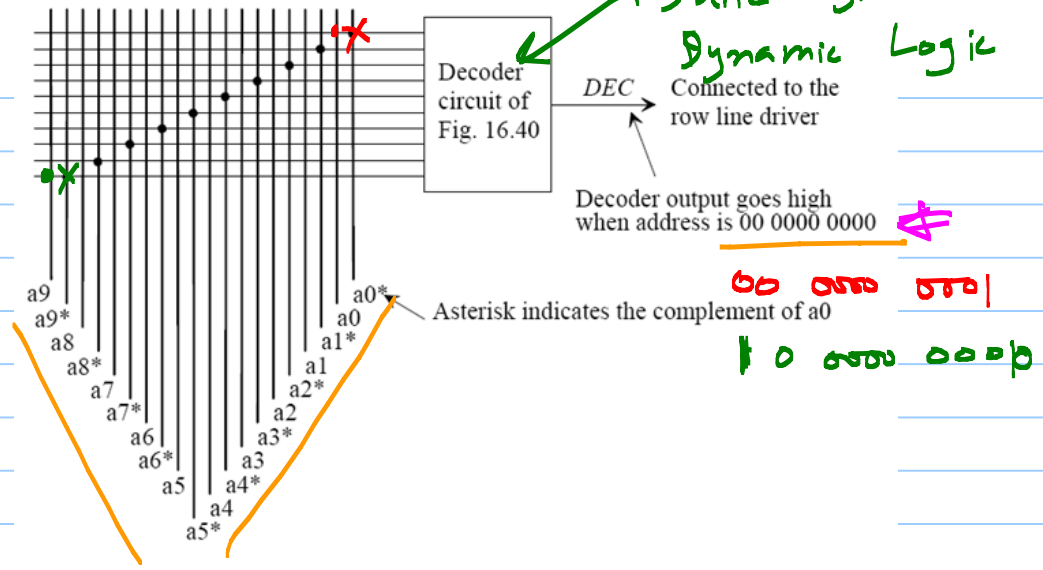
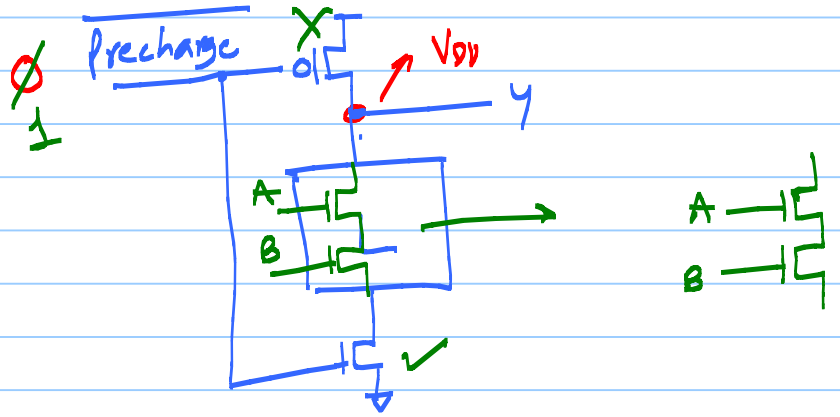


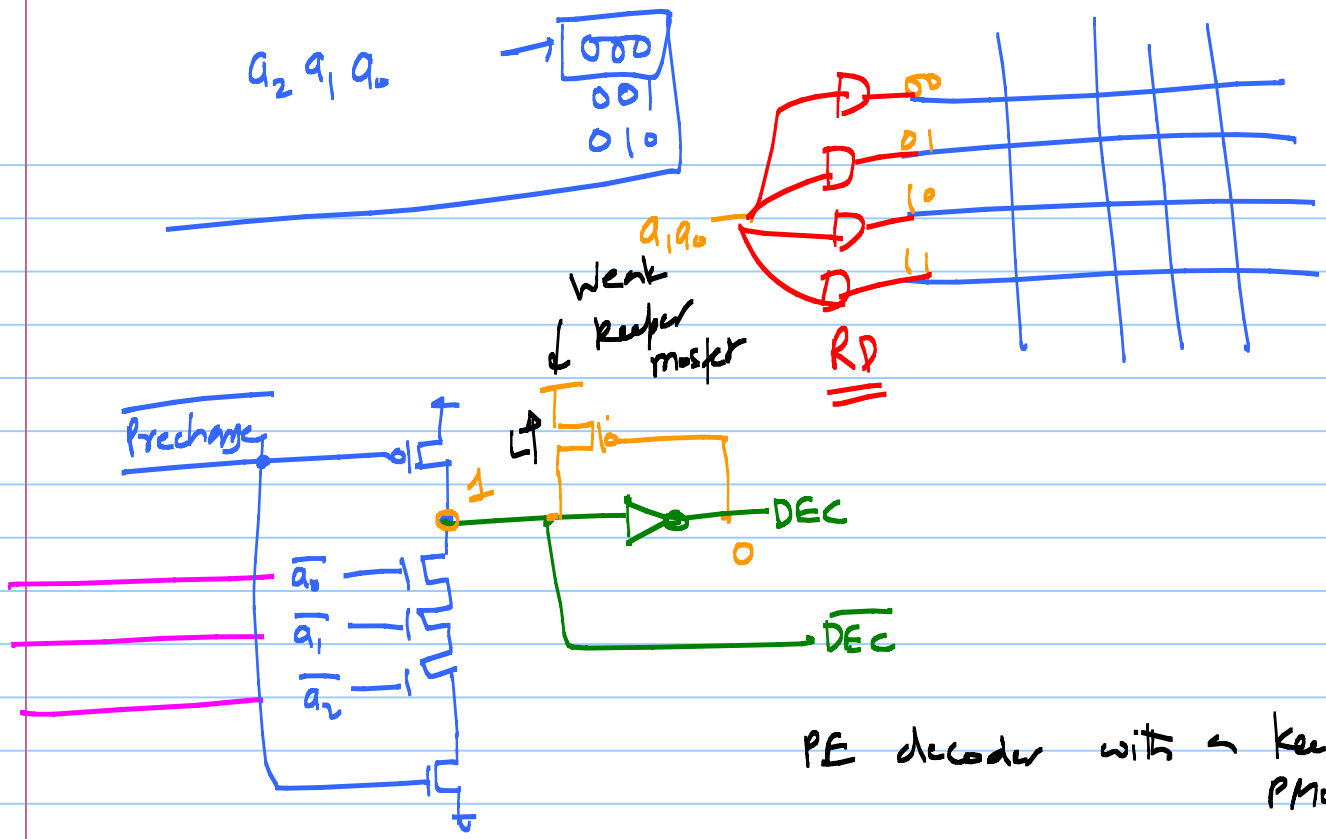
Figure 16.41 How the address lines are connected to a decoder element.

PE Logic

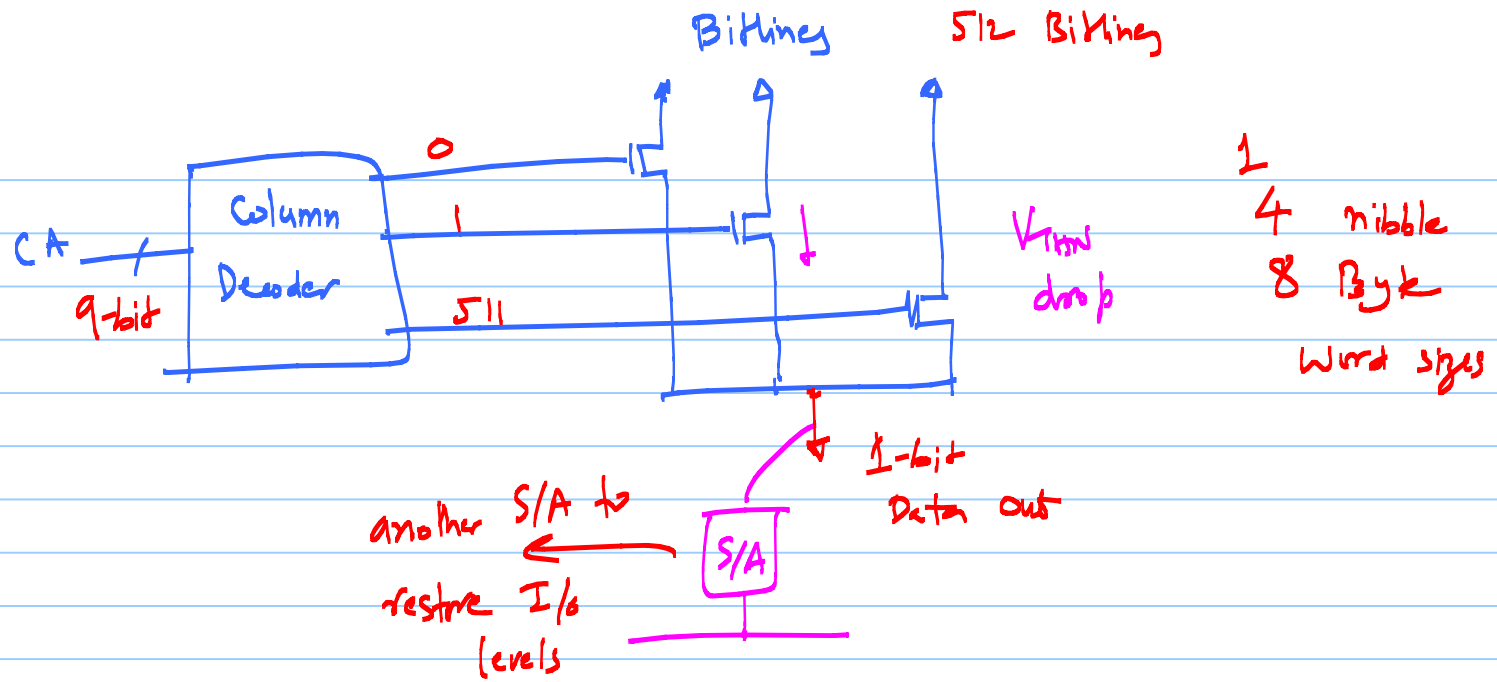
↓ precharge - Evaluate logic

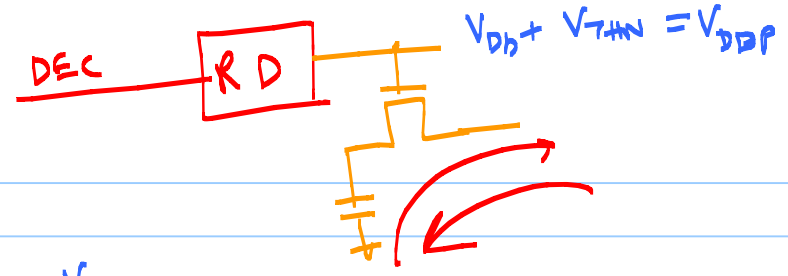
$Y = \overline{AB}$





PE decoder with a keeper PMOS.


Bitline
512 Bitline
0
1
511
CA
9-bit
Column
Decoder
$V_{bitline}$
drop
1
4 nibble
8 Byte
Word size
1-bit
Data out
another S/A to
restore I/O
levels
S/A



"charge pump"

↳ $V_{DDP} > V_{DD}+V_{THN}$