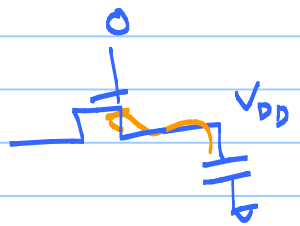
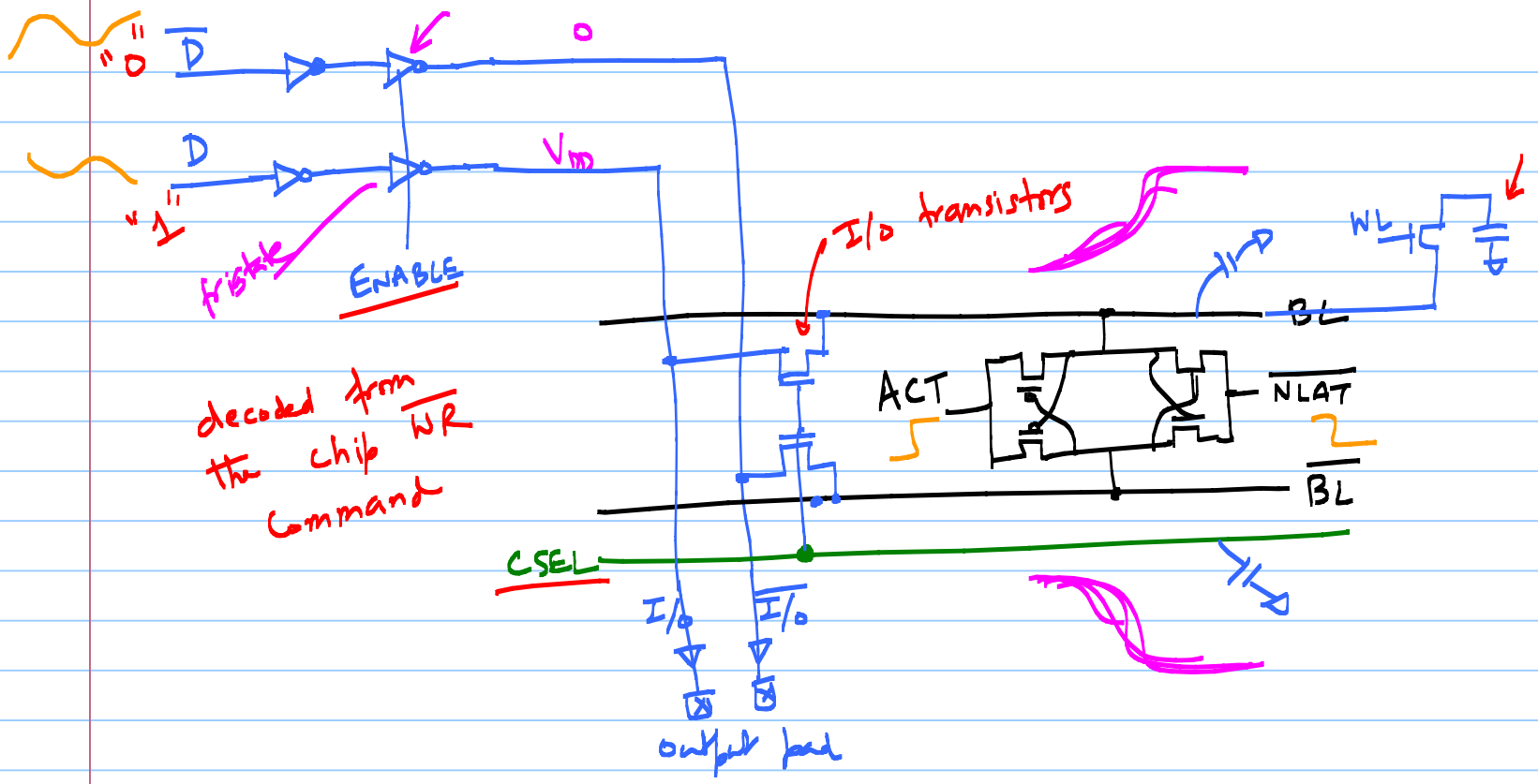
ECE 518 – Lecture 3

Note Title 1/29/2013

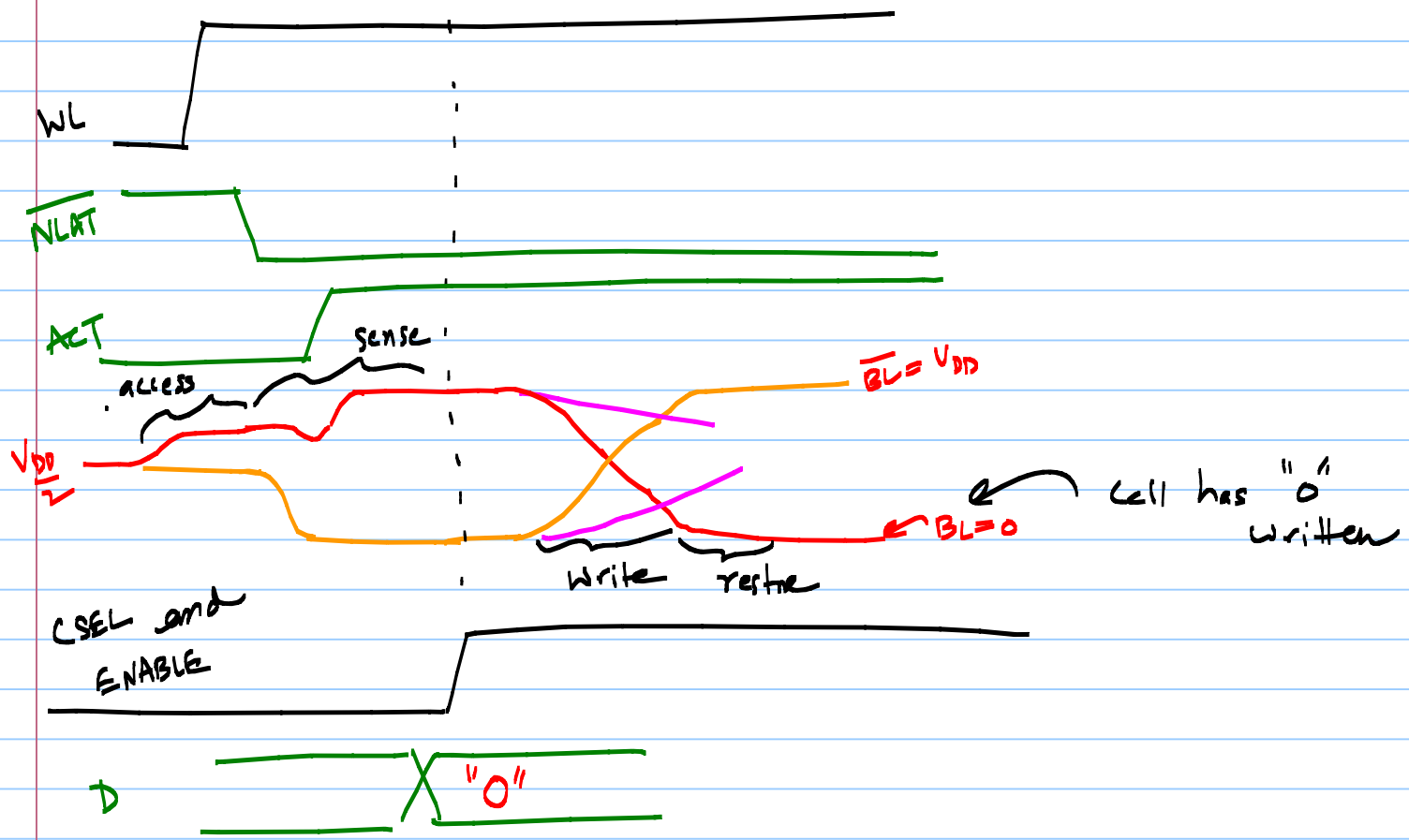
leakage → Sub V_T conduction
junction leakage
GIDL

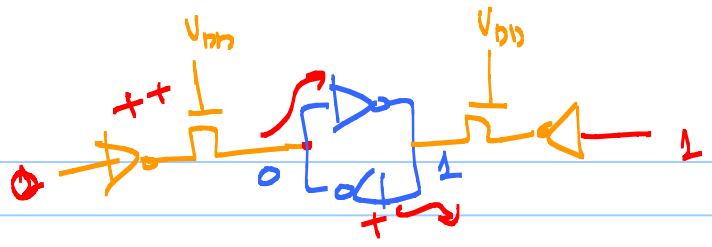
-ve Body biasing



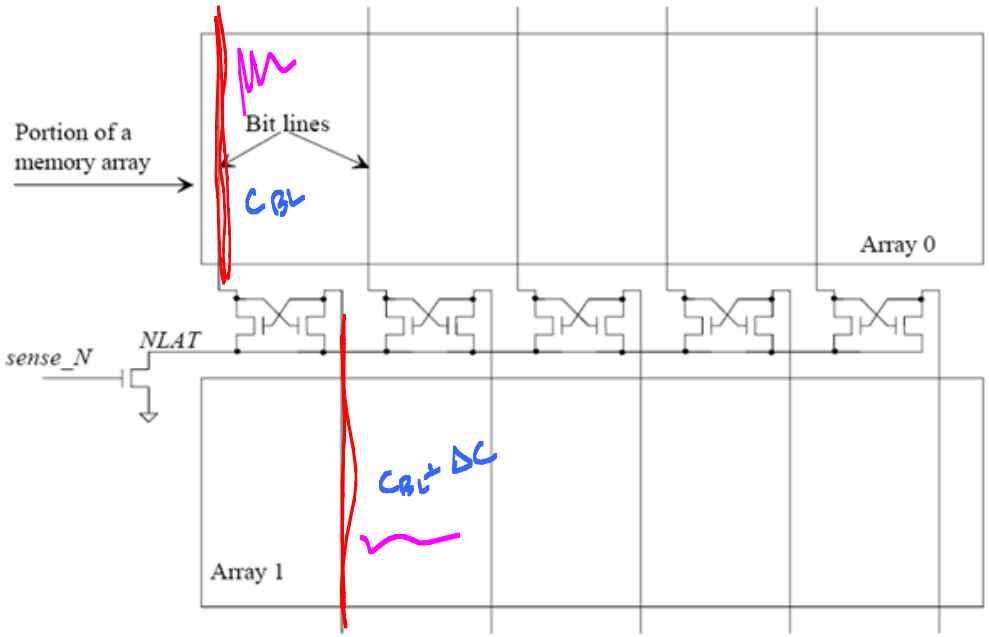

"0"
D
0
"1"
D
V_{DD}
fistate
ENABLE
decoded from the chip command
$\overline{WR}$
I/O transistors
WL
BL
ACT
NLAT
$\overline{BL}$
CSEL
I/O
$\overline{I/O}$
output load

Ex. Sense "1" followed by a "0" write operation





← SRAM cell



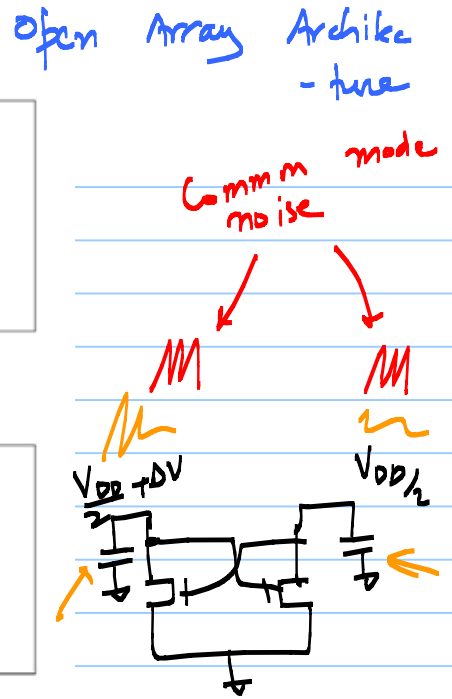


Figure 16.6 How the NSA is placed between two memory arrays in the so-called open memory array architecture.

Folded Array Architecture

Can't have a mbit cell at every intersection of WL & BL's

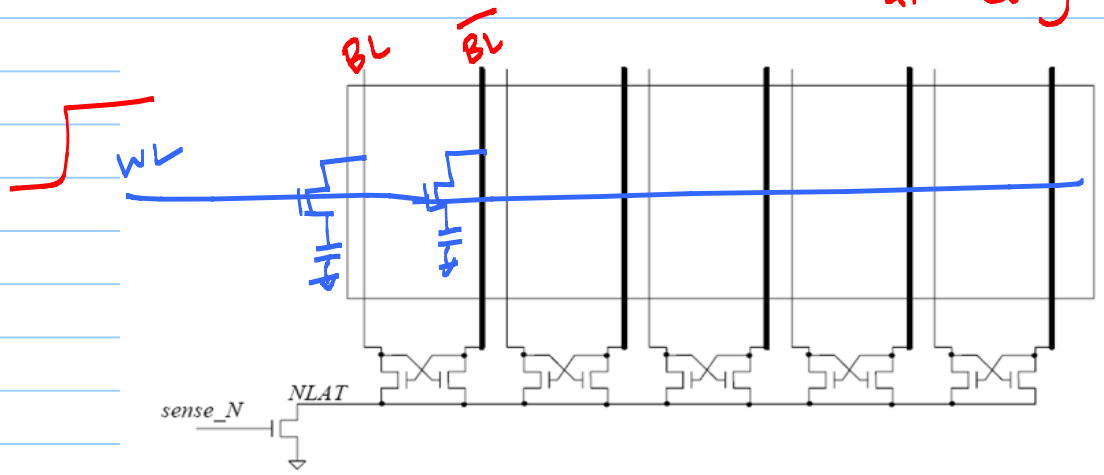


Figure 16.16 The folded array is formed by taking the open array architecture (open book) topology seen in Fig. 16.6 and "closing the book," that is, folding array 1 on top of array 0. Note that the bold lines indicate the bitlines from array 1 in the newly formed array.

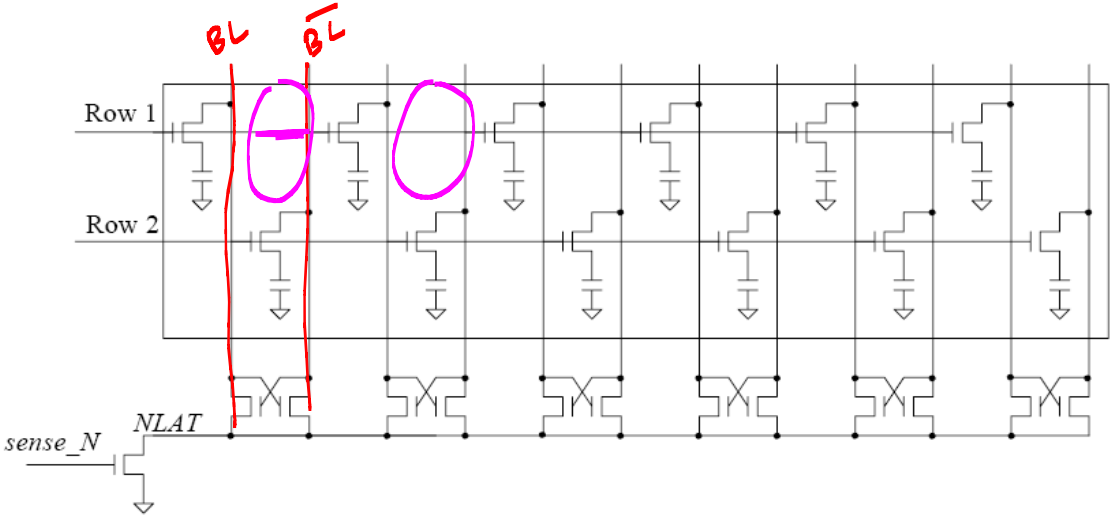
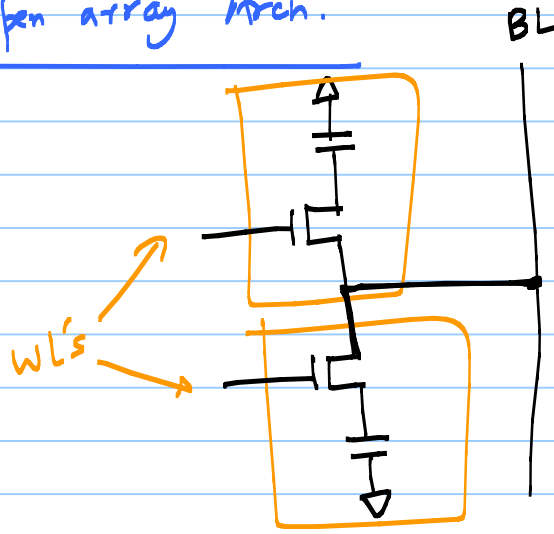
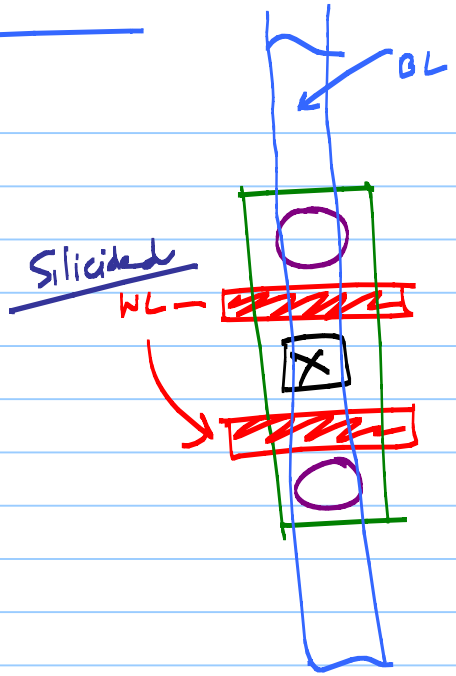


Figure 16.17 How a memory cell is located at every other intersection of a row line and a column line in a folded-area architecture.

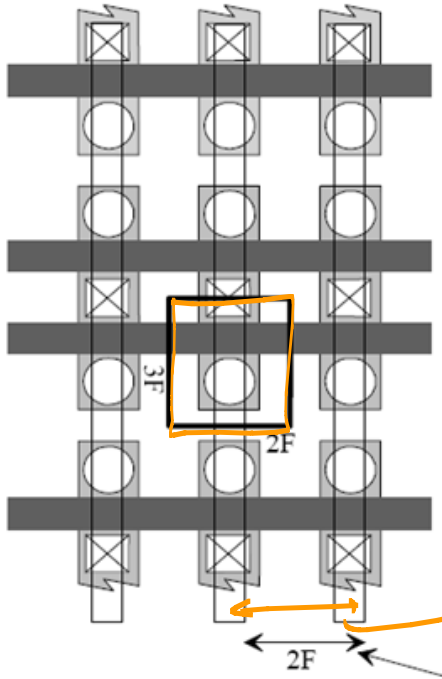
Layout of a 1bit Cell

Open array Arch.





F is feature size, which is half the bit line pitch; that is, F = pitch/2.



process technology

$F = \frac{P}{2}$

$6F^2$

Bitline pitch

Figure 16.19 Layout of mbit used in an open bit line configuration.

Folded Array

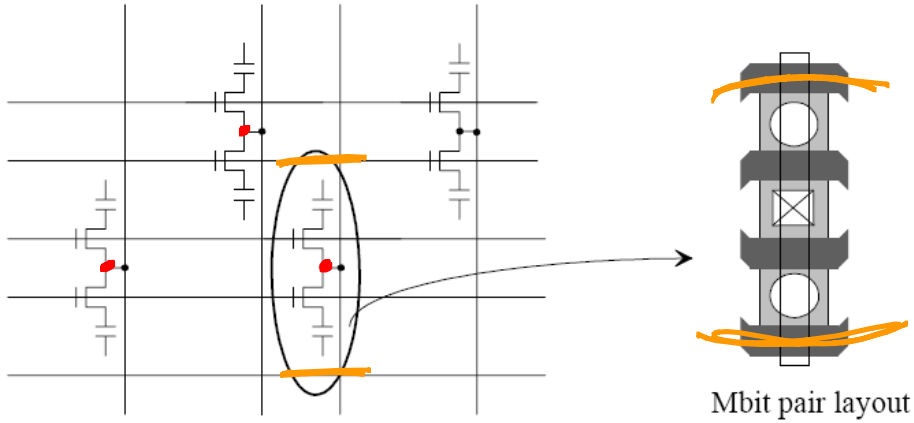


Figure 16.20 The mbit pair used for a folded architecture.

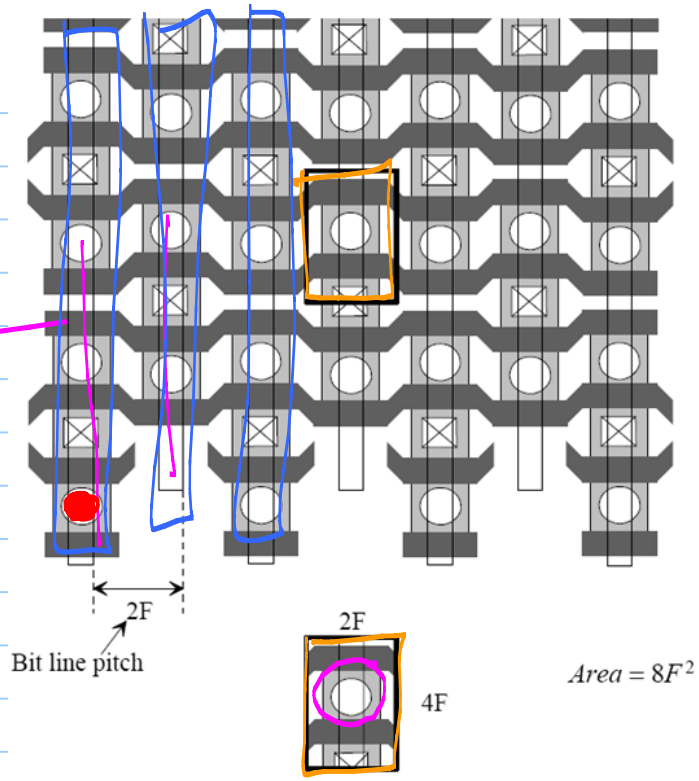


Figure 16.21 Folded architecture layout and cell size.

(a) Trench Cap

(b) Buried Capacitor

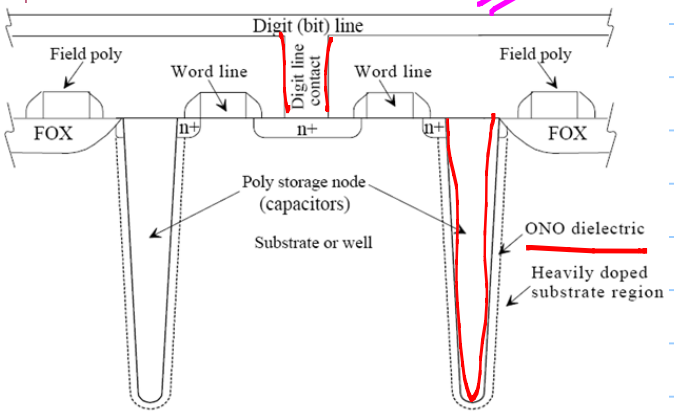


Figure 16.22 Cross-sectional view of a trench capacitor cell.

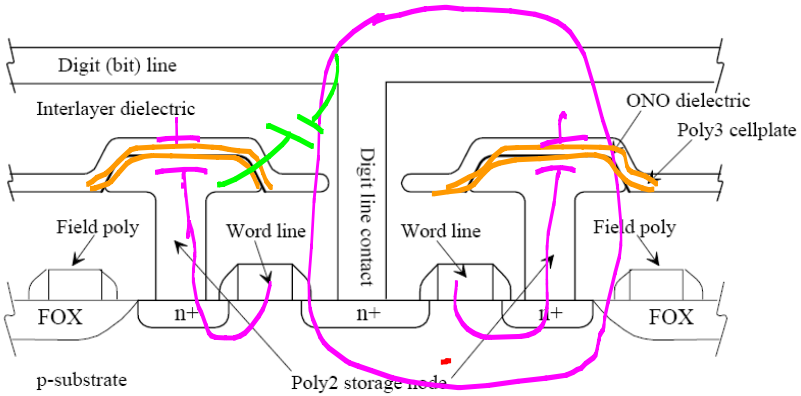


Figure 16.23 Cross-sectional view of a buried capacitor cell.

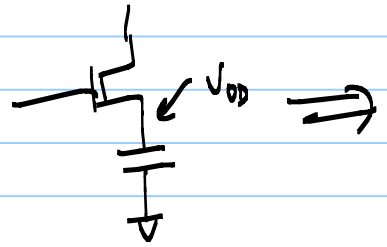
(+) Good density
(+) Less coupling
(−) Process is Complicated

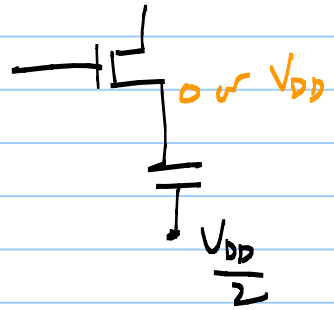
(+) Simpler process
(−) more coupling
(−) Larger Cap area

$C_{ox} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}}$ ↑

lower t_{ox}

✗ Reduce dielectric stress





stress $\leq \frac{V_{DD}}{2}$