ECE 518 → Lecture 26

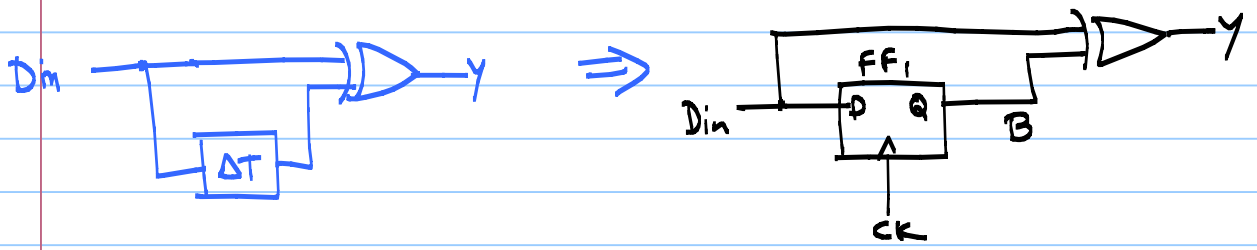
Note Title 4/25/2013

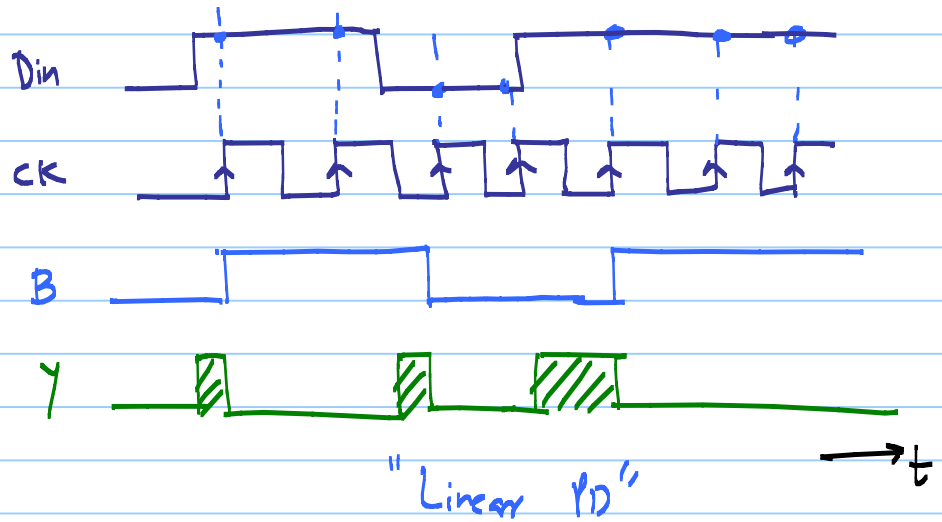
* Phase detectors for random data

① data transition detection

② phase difference detection

① Hogge or Linear PD





$t_{CQ} = 0$

⇒ Circuit produces a pulse for each data transition
↳ edge detection

⇒ width of each pulse (Y) varies linearly with $\Delta\phi$ between Din and CK.

* average value of V_y depends upon data transition density

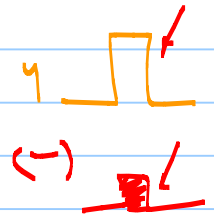
⇒ PD gain depends upon α → data transition density

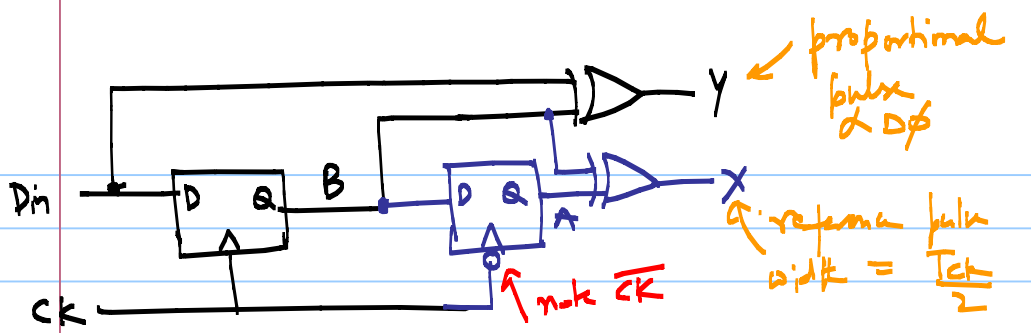
↳ 0.5

⇒ we need CK to align with the middle of the bit period

* create a reference pulse

↳ reference pulse should also depend upon data transition density

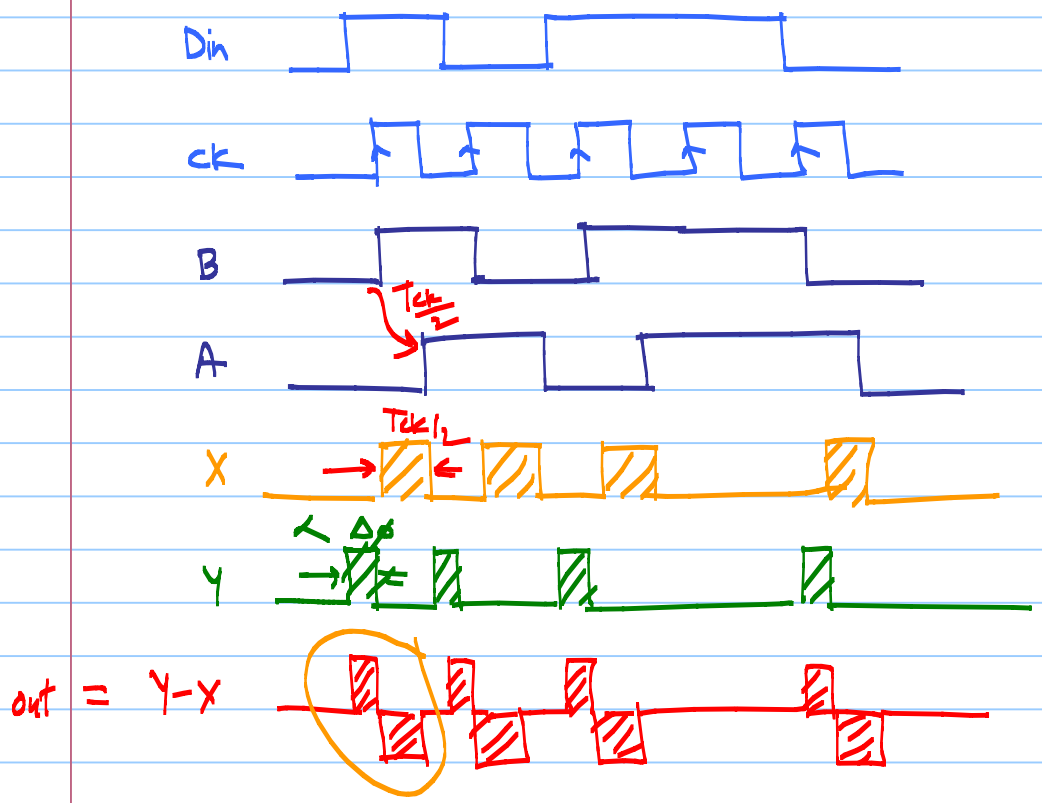




proportional pulse $\propto D\phi$

reference pulse width = $\frac{T_{clk}}{2}$

$\Rightarrow$ FF_2 Delay retimed data B by $\frac{T_{clk}}{2}$ and XOR with itself


Din
ck
B
A
X
Y
out = Y-X

* Difference b/w areas of X & Y are the PD output

* In locked condition X and Y produce equal widths $= \frac{T_{clk}}{2}$
at this point $\arg(Y-X) = 0$

$\Rightarrow$ ∵ PW of $X = \frac{T_{clk}}{2}$

$\Rightarrow$ PW of $Y = \frac{T_{clk}}{2}$

$\Rightarrow$ CK is aligned with the middle of data

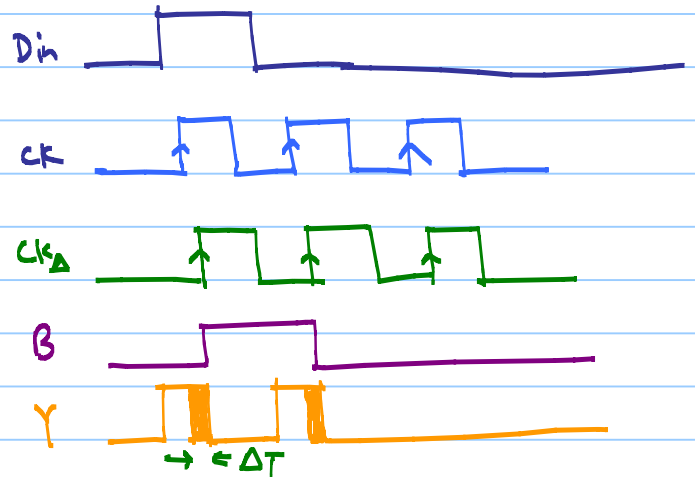
* Hogge PD (1985)

Hogge PD Non-idealities:

* finite delay in FFs → t_{cq}

↳ B changes $\Delta T = t_{cq}$ after the clock rising edge

⇒ pulse at Y is ΔT wider than the actual phase difference between Din & clk.



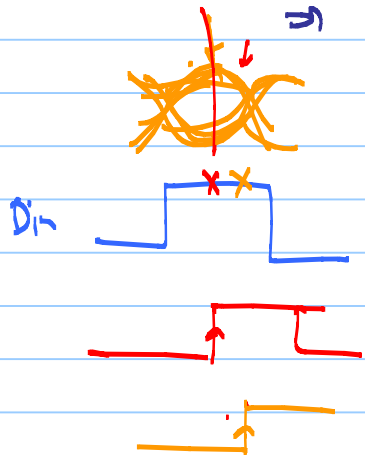
"SONET"
STM-1
E1/T1

$$\phi_{offset} = \frac{\Delta T}{T_{CK}} \cdot 2\pi$$

Pulse width of X is still $\frac{T_{clk}}{2}$

* t_C simply changes the PW at Y to be greater by ΔT

⇒ in locked condition ⇒ Din & CK sustain a skew of ΔT so as to equalize the widths of X & Y



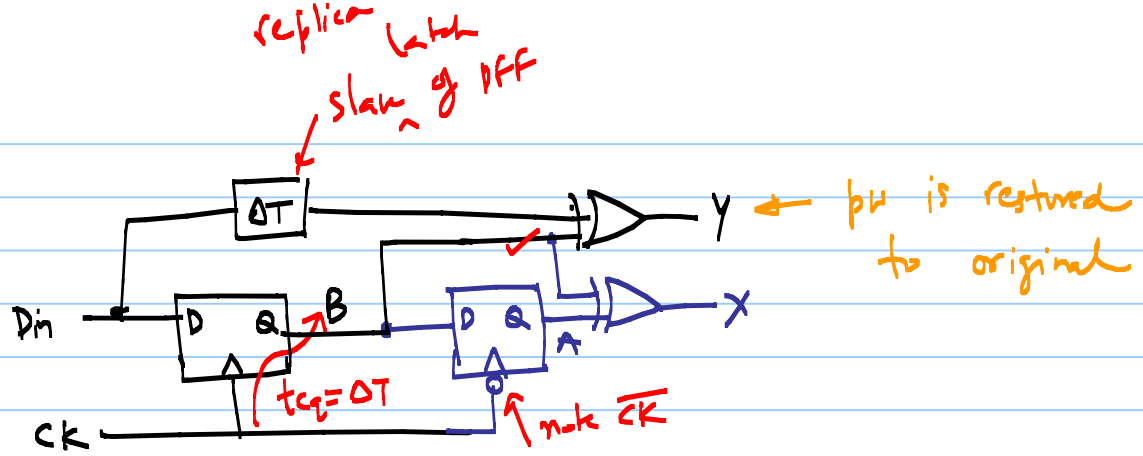
↳ lose timing margin

at high speeds ΔT could be comparable to T_{clk}

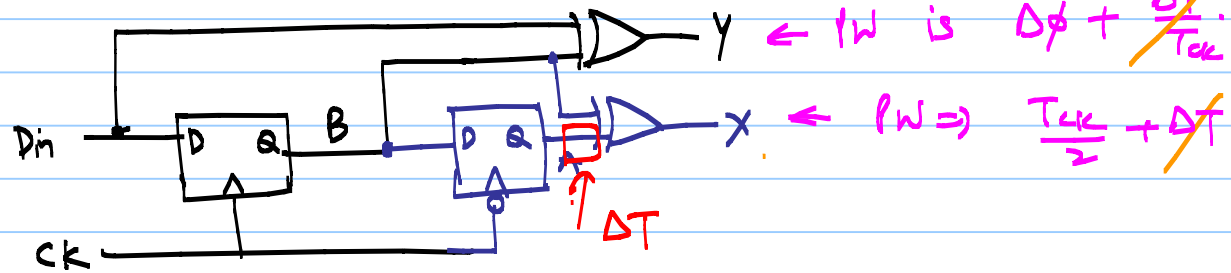
* Also degrades jitter tolerance

* BER ⟶ 10^{-12}

bit error rate "BERT"



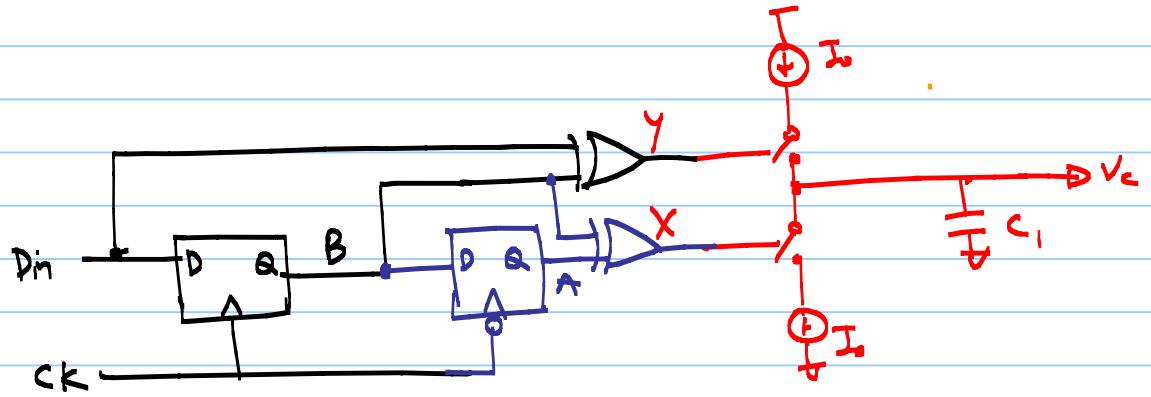
← pw is restored to original

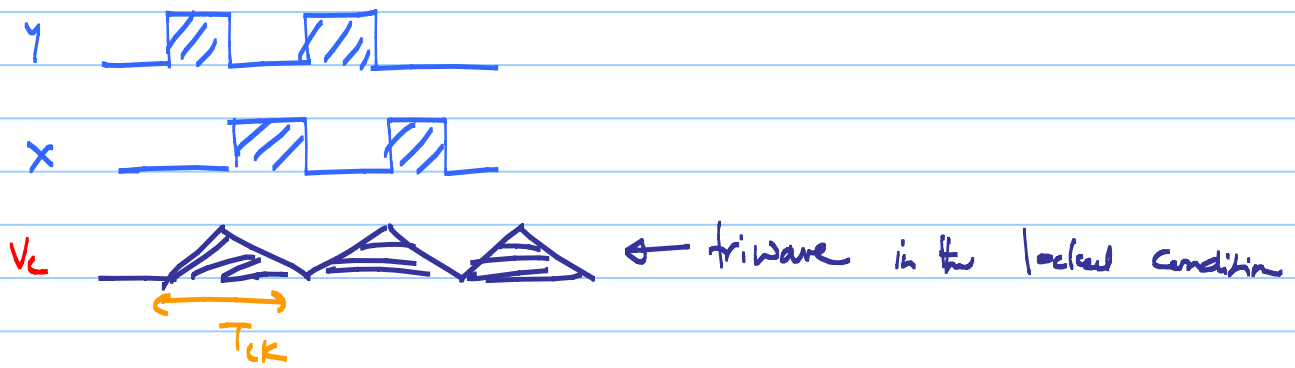


← PW is $\Delta\phi + \frac{\Delta T}{T_{CK}} \cdot 2\pi$

← PW ⇒ $\frac{T_{CK}}{2} + \Delta T$

Type - II





← triware in the locked condition

⇒ a triangular wave is generated at Vc
which has nonzero area
↳ surely disturbs VCO phase
↳ deterministic jitter

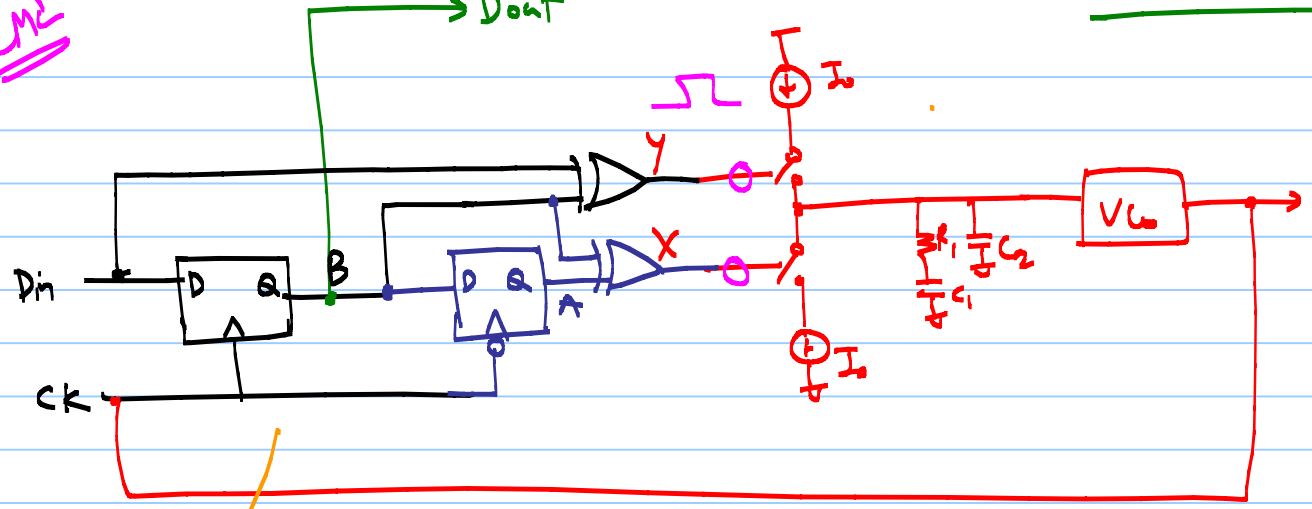
modification of Hogge PD

CMOS

retimed data

Dout

Type-II CDR



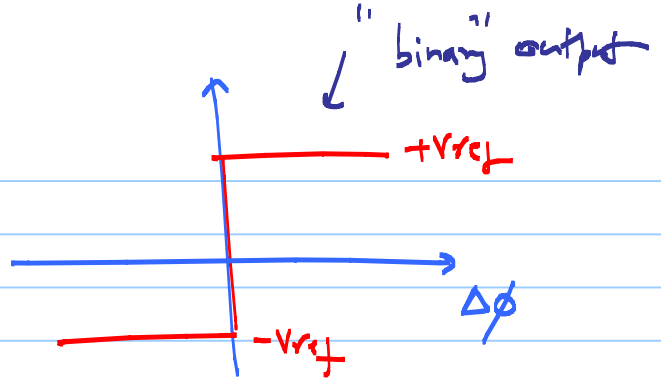
$K_{PD} = \frac{\alpha I_o}{2\pi C}$

* Linear CDR → Hogge PD

✓ little activity when the CDR loop is locked

✗ requires very wide BW at X & Y
to ensure complete switching of the CP
to avoid dead zone

Alexander Phase Detector



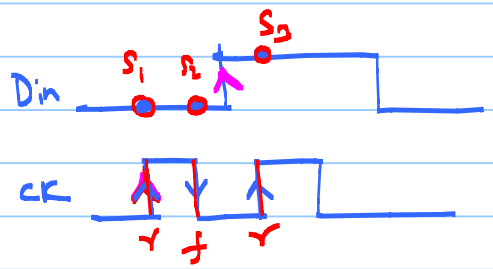
non-linear PD

Bang-Bang PD

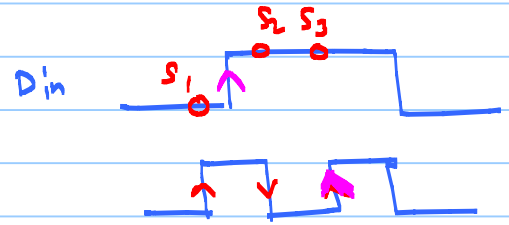
!! PD

VDD!, GND!

Clock Early



Clock Late



→ Take three data samples S_1, S_2 & S_3 by 3 consecutive clock edges

→ The PD detects whether a transition occured and whether the clock leads or lags data

→ A "Early-Late" detection method.