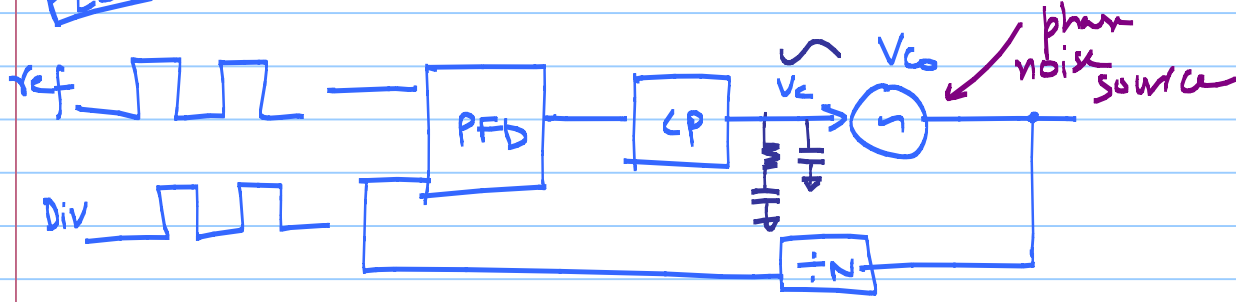
ECE 518- Lecture 23

Note Title 4/16/2013

PLL

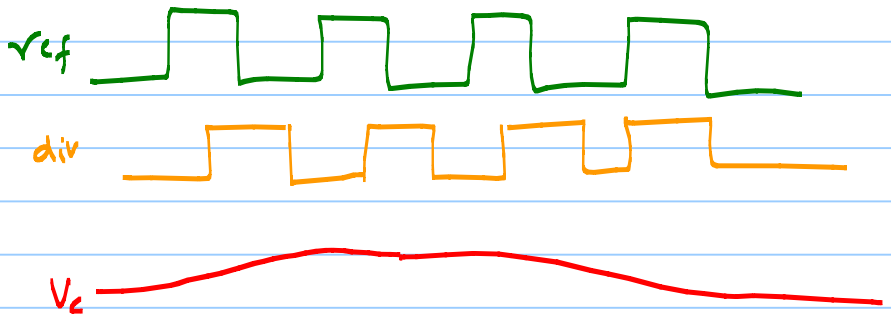


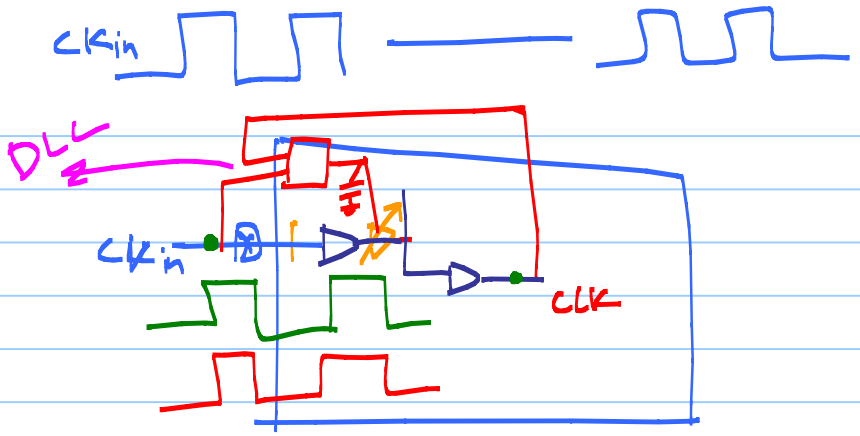
phase noise source

$R_{ing} \rightarrow 3\text{-}5\times$

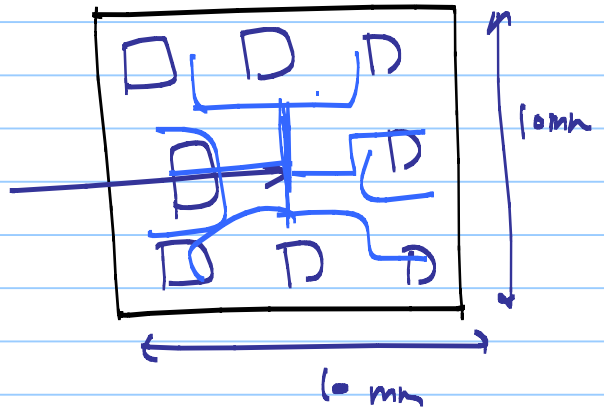
$L_C \rightarrow 25\%$

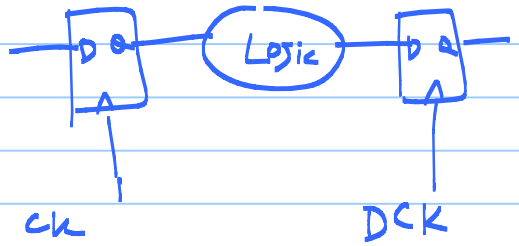
$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$





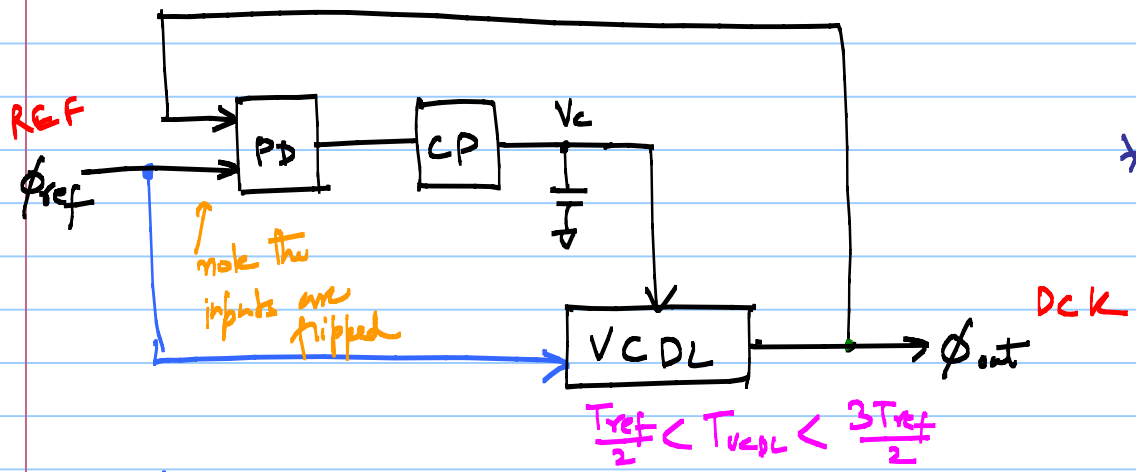
Clock Tree





Delay locked Loop (DLL)

VCDL → Voltage Controlled Delay Line



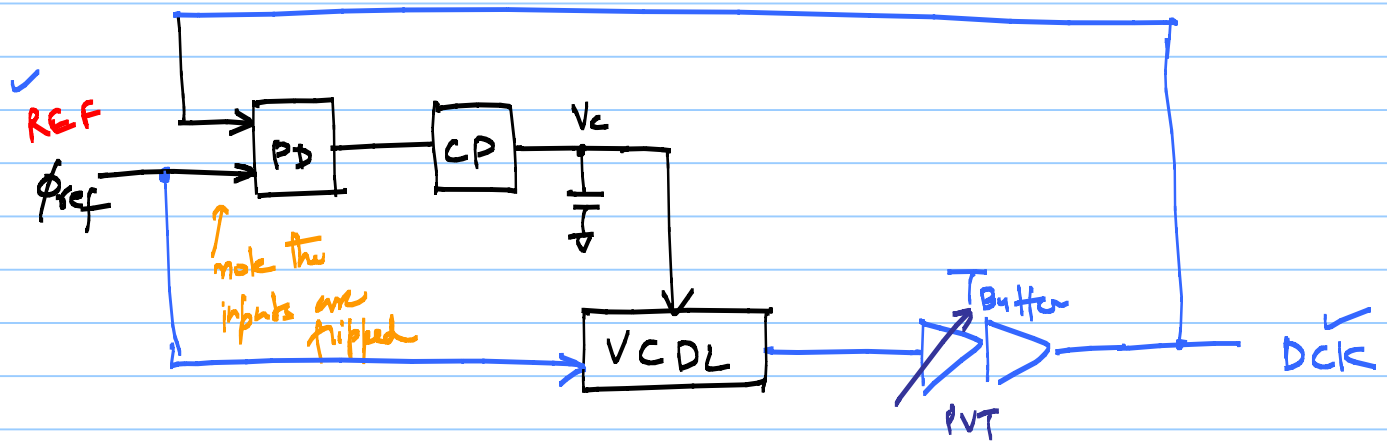
* first order system

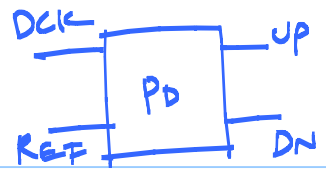
$\frac{T_{ref}}{2} < T_{VCDL} < \frac{3T_{ref}}{2}$

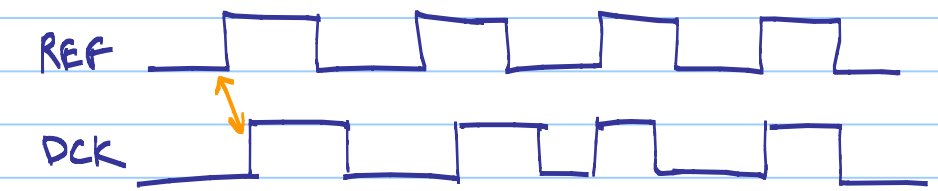
Objective: align output clock phase (ϕ_{out}) to the input clock phase (ϕ_{ref})

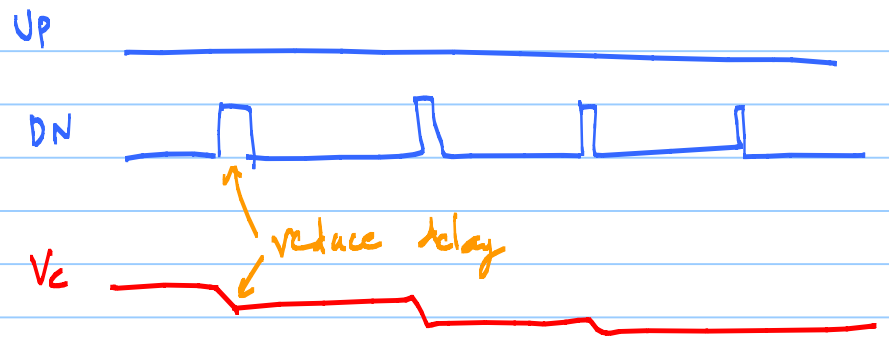
* reference is applied to both PD & VCDL

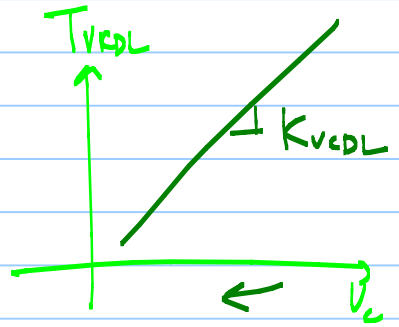
x In steady-state, VCDL delay (T_{VCDL}) =



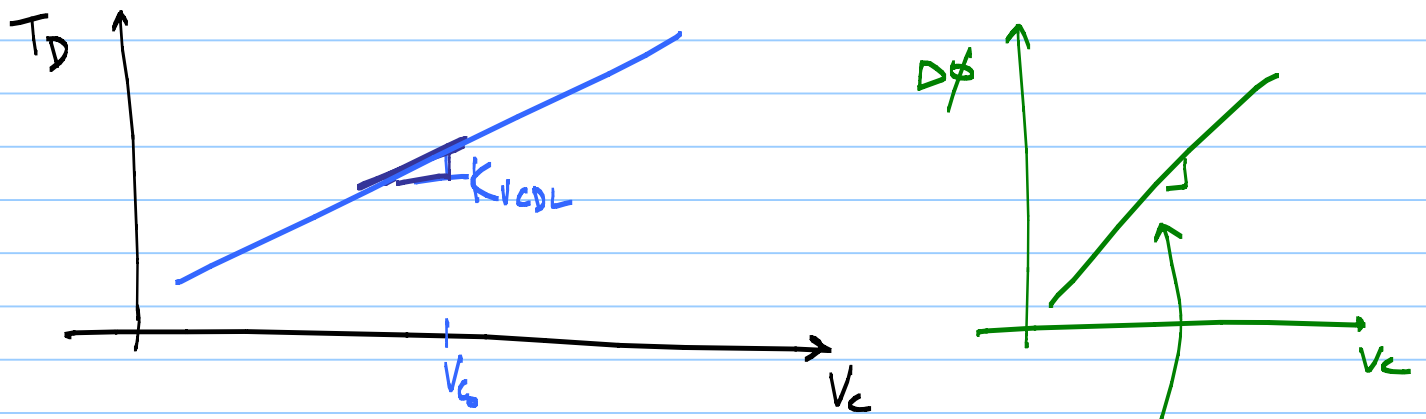

DCK
UP
PD
REF
DN


REF
DCK


UP
DN
reduce delay
Vc


TVCDL
KVCDL
Vc

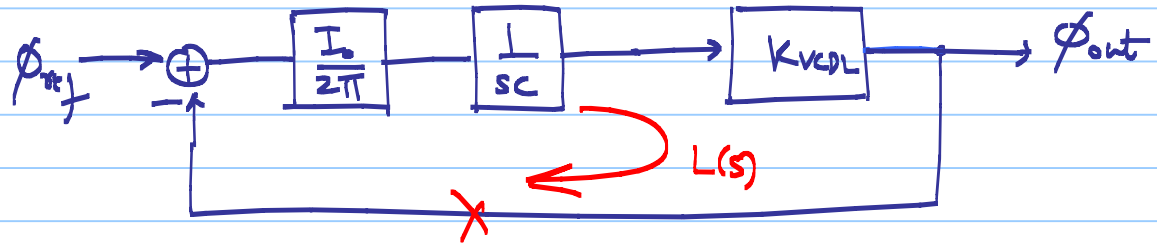
VCDL :



VCDL gain ; $K_{VCDL} = \frac{\Delta T_D}{\Delta V_c}$, $\frac{sec}{V}$

$$K_{VCDL} = \frac{2\pi}{T_{ref}} \cdot \frac{\Delta T_D}{\Delta V_c} , \quad \frac{rad}{V}$$

Phase domain Model :



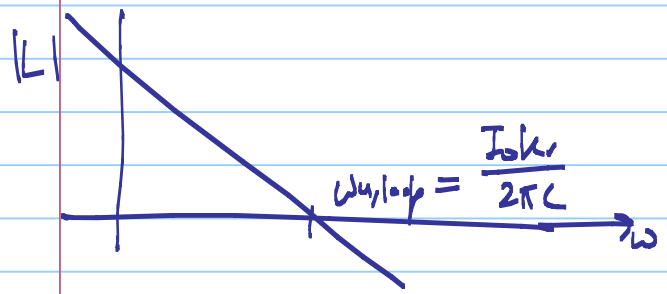
$$L(s) = \frac{I_p}{2\pi}\frac{K_{VCO}}{sC}$$ ← single integrator

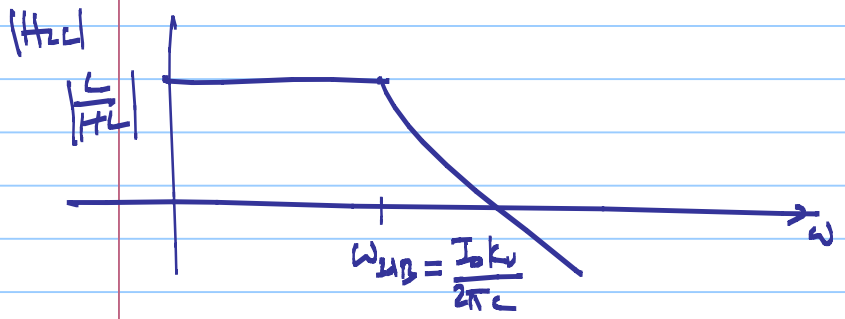
Type-I 2nd-order

$$H_{cl}(s) = \frac{\phi_{out}}{\phi_{ref}}(s) = \frac{L(s)}{1+L(s)} = \frac{\frac{I_p K_v}{2\pi\, sC}}{1+\frac{I_p}{2\pi}\frac{K_v}{sC}}$$

$$H_{cl}(s) = \frac{1}{1 + \frac{2\pi s C}{I_0 \cdot k_v}}$$

$$= \frac{1}{1 + \frac{s}{\omega_{3dB}}}$$

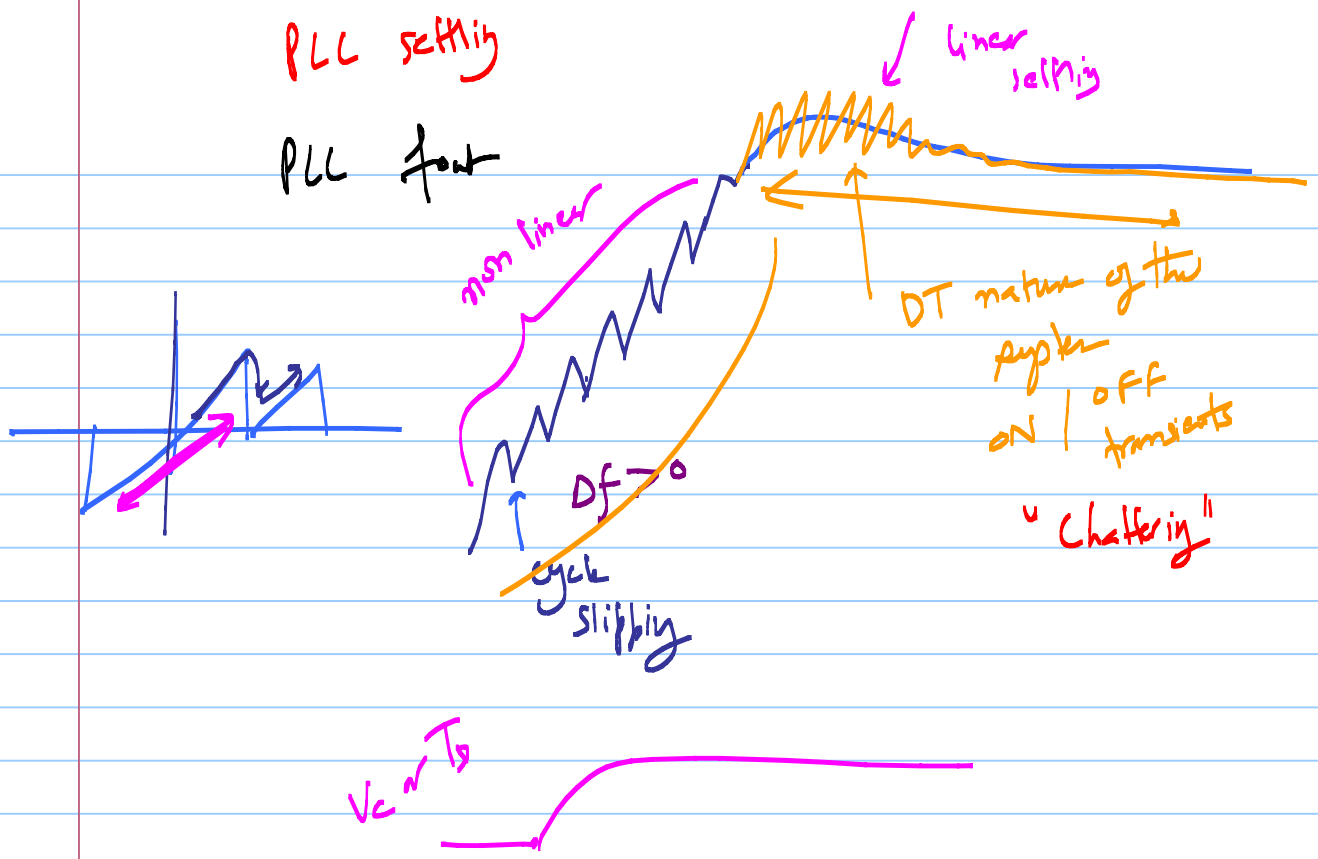




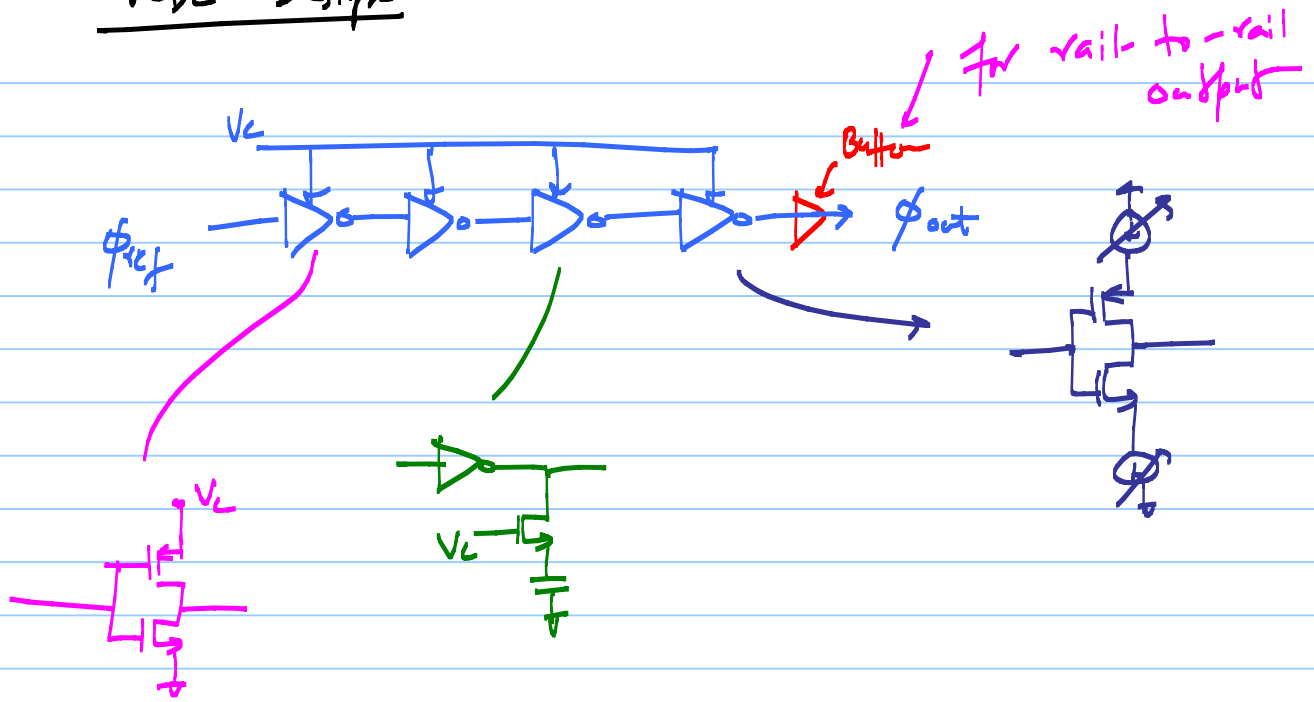
$$\omega_{u,loop} = \omega_{3dB} = \frac{I_0 K_{vcDL}}{2\pi C}$$

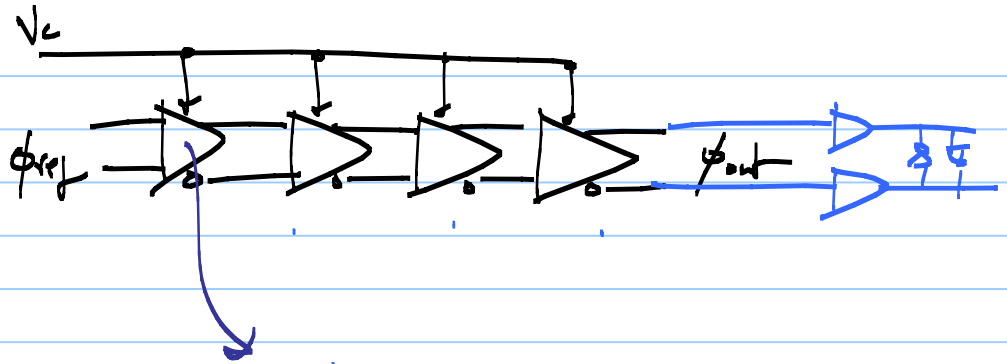
1% settling $\rightarrow \frac{4.7}{\omega_{3dB}}$

$$\#\ of\ \frac{ref}{cycles} = \frac{\frac{4.7}{\omega_{3dB} \cdot T_{ref}}}$$

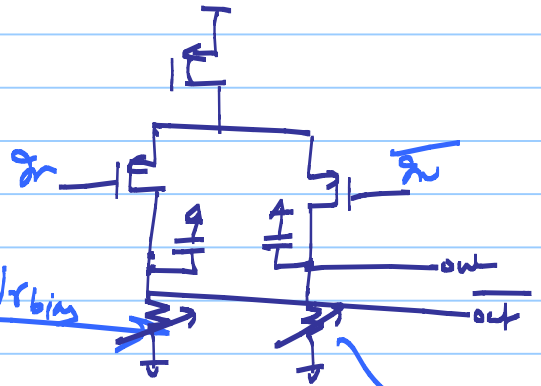

PLL settling
PLL fast
linear settling
non linear
DT nature of the pulse
on / off transients
" Chattering"
Df = 0
cycle slipping
Vc or Td

VCDL Design

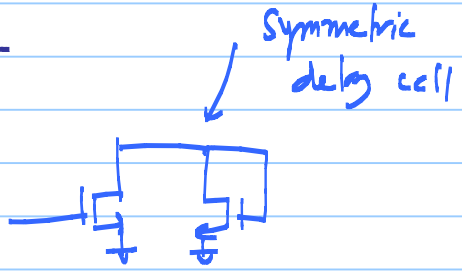


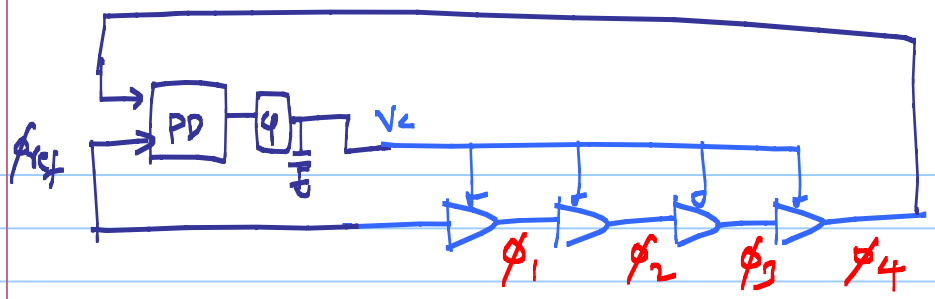


Replica biasing



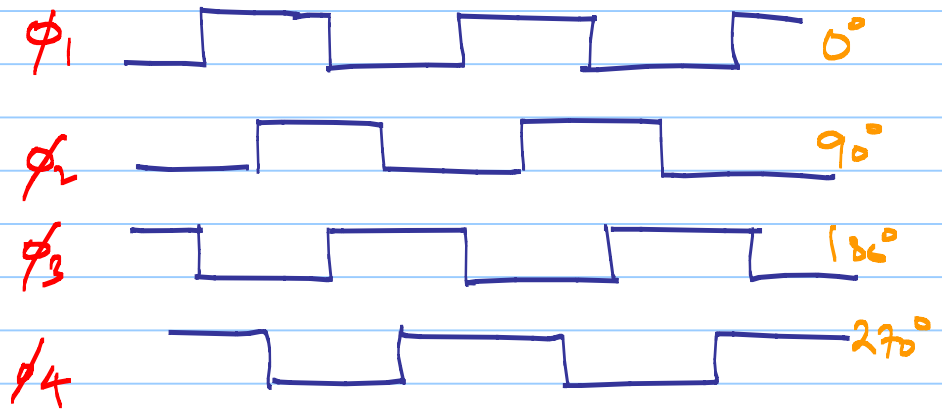
Better PSRR





$T_c = T_{ref}$

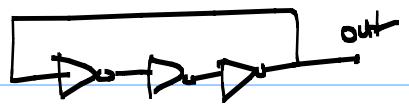
$\tau = \frac{T_{ref}}{4}$



Generate Multi phase clocks (PVT Tolerant)

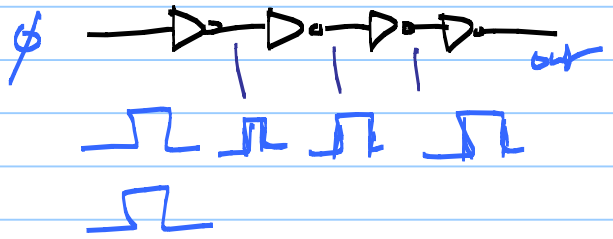
$\times$ phase mismatch

open loop VCO



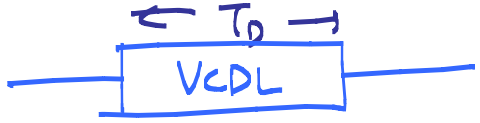
accumulates jitter

Delay line



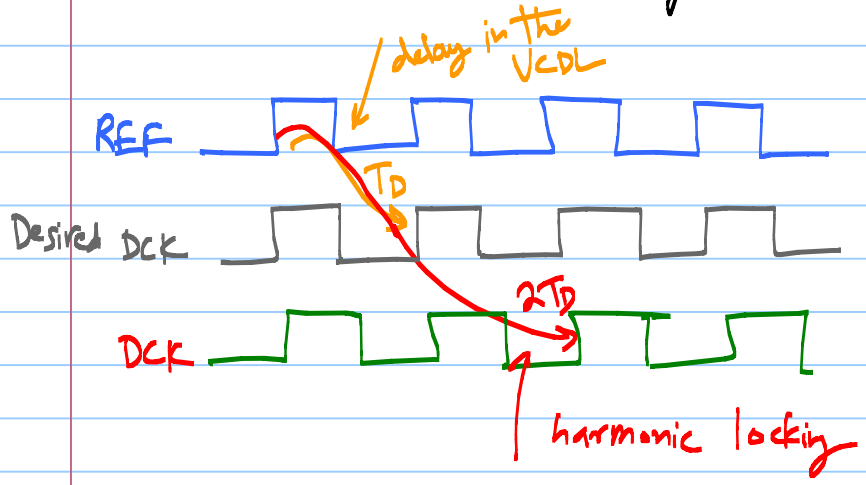
* DLL accumulates jitter only for T_{ref}

DLL issues



$T_{D_{min}} < T_D < 2.5 T_{ref}$

① Harmonic locking



In locked condition

$T_D = T_{ref}$

$= 2T_{ref}$

⋮

* Accumulate jitter for $2T_{ref}$ instead of T_{ref}

* To avoid harmonic locking $T_D < 2T_{ref}$

* Some logic to detect false locking
  - ↳ reset T_D to T_{min}
    V_{CDL} delay to minimum delay.

Stuck at minimum Delay

Problem: DLL trying to lock with $T_D = 0$

$$T_{D,min} > \frac{T_{ref}}{2}$$

* Stuck at maximum delay