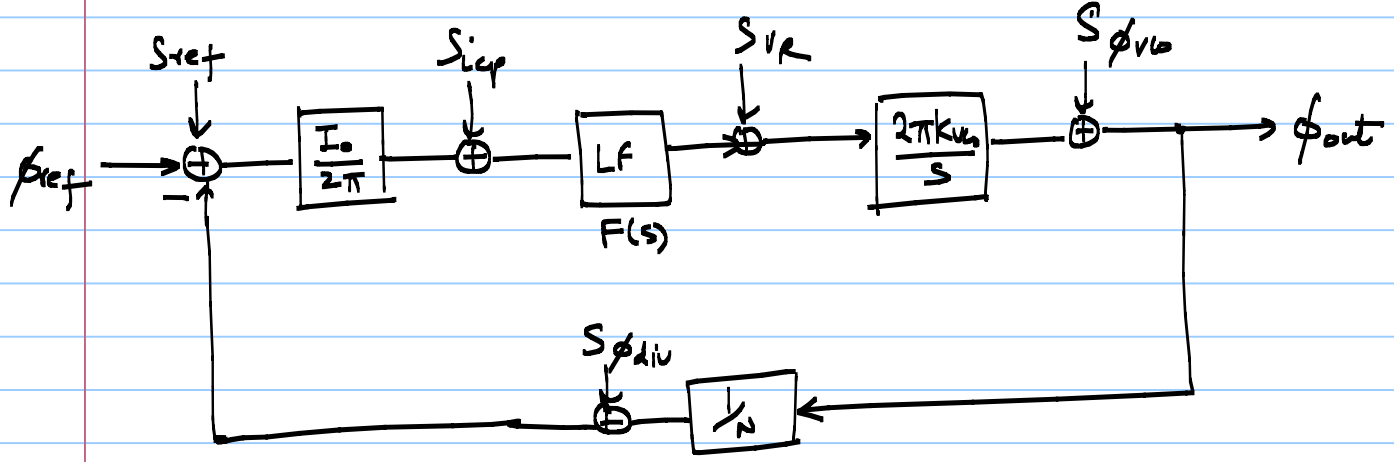
ECE 518 – Lecture 22

Note Title 4/11/2013



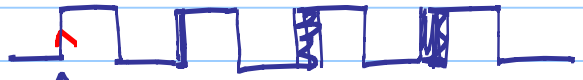
Aside:

free running oscillator

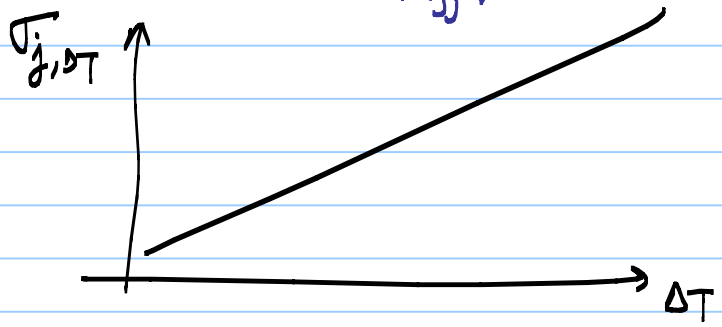
* f_{ck} is not stable with PVT

Can't use a free running VCO

* Accumulated jitter

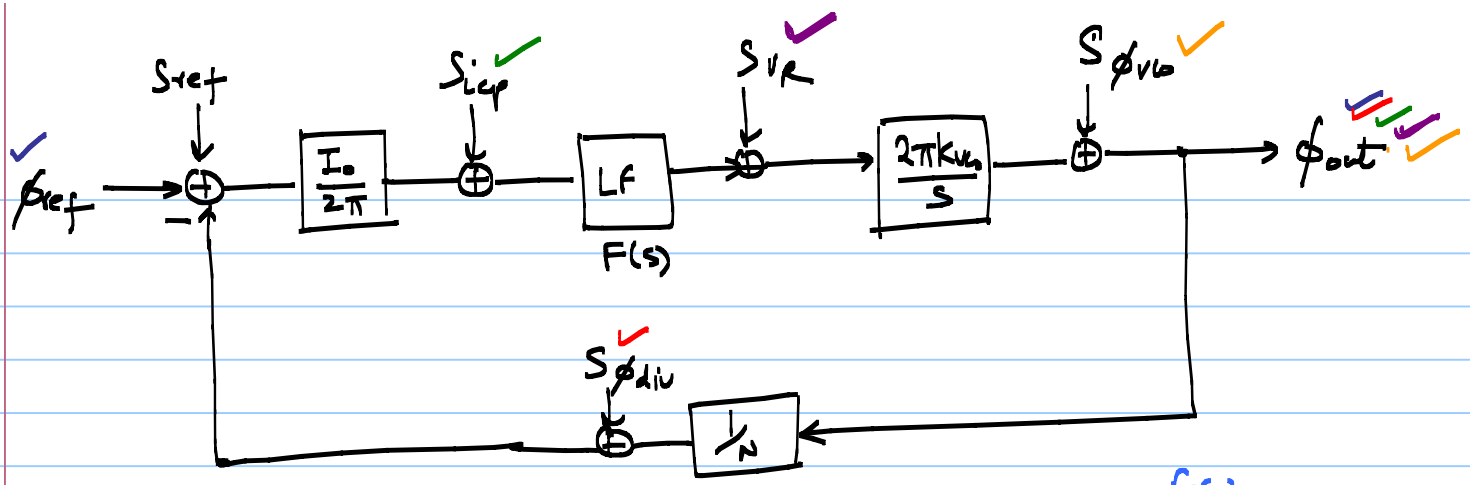


accumulated jitter

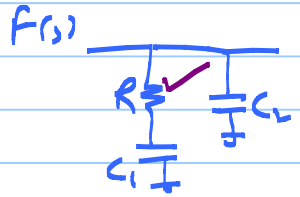


random walk

Brownian motion



$$L(s) = \frac{I_0 K_{VCO}}{N} \cdot \frac{F(s)}{s}$$



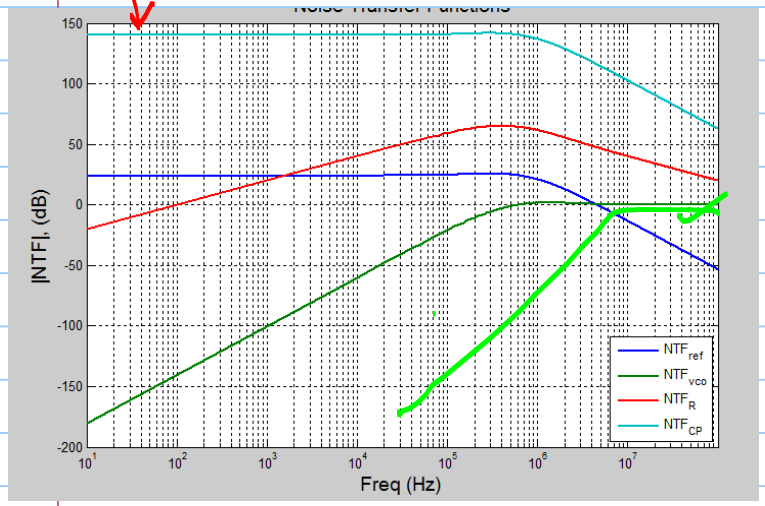
$$NTF_{ref}(s) = \frac{\phi_{out}(s)}{\phi_{ref}(s)} = \frac{N \cdot L(s)}{1 + L(s)}, \qquad NTF_{div}(s) = NTF_{ref}(s)$$

$$NTF_{cp}(s) = \frac{\phi_{out}(s)}{i_{cp}(s)} = \frac{2\pi}{I_0} \cdot NTF_{ref}(s)$$

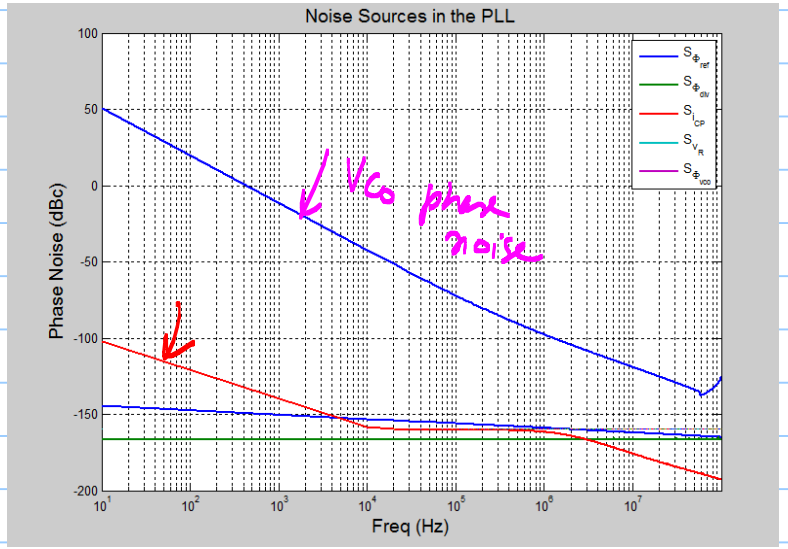
$$NTF_R(s) = \frac{\phi_{out}(s)}{V_R(s)} = \frac{\frac{(2\pi K_{VCO})}{s}}{1 + L(s)}$$

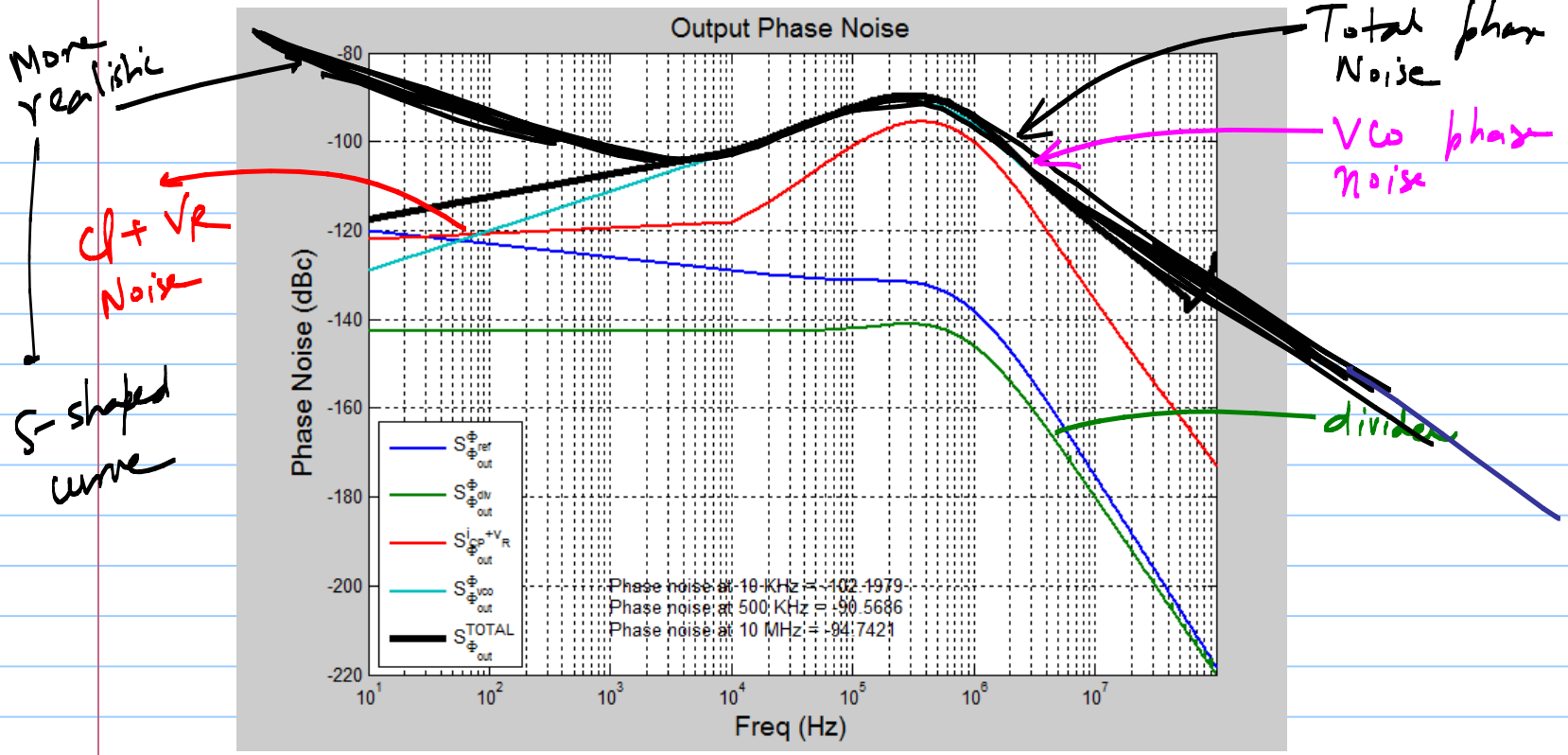
$$NTF_{VCO}(s) = \frac{\phi_{out}}{\phi_{VCO}}(s) = \frac{1}{1 + L(s)}$$

NTFs

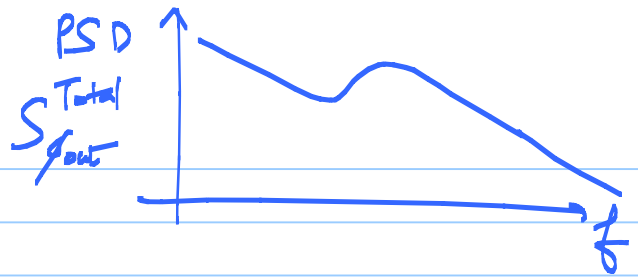


Noise Sources




More realistic
S-shaped curve
Output Phase Noise
Phase Noise (dBc)
Freq (Hz)
-80
-100
-120
-140
-160
-180
-200
-220
10^1
10^2
10^3
10^4
10^5
10^6
10^7
$S^{\Phi}_{\Phi_{out}}{}^{ref}$
$S^{\Phi}_{\Phi_{out}}{}^{div}$
$S^{i_{CP}+V_R}_{\Phi_{out}}$
$S^{\Phi}_{\Phi_{out}}{}^{vco}$
$S^{TOTAL}_{\Phi_{out}}$
Phase noise at 10 KHz = -102.1979
Phase noise at 500 KHz = -90.5686
Phase noise at 10 MHz = -94.7421
Total phase Noise
VCO phase noise
divider
CP + VR Noise

Jitter Calculation



Total phase noise

$$\sigma_{\Delta\phi}^2 = \int_0^\infty S_{\phi_{out}}^{total}(f)\, df$$

rms

$$\sigma_{\Delta\phi} = \sqrt{\int_0^\infty S_{\phi_{out}}^{total}(f)\cdot df} \quad \text{radians}$$

$$= \sqrt{\int_0^\infty S_{\phi_{out}}^{total}(f)\cdot df} \cdot \frac{360^\circ}{2\pi} \quad \text{degrees}$$

$$\sigma_{DT} = \sqrt{\int_{-\infty}^{\infty} S_{\phi_{out}}^{Total}(f) \cdot df} \cdot \frac{T_{VCO}}{2\pi} \quad (sec)$$

σ_{DT} ↑ rms jitter (ps)

↑ random jitter (rj)

---

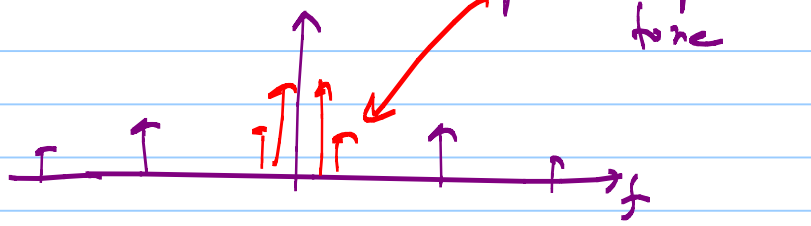
deterministic jitter (dj)

PSRR

* cf current mismatch — static / dynamic
* charge sharing

$N = 2.125 = 2 + \frac{1}{8} = \frac{17}{8}$

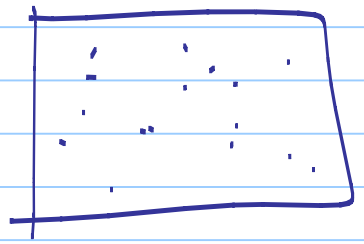
fractional divider → dj



mismatch → Monte Carlo simulation

* analysis

* PSRR → Brute force simulation



$\Rightarrow$ r_j & d_j Tradeoff

$d_j \Rightarrow$ reference feedthrough $\Leftarrow$ LPF

$r_j \Rightarrow$ VCO phase noise $\Rightarrow$ HPF

LPF, HPF $\rightarrow$ loop BW ω_{3dB}

ω_{3dB} $\rightarrow$ Power tradeoff

Noise optimization:

$\omega_{c,loop}$ ≈ ξ

① Start with an estimate of PLL BW (ω_{3dB})
↳ $\omega_{c,loop} < \frac{\omega_{ref}}{10}$

② find loop parameters, I_p, R, C_1 & C_2,

③ Simulate/Estimate PSD of the noise sources

④ find total output noise

⑤ Meet specs?

No → ⑥ adjust ω_{3dB} to lower noise → ② find loop parameters, I_p, R, C_1 & C_2,

Yes → See if you reduce power → ② find loop parameters, I_p, R, C_1 & C_2,

Matlab + Cadence,

PLL assistant from cppsim.com

Phase Noise

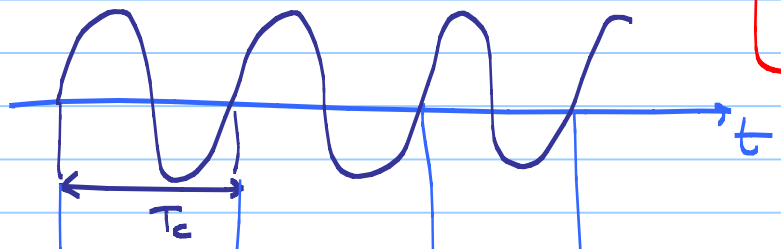
PSS

RF microelectronics
→ Razavi, 2nd Ed
2017

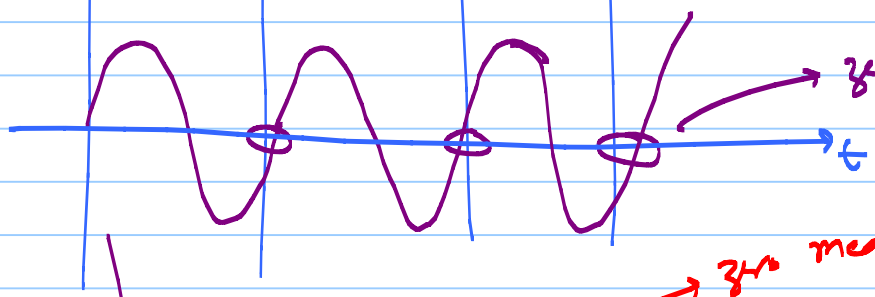
Ideal oscillator

$A\cos(\omega_c t)$

$T_c = \frac{2\pi}{\omega_c}$



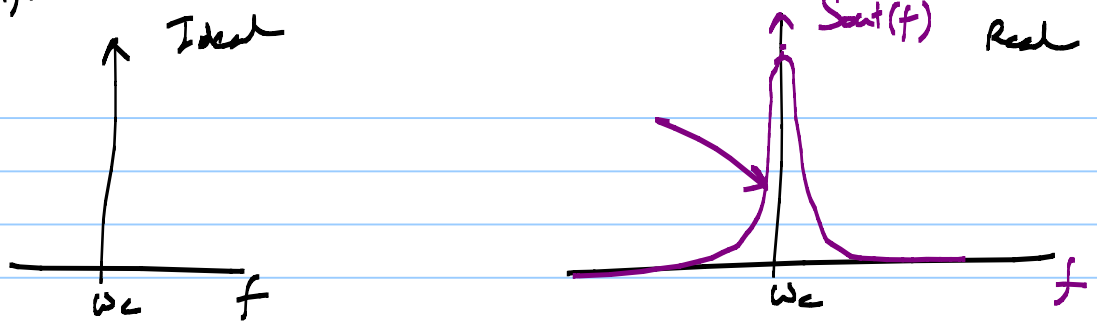
Real oscillator



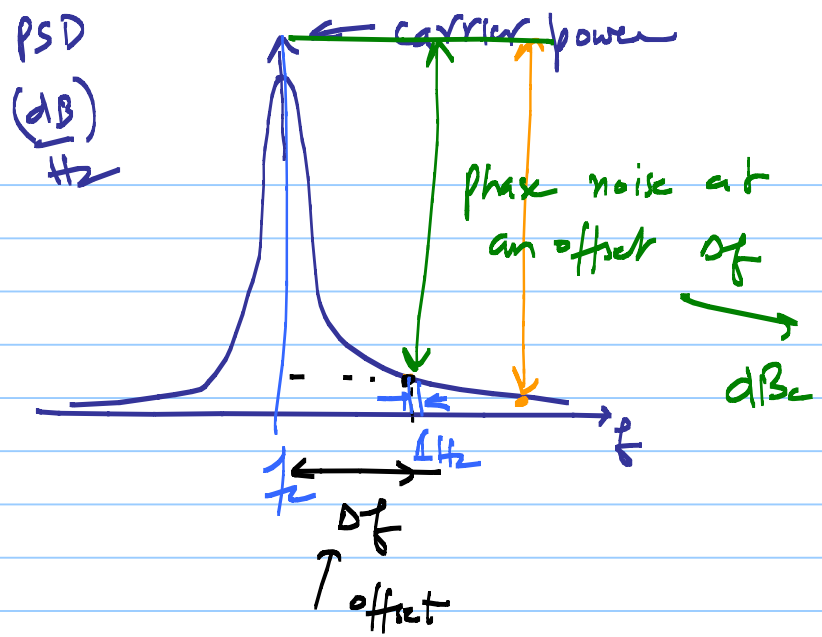
$A\cos(\omega_c t + \phi_n(t))$ → zero mean, σ, gaussian type

random "phase" noise

PSD: $S_{out}(f)$



~~impulse~~ is "broadened" due to the phase noise

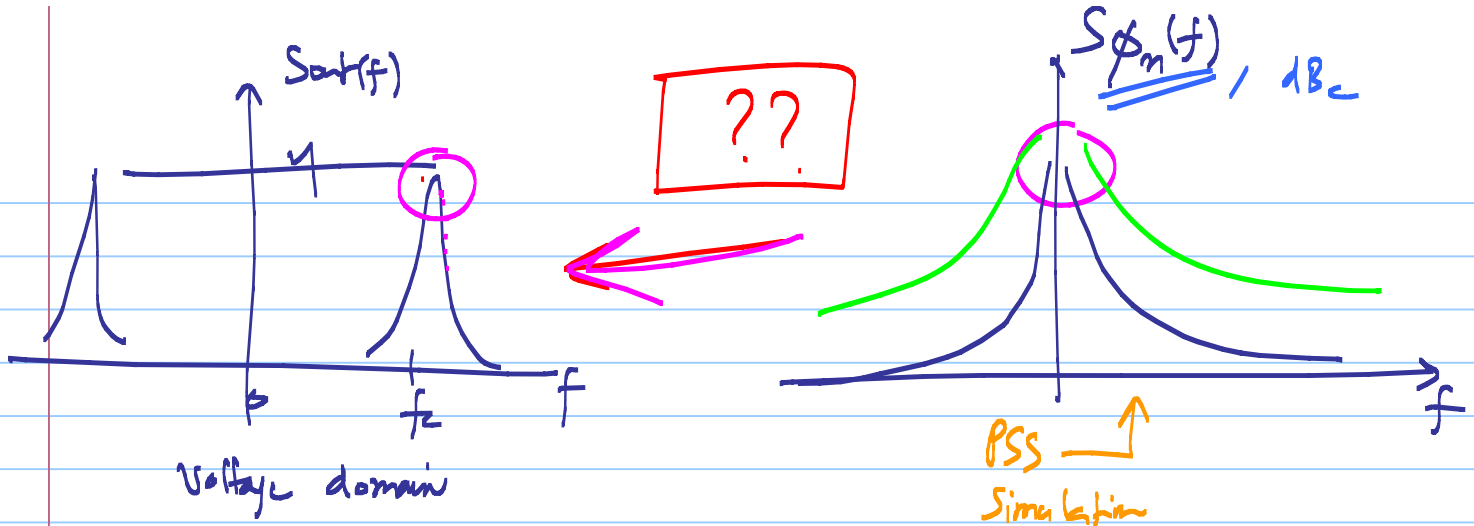


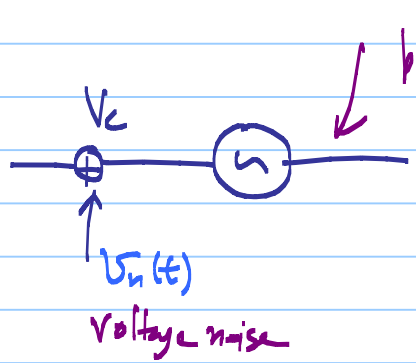
* Spectrum Analyzer
* FFT matlab

* Normalize the power at $f_c + \Delta f$ in 1 Hz BW wrt the power of the carrier (dB_c)

Ex. GSM

phase noise of the frequency synthesizer $< -115 \frac{dB_c}{Hz}$ at 600 kHz offset

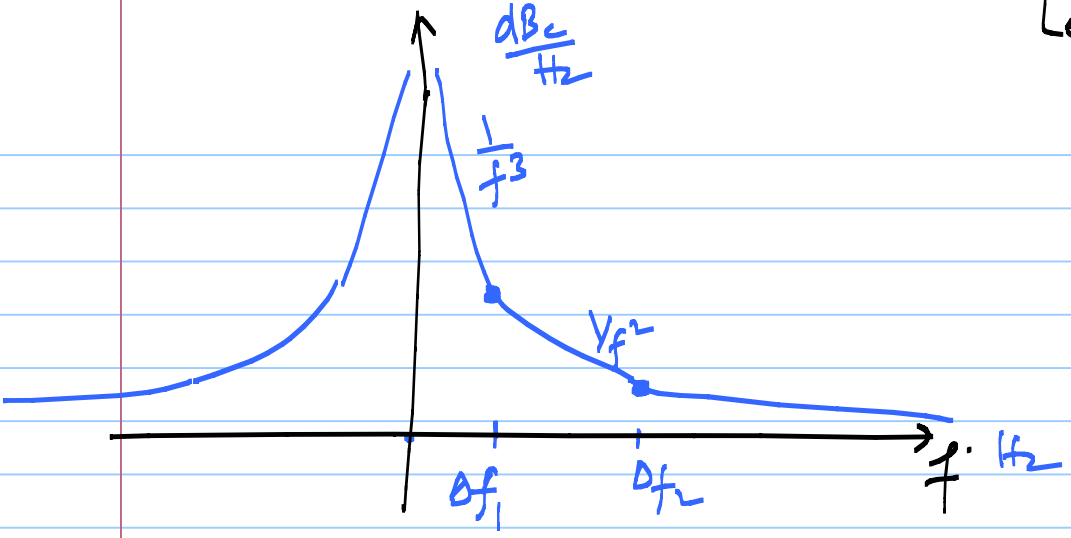




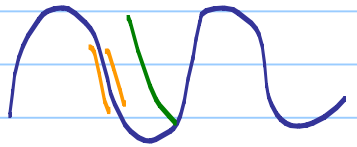
$$v_{out}(t) = A\cos(\omega_0 t + \phi_n(t))$$

$\phi_n(t) = f(v_n)$

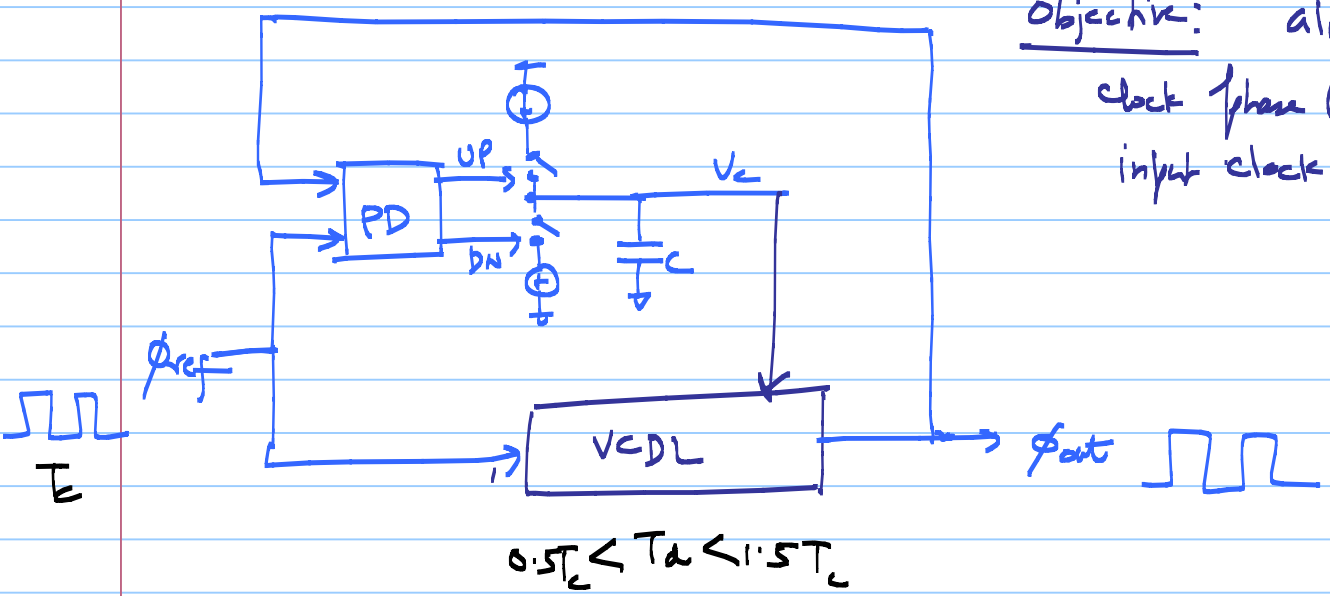
Amplitude to phase conversion



Leeson's Model for phase noise



Delay Locked Loop (DLL)



Objective: align the output clock phase (ϕ_{out}) to the input clock (ϕ_{ref})

$0.5T_c < T_d < 1.5T_c$

At steady-state

VCDL delay = T_c