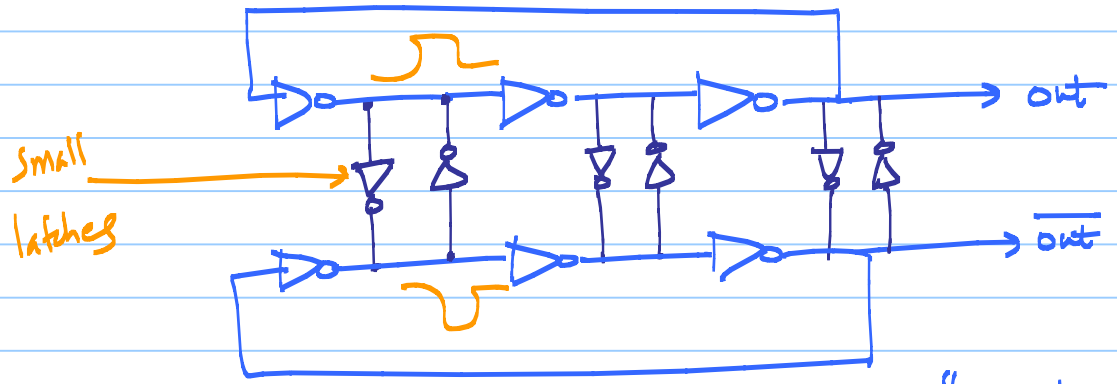
ECE 518 - Lecture 21

Note Title 4/9/2013

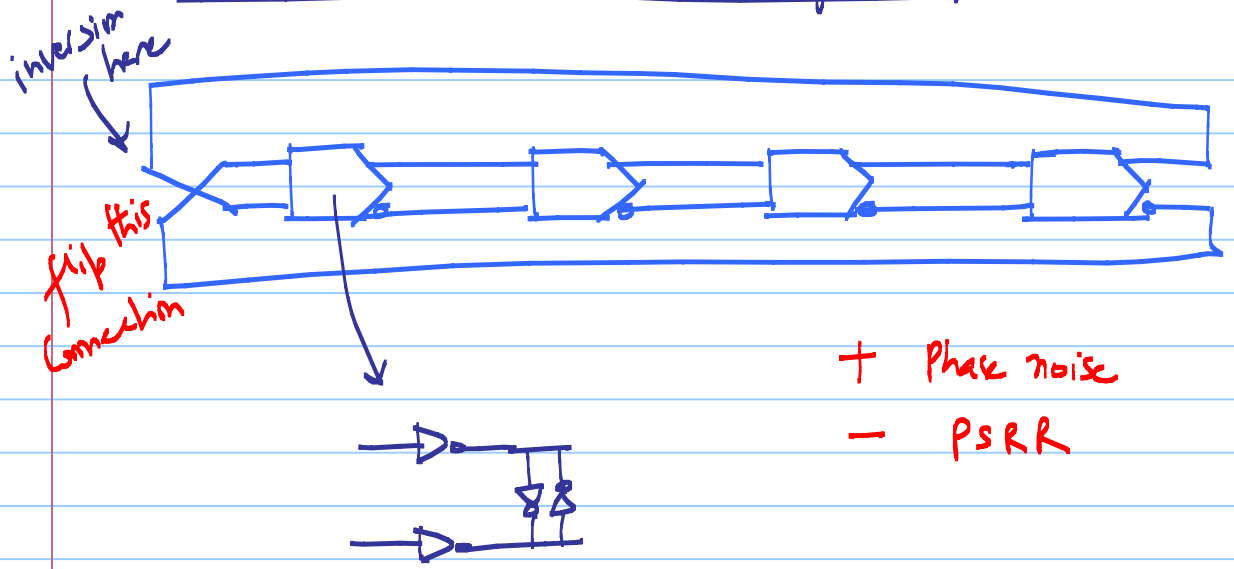
I, V_{DD}, C_{eff}



* frequency slows as the latches fight the ring oscillator

"pseudo-differential"

Vco with with even delay steps

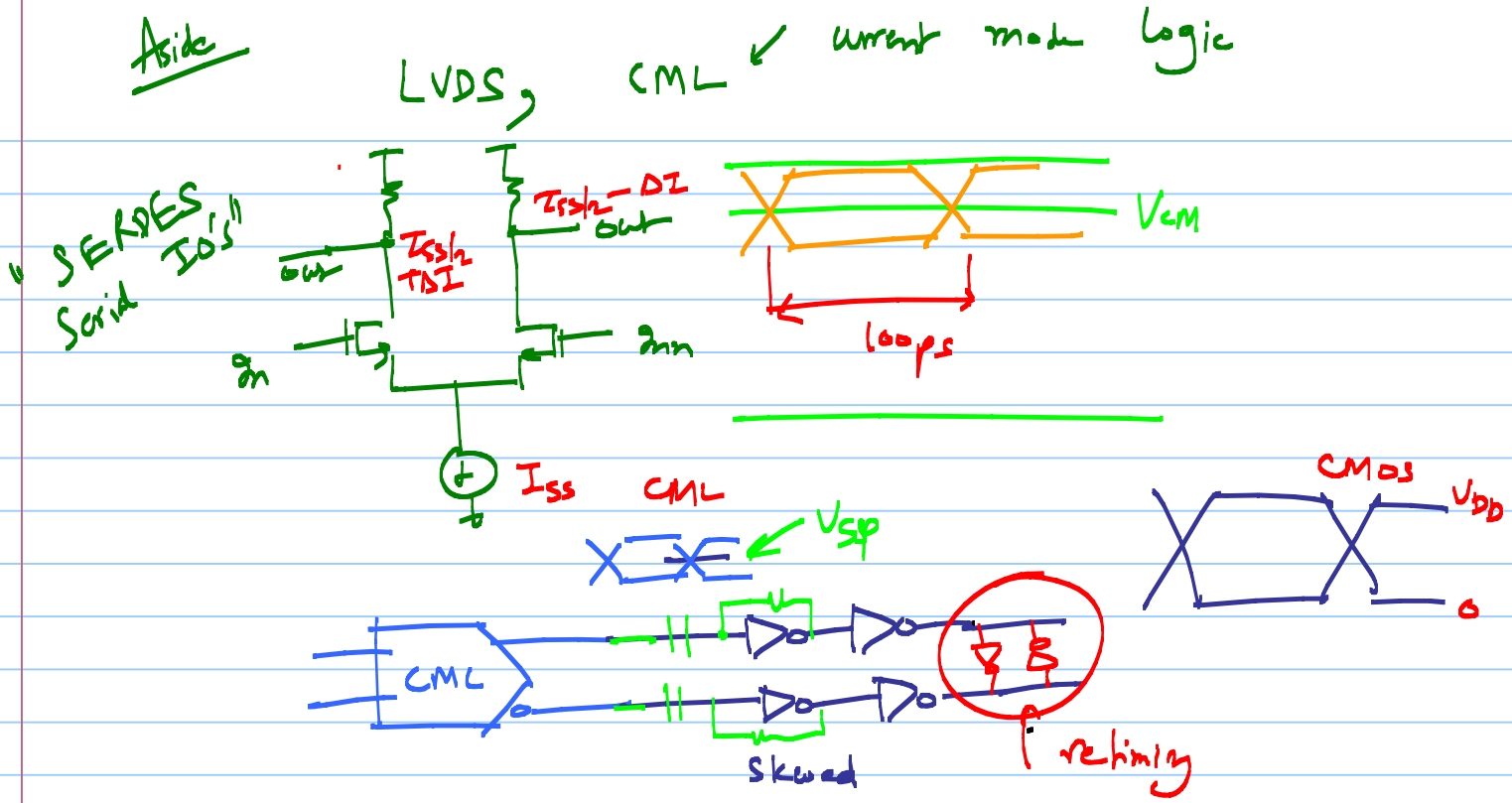


+ Phase noise

− PSRR

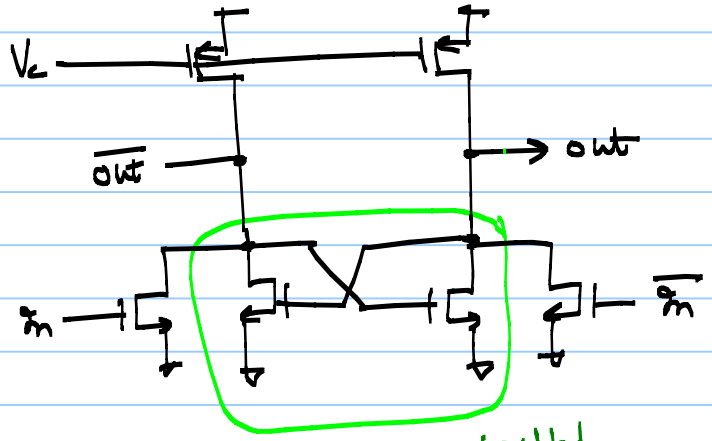
Aside

LVDS, CML ← current mode logic

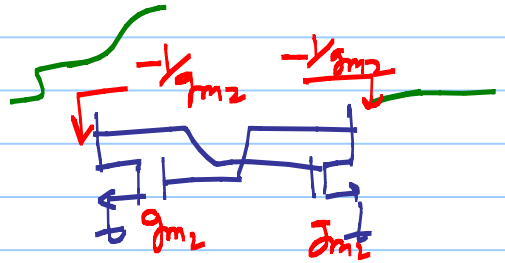


CML – CMOS converter

Pseudo-Differential Delay Cells



"Cross Coupled Latch"



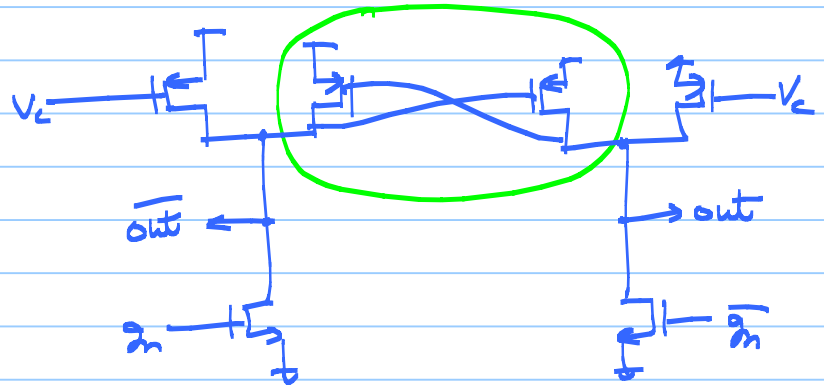
$$\tau = RC$$

$$\left(r_{op} \| r_{on} - \frac{1}{g_{m2}}\right) C_L$$

* wide tuning range

(-) Assymetric output waveforms
  ↳ duty cycle distortion

(-) Poor PSRR


V_c
V_c
$\overline{out}$
out
g_m
$\overline{g_m}$

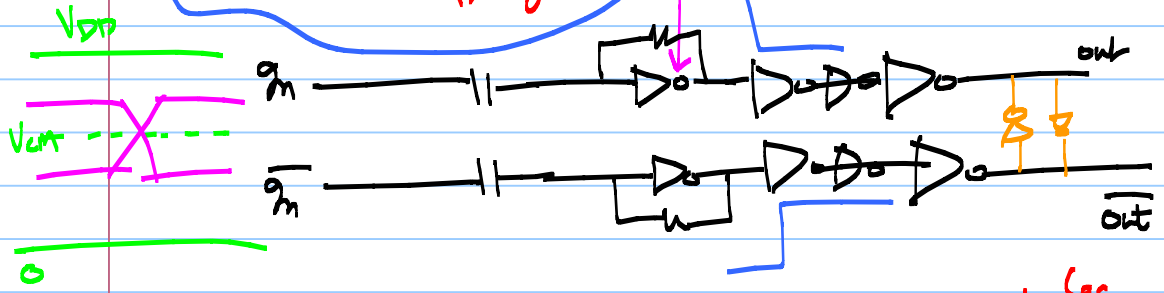
VCO Buffers

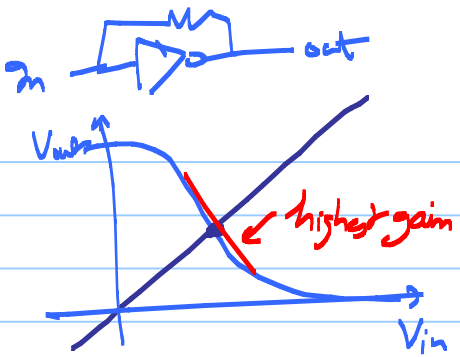
* Convert low-swing VCO output to full-swing

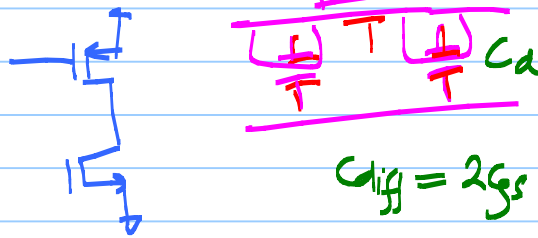
  * Requirements:
    - ↳ least loading C_{in} ↓↓
    - → 50% output duty cycle
    - → fast rise/fall times
    - → Power ↓
    - → PSSR ↑

Weste Harris Logical Effort Theory

for minimum A => FO4

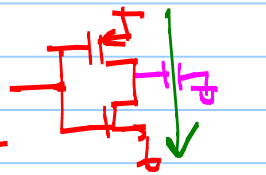






Cdiff = 2Cgs

Crowbar current



Noise in PLL

Deterministic

* Supply noise
* Coupling noise
* Substrate noise

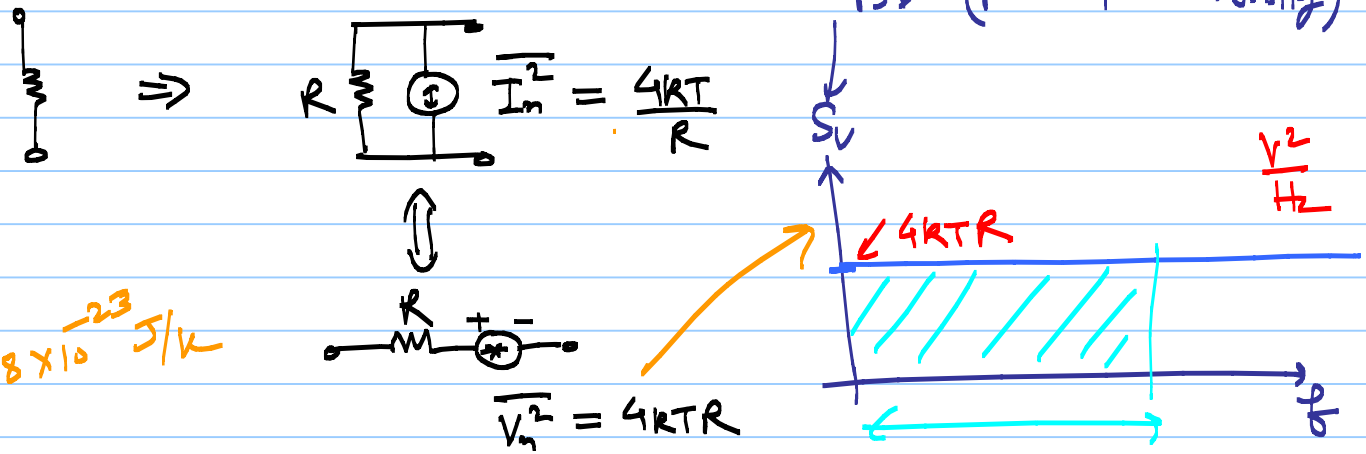
"reference feed through"

Random

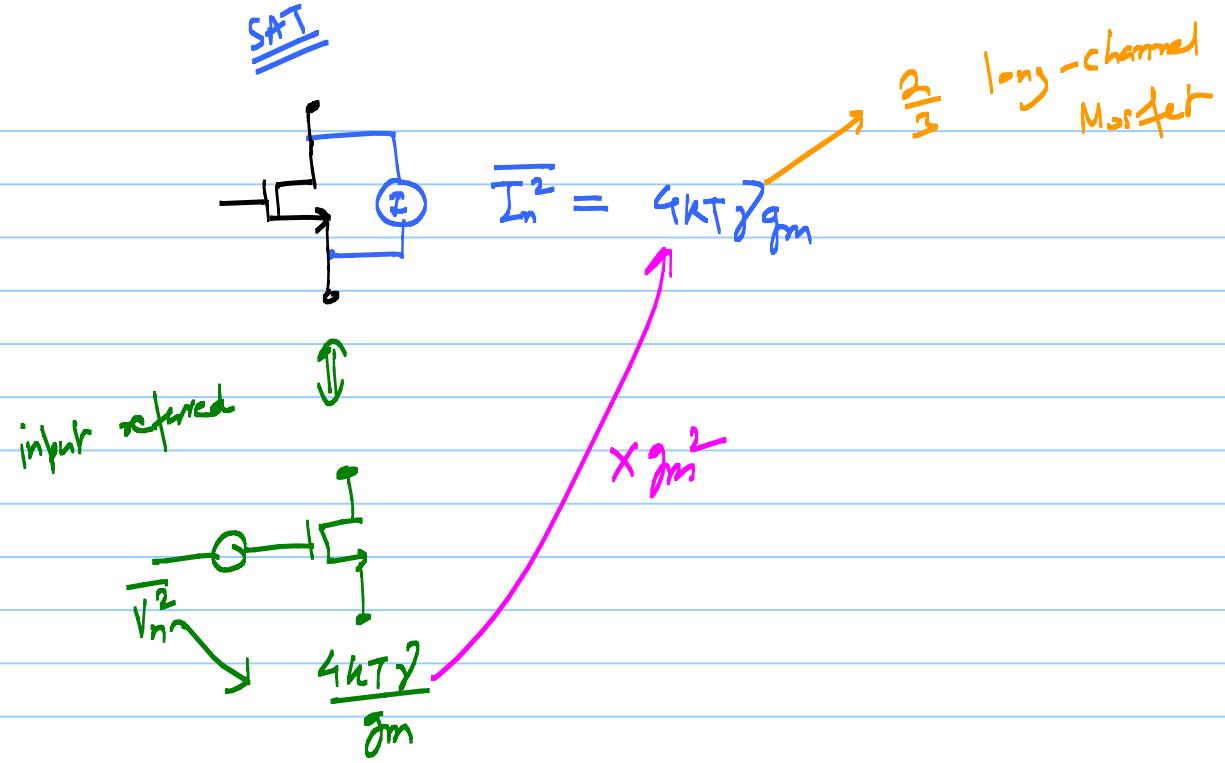
→ Thermal

→ Flicker noise

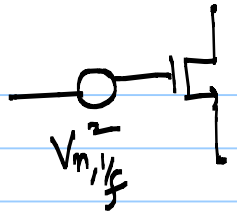
Thermal Noise



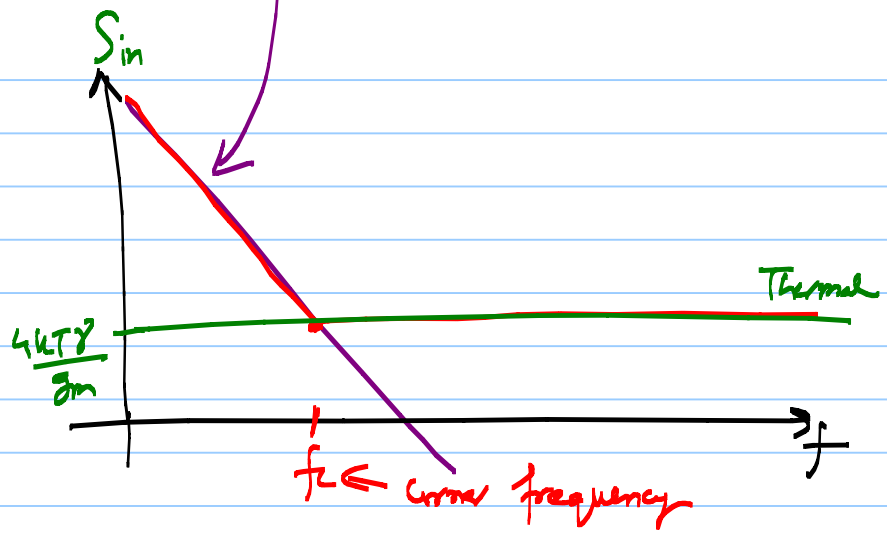
$k = 1.38 \times 10^{-23}$ J/K

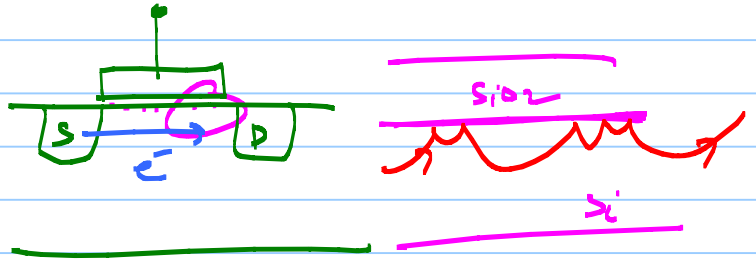

SAT
$\overline{I_n^2} = 4kT\gamma g_m$
$\frac{2}{3}$ long-channel MOSFET
input referred
$\overline{V_n^2}$
$\frac{4kT\gamma}{g_m}$
$\times g_m^2$

Flicker Noise ($1/f$ noise)



$$\overline{V_{n,1/f}^2} = \frac{K}{WL} \cdot \frac{1}{f}$$





Generic Noise Analysis

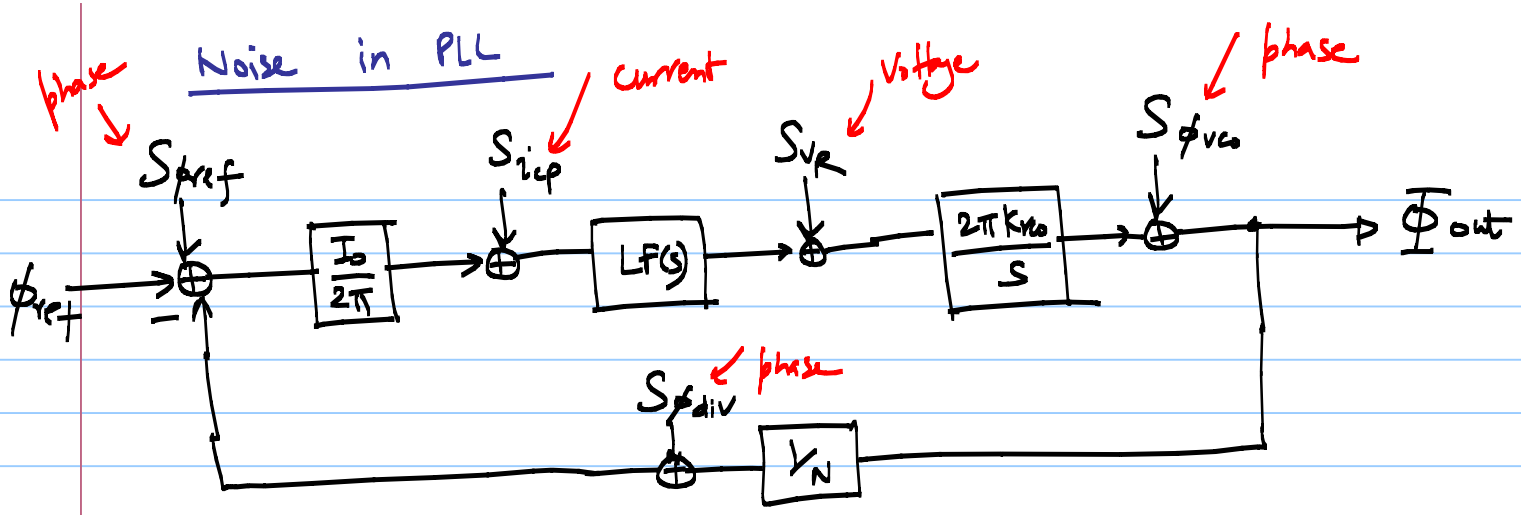
.noise
.pnoise

1. Identify all noise sources
2. Calculate/estimate, PSD of each noise source, $S_i(f)$
3. Evaluate TF from each of the noise sources to the output of the PLL $\left(H_i(f) = \frac{\phi_{out}(s)}{\phi_i(s)} \right)$

* Comm System Class

4. Determine the contribution of each noise source to the output $\Rightarrow$ $|H_i(f)|^2 \cdot S_i(f)$
5. Sum all the contributions for total output noise $= \sum_i |H_i(f)|^2 \cdot S_i(f)$

Noise in PLL



Noise PSD ⇒

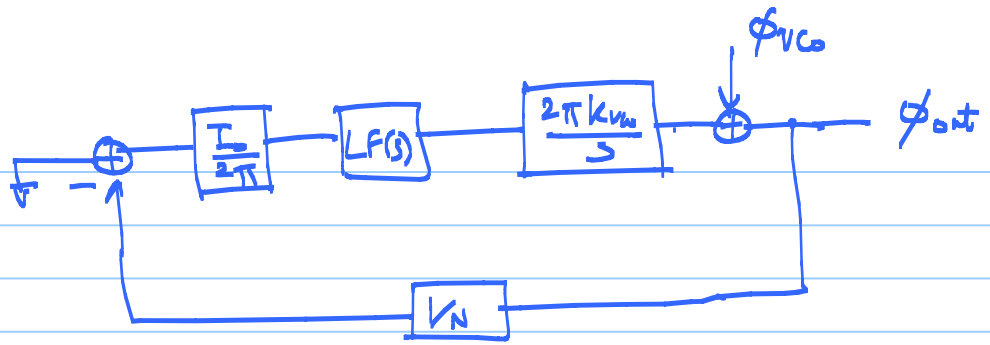
$S_{\phi ref}$ ← reference clock noise

S_{icp} ← PFD/CP noise

S_{VR} ← Loop filter resistor noise

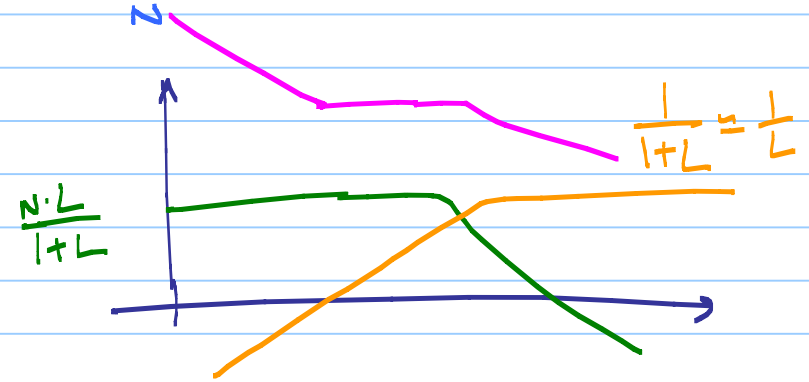
$S_{\phi VCO}$ ← VCO phase noise PSD

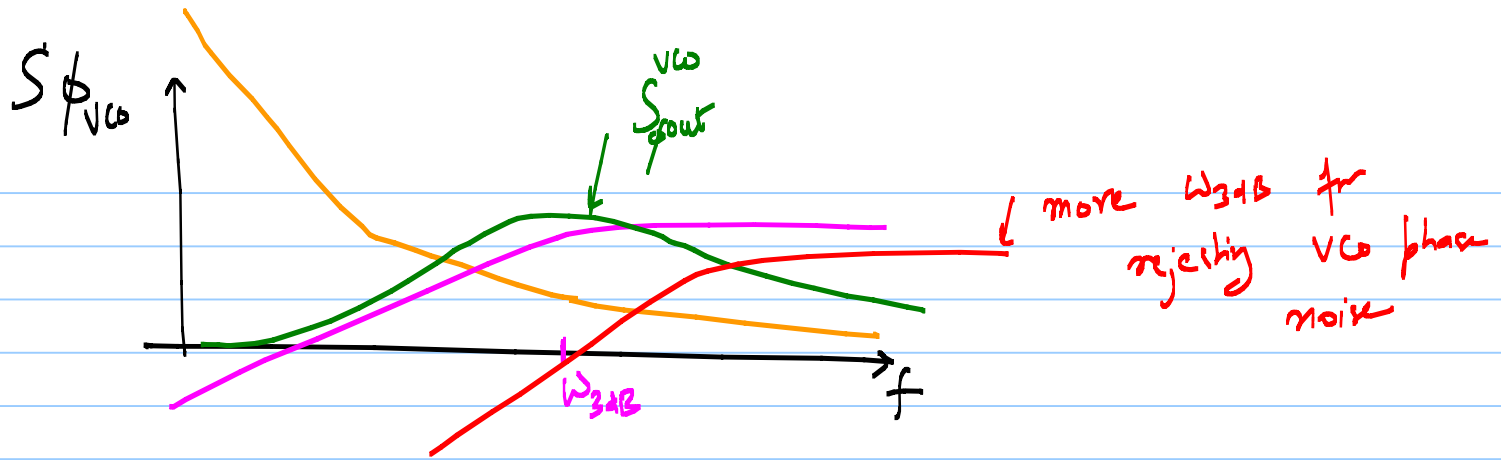
$S_{\phi div}$ ← divider noise



$$L(s) = \frac{I_{cp} K_{VCO}}{N} \cdot LF(s)$$

$$\frac{\phi_{out}}{\phi_{VCO}} = \frac{1}{1 + L(s)}$$




$S_{\phi_{VCO}}$
S^{VCO}_{open}
ω_{3dB}
f
more ω_{3dB} for rejecting VCO phase noise